

# DATA SHEET

**74LVT574**

**3.3V Octal D-type flip-flop (3-State)**

Product specification  
Supersedes data of 1995 Nov 14  
IC23 Data Handbook

1998 Feb 19

3.3V Octal D-type flip-flop (3-State)

74LVT574

FEATURES

- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-State outputs for bus interfacing
- Common output enable
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT574 is a high-performance BiCMOS product designed for V<sub>CC</sub> operation at 3.3V.

This device is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable (OE) control gates. The state of each D input (one set-up time before the Low-to-High clock transition) is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ( $\overline{OE}$ ) controls all eight 3-State buffers independent of the clock operation.

When  $\overline{OE}$  is Low, the stored data appears at the outputs. When  $\overline{OE}$  is High, the outputs are in the High-impedance "off" state, which means they will neither drive nor load the bus.

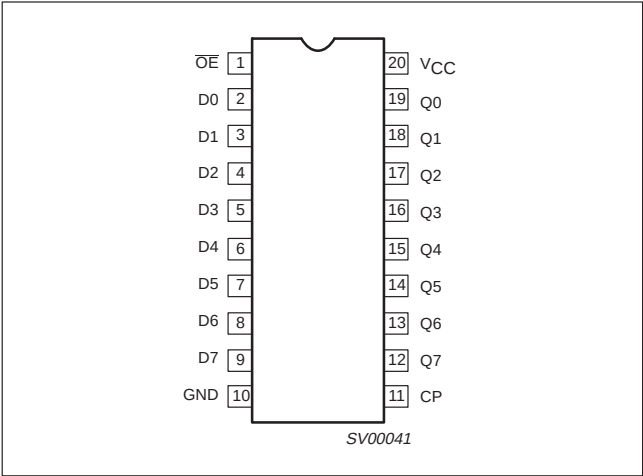
QUICK REFERENCE DATA

| SYMBOL                               | PARAMETER                                 | CONDITIONS<br>T <sub>amb</sub> = 25°C; GND = 0V    | TYPICAL    | UNIT |
|--------------------------------------|-------------------------------------------|----------------------------------------------------|------------|------|
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>CP to Q <sub>n</sub> | C <sub>L</sub> = 50pF;<br>V <sub>CC</sub> = 3.3V   | 3.6<br>4.3 | ns   |
| C <sub>IN</sub>                      | Input capacitance                         | V <sub>I</sub> = 0V or 3.0V                        | 4          | pF   |
| C <sub>OUT</sub>                     | Output capacitance                        | Outputs disabled;<br>V <sub>I/O</sub> = 0V or 3.0V | 8          | pF   |
| I <sub>CCZ</sub>                     | Total supply current                      | Outputs disabled;<br>V <sub>CC</sub> = 3.6V        | 0.13       | mA   |

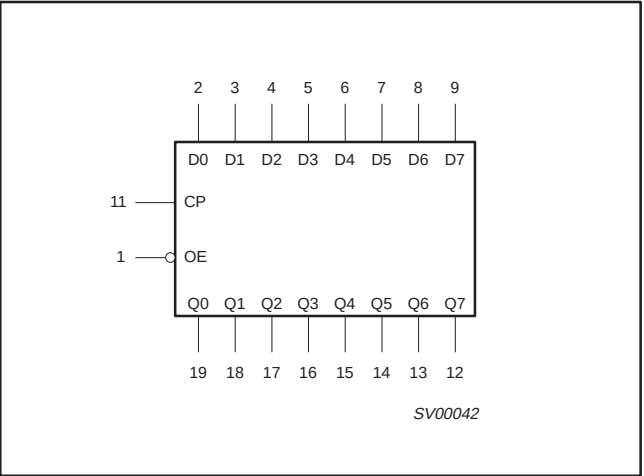
ORDERING INFORMATION

| PACKAGES                    | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|-----------------------------|-------------------|-----------------------|---------------|------------|
| 20-Pin Plastic SOL          | −40°C to +85°C    | 74LVT574 D            | 74LVT574 D    | SOT163-1   |
| 20-Pin Plastic SSOP Type II | −40°C to +85°C    | 74LVT574 DB           | 74LVT574 DB   | SOT339-1   |
| 20-Pin Plastic TSSOP Type I | −40°C to +85°C    | 74LVT574 PW           | 74LVT574PW DH | SOT360-1   |

PIN CONFIGURATION



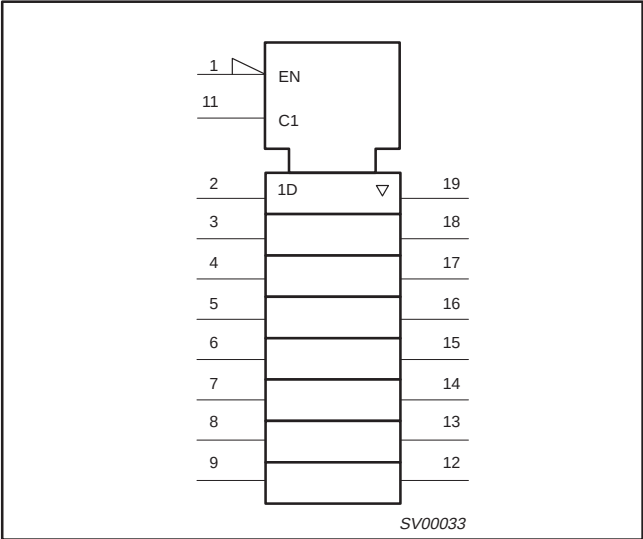
LOGIC SYMBOL



3.3V Octal D-type flip-flop (3-State)

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LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

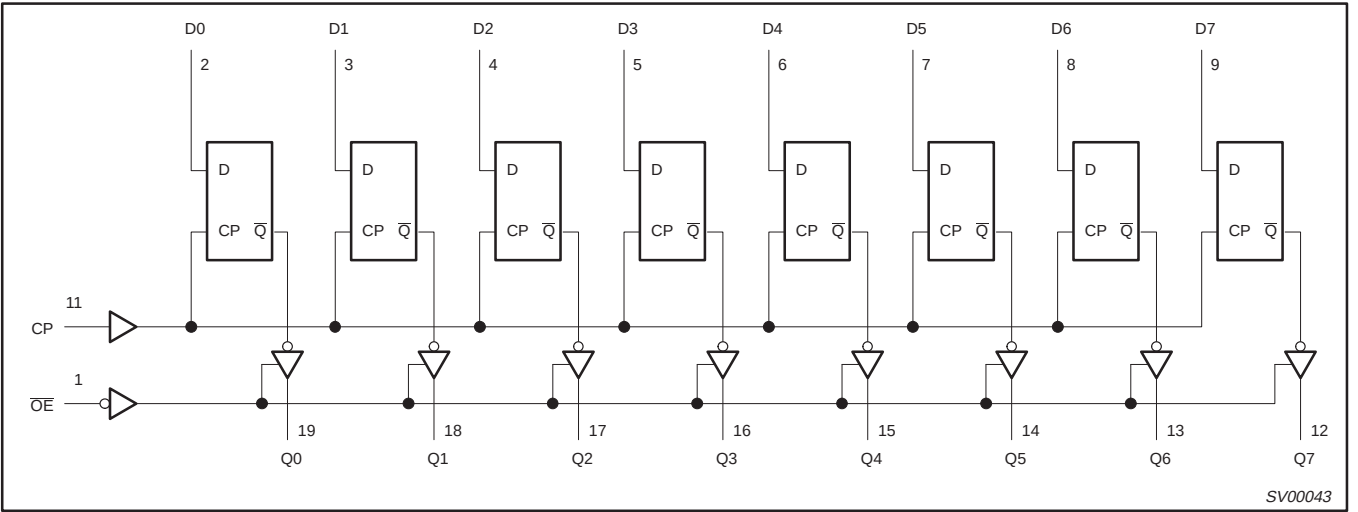
| PIN NUMBER                     | SYMBOL          | FUNCTION                               |
|--------------------------------|-----------------|----------------------------------------|
| 1                              | $\overline{OE}$ | Output enable input (active-low)       |
| 2, 3, 4, 5, 6, 7, 8, 9         | D0-D7           | Data inputs                            |
| 19, 18, 17, 16, 15, 14, 13, 12 | Q0-Q7           | Data outputs                           |
| 11                             | CP              | Clock pulse input (active rising edge) |
| 10                             | GND             | Ground (0V)                            |
| 20                             | V <sub>CC</sub> | Positive supply voltage                |

FUNCTION TABLE

| INPUTS          |            |    | INTERNAL REGISTER | OUTPUTS | OPERATING MODE         |
|-----------------|------------|----|-------------------|---------|------------------------|
| $\overline{OE}$ | CP         | Dn |                   | Q0 – Q7 |                        |
| L               | $\uparrow$ | l  | L                 | L       | Load and read register |
| L               | $\uparrow$ | h  | H                 | H       |                        |
| L               | $\nmid$    | X  | NC                | NC      | Hold                   |
| H               | X          | X  | NC                | Z       | Disable outputs        |

H = High voltage level  
h = High voltage level one set-up time prior to the Low-to-High clock transition  
L = Low voltage level  
l = Low voltage level one set-up time prior to the Low-to-High clock transition  
NC= No change  
X = Don't care  
Z = High impedance "off" state  
 $\uparrow$  = Low-to-High clock transition  
 $\nmid$  = not a Low-to-High clock transition

LOGIC DIAGRAM



## 3.3V Octal D-type flip-flop (3-State)

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**ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>**

| SYMBOL    | PARAMETER                      | CONDITIONS                  | RATING       | UNIT |
|-----------|--------------------------------|-----------------------------|--------------|------|
| $V_{CC}$  | DC supply voltage              |                             | −0.5 to +4.6 | V    |
| $I_{IK}$  | DC input diode current         | $V_I < 0$                   | −50          | mA   |
| $V_I$     | DC input voltage <sup>3</sup>  |                             | −0.5 to +7.0 | V    |
| $I_{OK}$  | DC output diode current        | $V_O < 0$                   | −50          | mA   |
| $V_{OUT}$ | DC output voltage <sup>3</sup> | Output in Off or High state | −0.5 to +7.0 | V    |
| $I_{OUT}$ | DC output current              | Output in Low state         | 128          | mA   |
|           |                                | Output in High state        | −64          |      |
| $T_{stg}$ | Storage temperature range      |                             | −65 to 150   | °C   |

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

**RECOMMENDED OPERATING CONDITIONS**

| SYMBOL              | PARAMETER                                                          | LIMITS |     | UNIT |
|---------------------|--------------------------------------------------------------------|--------|-----|------|
|                     |                                                                    | MIN    | MAX |      |
| $V_{CC}$            | DC supply voltage                                                  | 2.7    | 3.6 | V    |
| $V_I$               | Input voltage                                                      | 0      | 5.5 | V    |
| $V_{IH}$            | High-level input voltage                                           | 2.0    |     | V    |
| $V_{IL}$            | Input voltage                                                      |        | 0.8 | V    |
| $I_{OH}$            | High-level output current                                          |        | −32 | mA   |
| $I_{OL}$            | Low-level output current                                           |        | 32  | mA   |
|                     | Low-level output current; current duty cycle ≤ 50%, $f \geq 1$ kHz |        | 64  |      |
| $\Delta t/\Delta v$ | Input transition rise or fall rate; outputs enabled                |        | 10  | ns/V |
| $T_{amb}$           | Operating free-air temperature range                               | −40    | +85 | °C   |

## 3.3V Octal D-type flip-flop (3-State)

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## DC ELECTRICAL CHARACTERISTICS

| SYMBOL             | PARAMETER                                                                      | TEST CONDITIONS                                                                                                                 |                        | LIMITS                |                      |      | UNIT |
|--------------------|--------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|------------------------|-----------------------|----------------------|------|------|
|                    |                                                                                |                                                                                                                                 |                        | Temp = -40°C to +85°C |                      |      |      |
|                    |                                                                                |                                                                                                                                 |                        | MIN                   | TYP <sup>1</sup>     | MAX  |      |
| V <sub>IK</sub>    | Input clamp voltage                                                            | V <sub>CC</sub> = 2.7V; I <sub>IK</sub> = -18mA                                                                                 |                        |                       | -0.9                 | -1.2 | V    |
| V <sub>OH</sub>    | High-level output voltage                                                      | V <sub>CC</sub> = 2.7 to 3.6V; I <sub>OH</sub> = -100μA                                                                         |                        | V <sub>CC</sub> -0.2  | V <sub>CC</sub> -0.1 |      | V    |
|                    |                                                                                | V <sub>CC</sub> = 2.7V; I <sub>OH</sub> = -8mA                                                                                  |                        | 2.4                   | 2.5                  |      |      |
|                    |                                                                                | V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -32mA                                                                                 |                        | 2.0                   | 2.2                  |      |      |
| V <sub>OL</sub>    | Low-level output voltage                                                       | V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 100μA                                                                                 |                        |                       | 0.1                  | 0.2  | V    |
|                    |                                                                                | V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 24mA                                                                                  |                        |                       | 0.3                  | 0.5  |      |
|                    |                                                                                | V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 16mA                                                                                  |                        |                       | 0.25                 | 0.4  |      |
|                    |                                                                                | V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 32mA                                                                                  |                        |                       | 0.3                  | 0.5  |      |
|                    |                                                                                | V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 64mA                                                                                  |                        |                       | 0.4                  | 0.55 |      |
| V <sub>RST</sub>   | Power-up output low voltage <sup>5</sup>                                       | V <sub>CC</sub> = 3.6V; I <sub>O</sub> = 1mA; V <sub>I</sub> = GND or V <sub>CC</sub>                                           |                        |                       | 0.13                 | 0.55 | V    |
| I <sub>I</sub>     | Input leakage current                                                          | V <sub>CC</sub> = 0 or 3.6V; V <sub>I</sub> = 5.5V                                                                              |                        |                       | 1                    | 10   | μA   |
|                    |                                                                                | V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND                                                                 | Control pins           |                       | ±0.1                 | ±1   |      |
|                    |                                                                                | V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub>                                                                        | Data pins <sup>4</sup> |                       | 0.1                  | 1    |      |
|                    |                                                                                | V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 0                                                                                      |                        |                       | -1                   | -5   |      |
| I <sub>OFF</sub>   | Output off current                                                             | V <sub>CC</sub> = 0V; V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5V                                                              |                        |                       | 1                    | ±100 | μA   |
| I <sub>HOLD</sub>  | Bus Hold current A inputs <sup>7</sup>                                         | V <sub>CC</sub> = 3V; V <sub>I</sub> = 0.8V                                                                                     |                        | 75                    | 150                  |      | μA   |
|                    |                                                                                | V <sub>CC</sub> = 3V; V <sub>I</sub> = 2.0V                                                                                     |                        | -75                   | -150                 |      |      |
|                    |                                                                                | V <sub>CC</sub> = 0V to 3.6V; V <sub>CC</sub> = 3.6V                                                                            |                        | ±500                  |                      |      |      |
| I <sub>EX</sub>    | Current into an output in the High state when V <sub>O</sub> > V <sub>CC</sub> | V <sub>O</sub> = 5.5V; V <sub>CC</sub> = 3.0V                                                                                   |                        |                       | 60                   | 125  | μA   |
| I <sub>PU/PD</sub> | Power up/down 3-State output current <sup>3</sup>                              | V <sub>CC</sub> ≤ 1.2V; V <sub>O</sub> = 0.5V to V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub> ; OE/OE = Don't care |                        |                       | 1                    | ±100 | μA   |
| I <sub>OZH</sub>   | 3-State output High current                                                    | V <sub>CC</sub> = 3.6V; V <sub>O</sub> = 3V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                                |                        |                       | 1                    | 5    | μA   |
| I <sub>OZL</sub>   | 3-State output Low current                                                     | V <sub>CC</sub> = 3.6V; V <sub>O</sub> = 0.5V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                              |                        |                       | 1                    | -5   | μA   |
| I <sub>CCH</sub>   | Quiescent supply current <sup>3</sup>                                          | V <sub>CC</sub> = 3.6V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0                              |                        |                       | 0.13                 | 0.19 | mA   |
| I <sub>CCL</sub>   |                                                                                | V <sub>CC</sub> = 3.6V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0                               |                        |                       | 3                    | 12   |      |
| I <sub>CCZ</sub>   |                                                                                | V <sub>CC</sub> = 3.6V; Outputs Disabled; V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0 <sup>5</sup>             |                        |                       | 0.13                 | 0.19 |      |
| ΔI <sub>CC</sub>   | Additional supply current per input pin <sup>2</sup>                           | V <sub>CC</sub> = 3V to 3.6V; One input at V <sub>CC</sub> -0.6V, Other inputs at V <sub>CC</sub> or GND                        |                        |                       | 0.1                  | 0.2  | mA   |

## NOTES:

1. All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V<sub>CC</sub> or GND.
3. This parameter is valid for any V<sub>CC</sub> between 0V and 1.2V with a transition time of up to 10msec. From V<sub>CC</sub> = 1.2V to V<sub>CC</sub> = 3.3V ± 0.3V a transition time of 100μsec is permitted. This parameter is valid for T<sub>amb</sub> = 25°C only.
4. Unused pins at V<sub>CC</sub> or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. I<sub>CCZ</sub> is measured with outputs pulled to V<sub>CC</sub> or GND.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

## AC CHARACTERISTICS

GND = 0V, t<sub>R</sub> = t<sub>F</sub> = 2.5ns, C<sub>L</sub> = 50pF, R<sub>L</sub> = 500Ω; T<sub>amb</sub> = -40°C to +85°C.

| SYMBOL                               | PARAMETER                                      | WAVEFORM         | LIMITS                        |                  |            |                        |            | UNIT |
|--------------------------------------|------------------------------------------------|------------------|-------------------------------|------------------|------------|------------------------|------------|------|
|                                      |                                                |                  | V <sub>CC</sub> = 3.3V ± 0.3V |                  |            | V <sub>CC</sub> = 2.7V |            |      |
|                                      |                                                |                  | MIN                           | TYP <sup>1</sup> | MAX        | MIN                    | MAX        |      |
| f <sub>MAX</sub>                     | Maximum clock frequency                        | NO TAG           | 150                           |                  |            | 150                    |            | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>CP to Qn                  | NO TAG           | 1.7<br>2.4                    | 3.6<br>4.3       | 5.4<br>5.9 |                        | 6.2<br>6.6 | ns   |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output enable time<br>to High and Low level    | NO TAG<br>NO TAG | 1.0<br>1.3                    | 2.9<br>3.4       | 4.8<br>5.1 |                        | 5.9<br>6.2 | ns   |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output disable time<br>from High and Low level | NO TAG<br>NO TAG | 1.9<br>1.7                    | 4.0<br>3.2       | 5.5<br>4.5 |                        | 5.9<br>4.5 | ns   |

## NOTE:

1. All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.

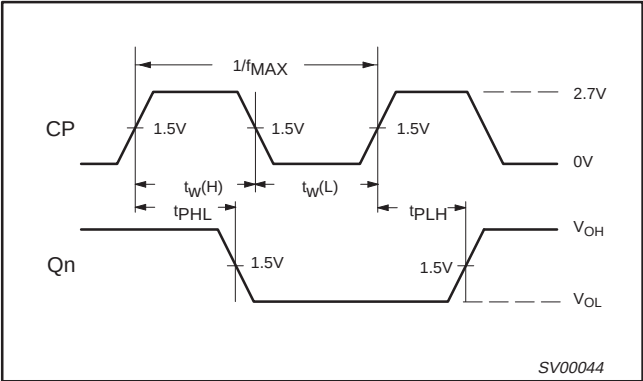
3.3V Octal D-type flip-flop (3-State)

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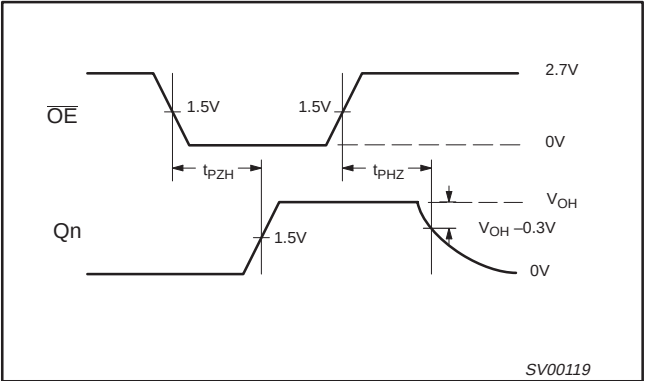
**AC SETUP REQUIREMENTS**  
GND = 0V,  $t_R = t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$ ;  $T_{\text{amb}} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

| SYMBOL                   | PARAMETER                         | WAVEFORM | LIMITS                                 |     |                        | UNIT |
|--------------------------|-----------------------------------|----------|----------------------------------------|-----|------------------------|------|
|                          |                                   |          | $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ |     | $V_{CC} = 2.7\text{V}$ |      |
|                          |                                   |          | MIN                                    | MAX | MIN                    |      |
| $t_{S(H)}$<br>$t_{S(L)}$ | Setup time, High or Low, Dn to CP | NO TAG   | 2.0<br>2.0                             |     | 2.4<br>2.4             | ns   |
| $T_{H(H)}$<br>$T_{H(L)}$ | Hold time, High or Low, Dn to CP  | NO TAG   | 0.3<br>0.3                             |     | 0<br>0                 | ns   |
| $T_{W(H)}$               | CP pulse width High or Low        | NO TAG   | 3.3<br>3.3                             |     | 3.3<br>3.3             | ns   |

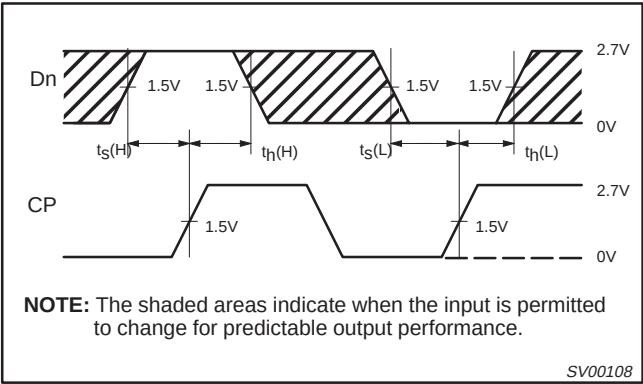
**AC WAVEFORMS**  
 $V_M = 1.5\text{V}$ ,  $V_{IN} = \text{GND to } 2.7\text{V}$



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

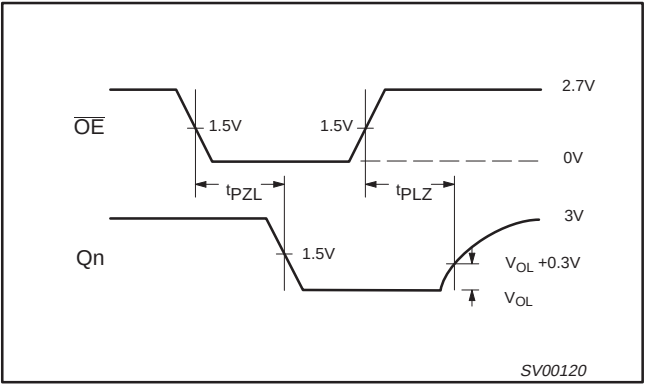


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



**NOTE:** The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 2. Data Setup and Hold Times

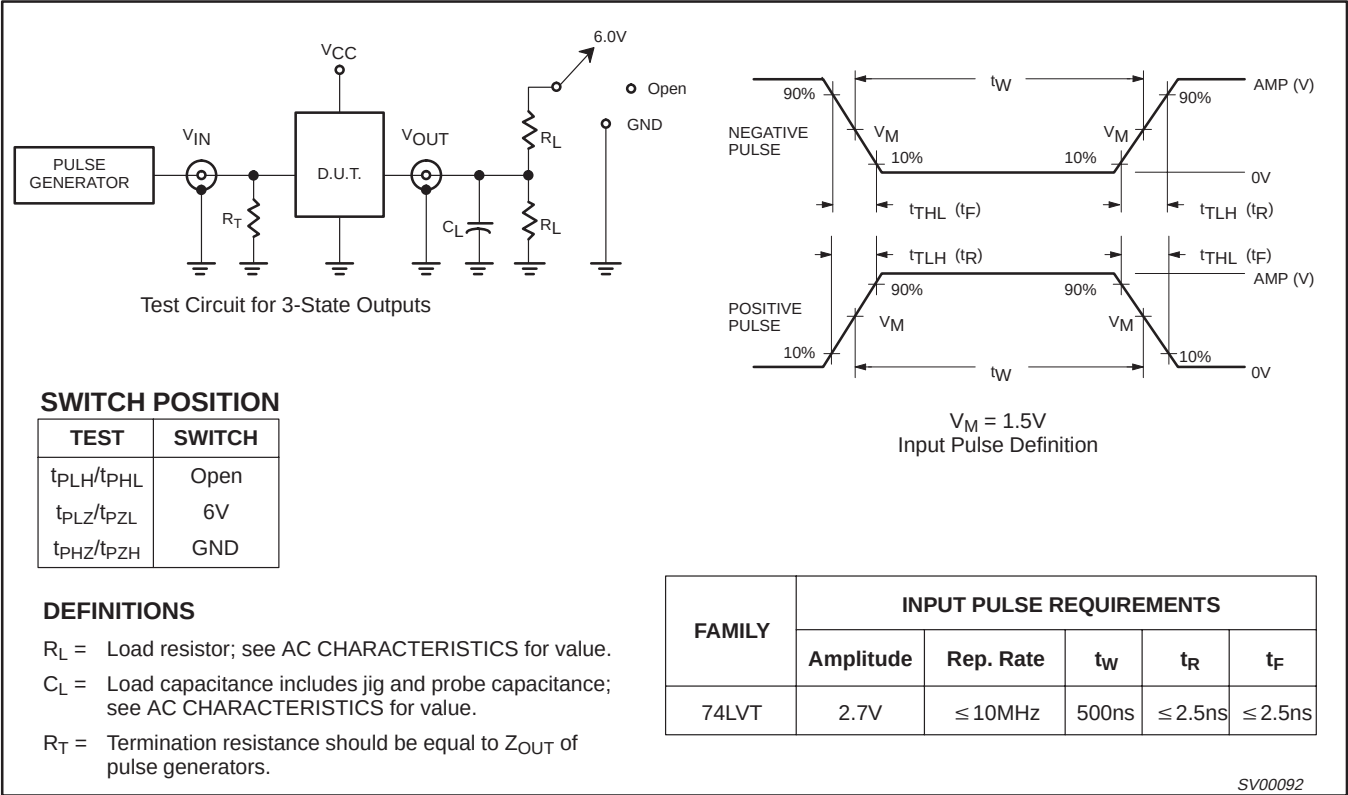


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

3.3V Octal D-type flip-flop (3-State)

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TEST CIRCUIT AND WAVEFORM

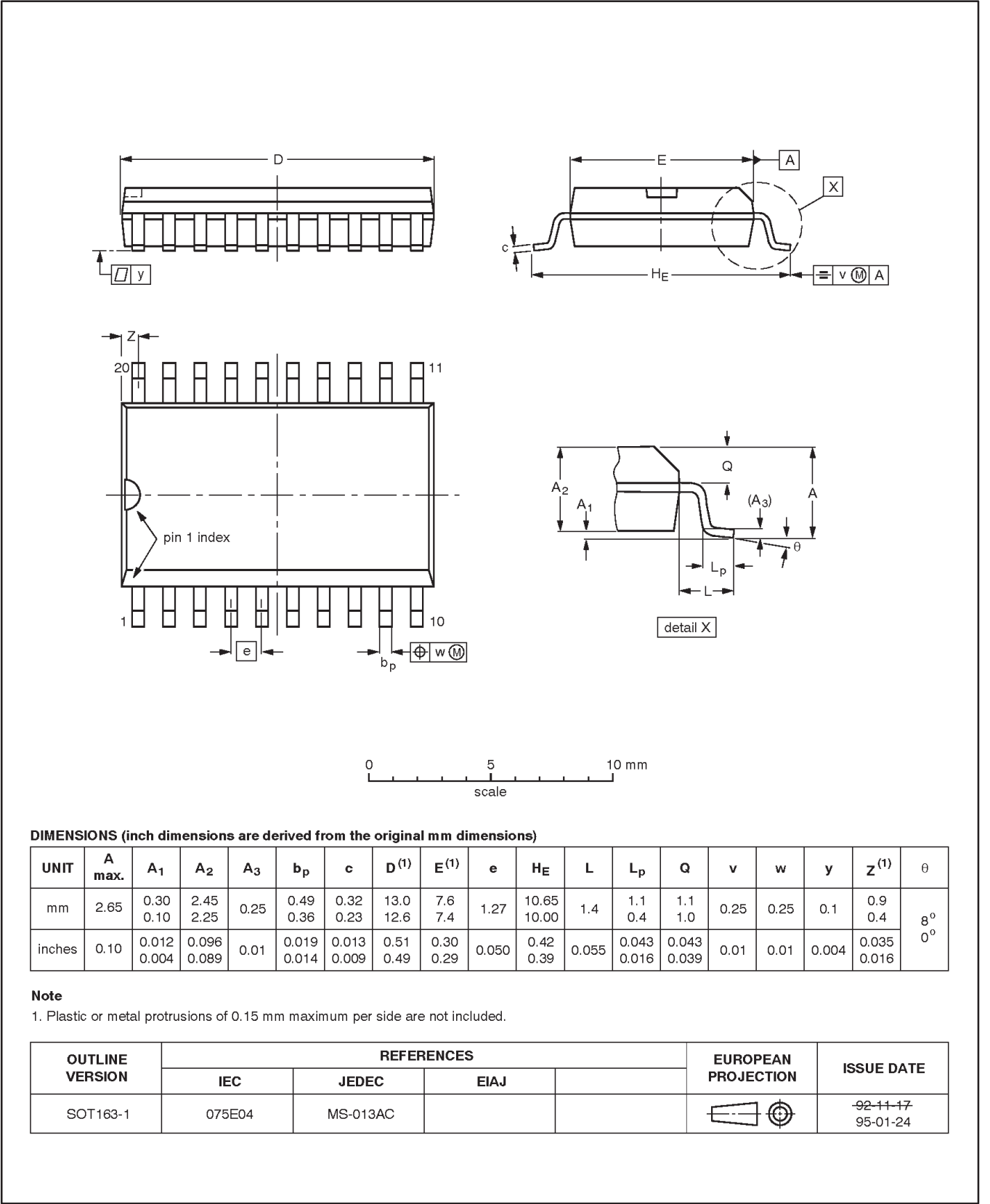


3.3V Octal D-type flip-flop (3-State)

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



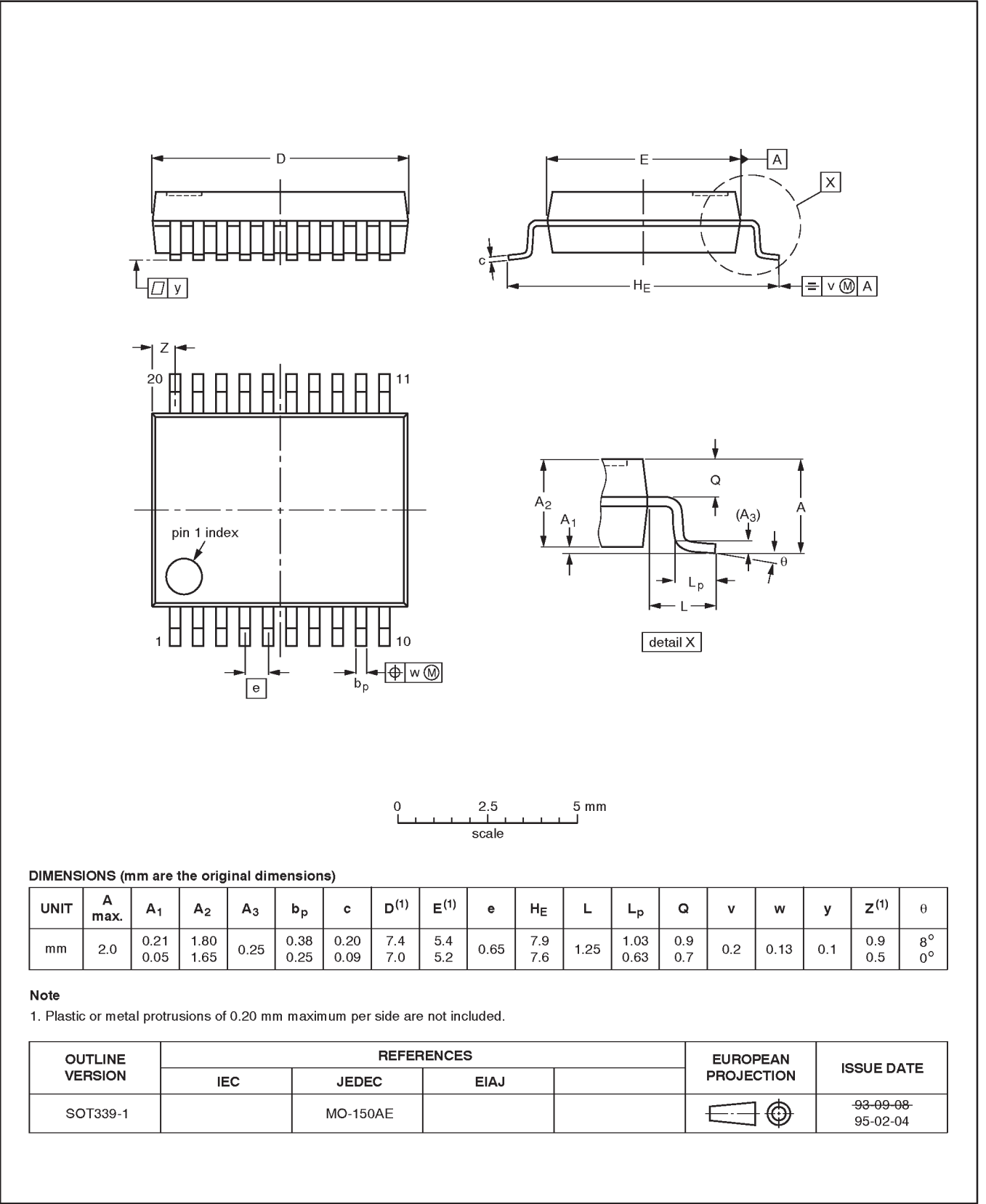


3.3V Octal D-type flip-flop (3-State)

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

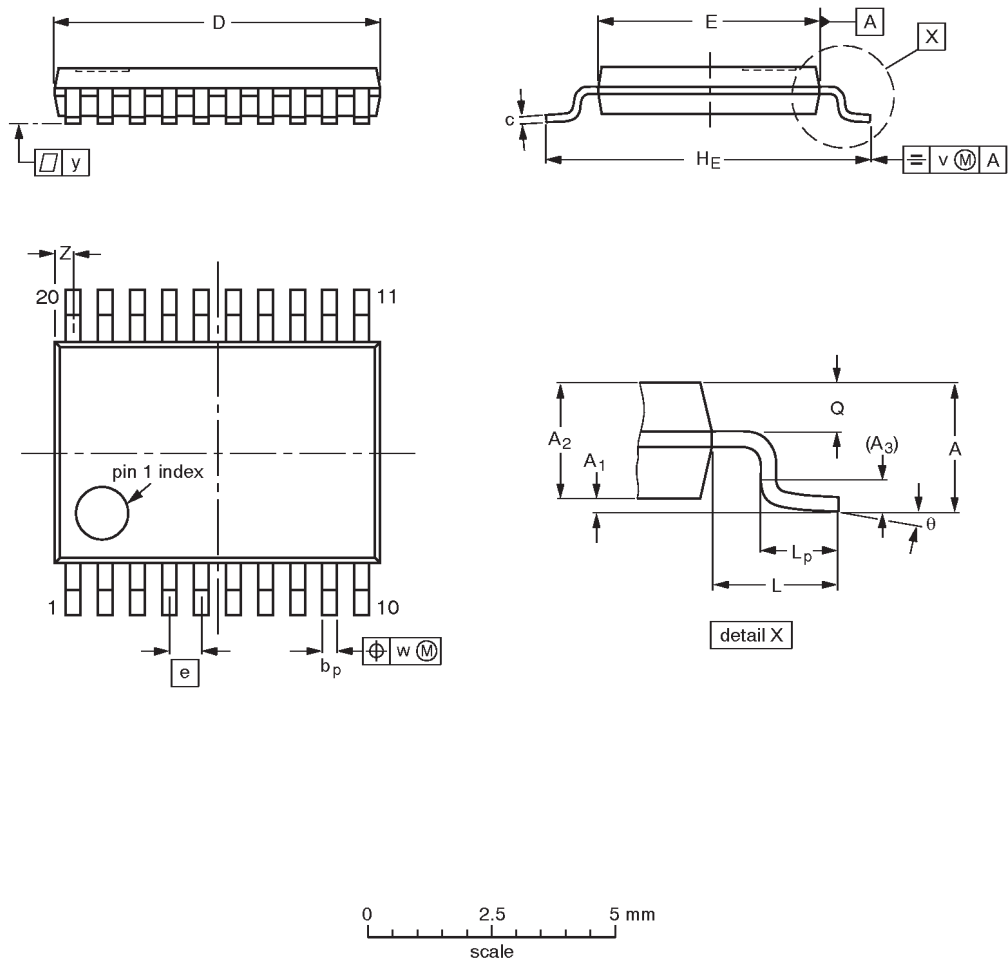


3.3V Octal D-type flip-flop (3-State)

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A<br>max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c          | D <sup>(1)</sup> | E <sup>(2)</sup> | e    | H <sub>E</sub> | L   | L <sub>p</sub> | Q          | v   | w    | y   | Z <sup>(1)</sup> | θ        |
|------|-----------|----------------|----------------|----------------|----------------|------------|------------------|------------------|------|----------------|-----|----------------|------------|-----|------|-----|------------------|----------|
| mm   | 1.10      | 0.15<br>0.05   | 0.95<br>0.80   | 0.25           | 0.30<br>0.19   | 0.2<br>0.1 | 6.6<br>6.4       | 4.5<br>4.3       | 0.65 | 6.6<br>6.2     | 1.0 | 0.75<br>0.50   | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.5<br>0.2       | 8°<br>0° |

- Notes
- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
  - 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE<br>VERSION | REFERENCES |          |      |  | EUROPEAN<br>PROJECTION | ISSUE DATE             |
|--------------------|------------|----------|------|--|------------------------|------------------------|
|                    | IEC        | JEDEC    | EIAJ |  |                        |                        |
| SOT360-1           |            | MO-153AC |      |  |                        | -93-06-16-<br>95-02-04 |

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**NOTES**

### 3.3V Octal D-type flip-flop (3-State)

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### Data sheet status

| <b>Data sheet status</b>  | <b>Product status</b> | <b>Definition <sup>[1]</sup></b>                                                                                                                                                                                                                           |
|---------------------------|-----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Objective specification   | Development           | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.                                                                                                          |
| Preliminary specification | Qualification         | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification     | Production            | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.                                                       |

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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**Philips Semiconductors**  
**811 East Arques Avenue**  
**P.O. Box 3409**  
**Sunnyvale, California 94088-3409**  
**Telephone 800-234-7381**

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