CIRRUS LOGIC®

CS4344/5/6/8

10-Pin, 24-Bit, 192 kHz Stereo D/A Converter

Features

- Multi-bit Delta-Sigma Modulator
- 24-Bit Conversion
- Automatically Detects Sample Rates up to 192 kHz
- 105 dB Dynamic Range
- -95 dB THD+N
- Low Clock Jitter Sensitivity
- Single +3.3 V or +5 V Power Supply
- Filtered Line Level Outputs
- On-Chip Digital De-emphasis
- Popguard™ Technology
- Small 10-Pin TSSOP Package

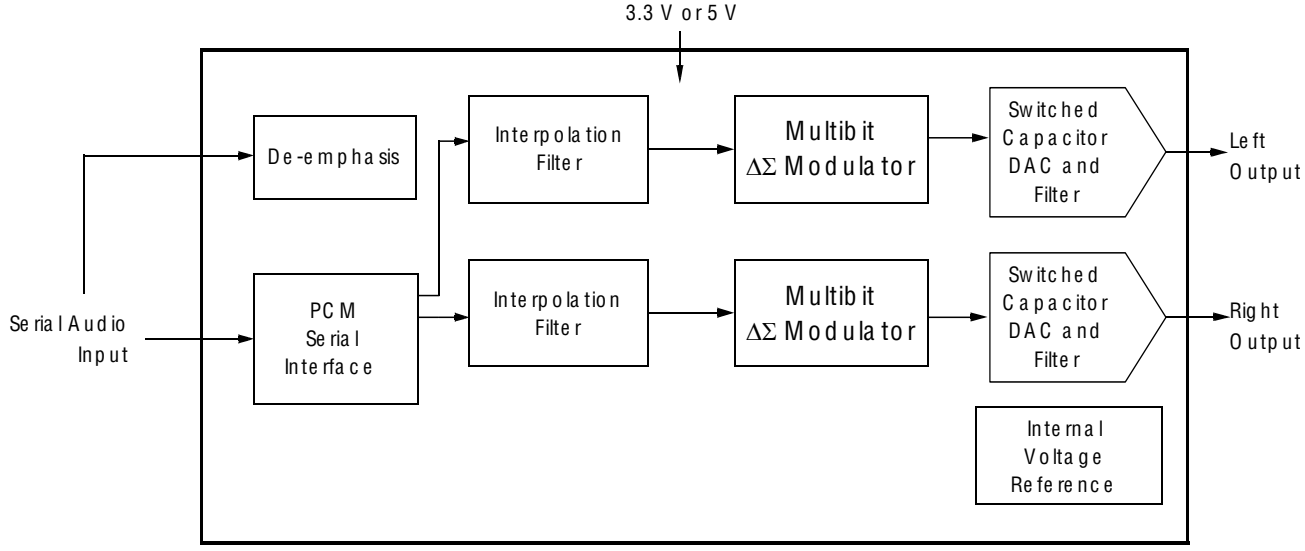
Description

The CS4344 family members are complete, stereo digital-to-analog output systems including interpolation, multi-bit D/A conversion and output analog filtering in a 10-pin package. The CS4344/5/6/8 support all major audio data interface formats, and the individual devices differ only in the supported interface format.

The CS4344 family is based on a fourth order multi-bit delta-sigma modulator with a linear analog low-pass filter. This family also includes auto-speed mode detection using both sample rate and master clock ratio as a method of auto-selecting sampling rates between 2 kHz and 200 kHz.

The CS4344 family contains on-chip digital de-emphasis, operates from a single +3.3 V or +5 V power supply, and requires minimal support circuitry. These features are ideal for DVD players & recorders, digital televisions, home theater and set top box products, and automotive audio systems.

ORDERING INFORMATION
See page 19



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

Revision History

Release	Date	Changes
A1	SEP 2003	Initial Release
PP1	JUN 2004	Updated Minimum Voltage Condition on page 5 Updated Analog Dynamic Performance for 3.3 V operation on page 6 Updated Full Scale Output Voltage on page 6 Updated “High-Level Input Voltage” on page 8 Updated Current Consumption Specifications on page 8 Corrected specifications for “Internal SCLK Mode” on page 9 Updated VQ in “Recommended Connection Diagram” on page 11 Updated Ramp Times for “Output Transient Control” on page 15 Updated Legal Notice
PP2	Sep 2004	Update lead-free device ordering info.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to www.cirrus.com

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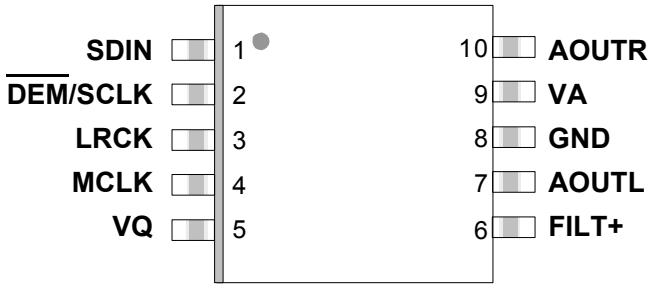
1.PIN DESCRIPTIONS



Pin Name	#	Pin Description
SDIN	1	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
DEM/SCLK	2	**De-Emphasis/External Serial Clock Input** (*Input*) - used for de-emphasis filter control or external serial clock input.
LRCK	3	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	4	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
VQ	5	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
FILT+	6	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
AOUTL	7	**Left Channel Analog Output** (*Output*) - The full scale analog output level is specified in the Analog Characteristics specification table.
GND	8	**Ground** (*Input*) - ground reference.
VA	9	**Analog Power** (*Input*) **-** Positive power for the analog and digital sections.
AOUTR	10	**Right Channel Analog Output** (*Output*) - The full scale analog output level is specified in the Analog Characteristics specification table.

2.CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltage and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS (AGND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Nom	Max	Units
DC Power Supply		VA	4.75 3.00	5.0 3.3	5.25 3.47	V V
Specified Temperature Range	-CZZ -DZZ	T_A	-10 -40	- -	+70 +85	°C °C

ABSOLUTE MAXIMUM RATINGS (AGND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply	VA	-0.3	6.0	V
Input Current, Any Pin Except Supplies	I_{in}	-	±10	mA
Digital Input Voltage	V_{IND}	-0.3	VA+0.4	V
Ambient Operating Temperature (power applied)	T_{op}	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

DAC ANALOG CHARACTERISTICS (Full-Scale Output Sine Wave, 997 Hz (Note 1), Fs = 48/96/192 kHz; Test load R_L = 3 kΩ, C_L = 10 pF (see Figure 1). Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified.)

Parameter			5 V Nom			3.3 V Nom			Unit
			Min	Typ	Max	Min	Typ	Max	
Dynamic Performance for CS4344/5/6/8-CZZ (-10 to 70°C)									
Dynamic Range	18 to 24-Bit	A-weighted	99	105	-	97	103	-	dB
		unweighted	96	102	-	94	100	-	dB
	16-Bit	A-weighted	90	96	-	90	96	-	dB
		unweighted	87	93	-	87	93	-	dB
Total Harmonic Distortion + Noise									
	18 to 24-Bit	0 dB	-	-95	-89	-	-95	-89	dB
		-20 dB	-	-82	-76	-	-80	-74	dB
		-60 dB	-	-42	-36	-	-40	-34	dB
	16-Bit	0 dB	-	-93	-87	-	-93	-87	dB
		-20 dB	-	-73	-67	-	-73	-67	dB
		-60 dB	-	-33	-27	-	-33	-27	dB
Dynamic Performance for CS4344-DZZ (-40 to 85°C)									
Dynamic Range	18 to 24-Bit	A-weighted	95	105	-	93	103	-	dB
		unweighted	92	102	-	90	100	-	dB
	16-Bit	A-weighted	86	96	-	86	96	-	dB
		unweighted	83	93	-	83	93	-	dB
Total Harmonic Distortion + Noise									
	18 to 24-Bit	0 dB	-	-95	-85	-	-95	-85	dB
		-20 dB	-	-82	-72	-	-80	-70	dB
		-60 dB	-	-42	-32	-	-40	-30	dB
	16-Bit	0 dB	-	-93	-83	-	-93	-83	dB
		-20 dB	-	-73	-63	-	-73	-63	dB
		-60 dB	-	-33	-23	-	-33	-23	dB

Note: 1. One-half LSB of triangular PDF dither added to data.

DAC ANALOG CHARACTERISTICS - ALL MODES

Parameter	Symbol	Min	Typ	Max	Unit
Interchannel Isolation (1 kHz)		-	100	-	dB
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	0.25	dB
Gain Drift		-	100	-	ppm/°C
Analog Output					
Full Scale Output Voltage		0.60•VA	0.65•VA	0.70•VA	Vpp
Quiescent Voltage	V_Q	-	0.5•VA	-	VDC
Max DC Current draw from an AOUT pin	I_{OUTmax}	-	10	-	µA
Max Current draw from VQ	I_{Qmax}	-	100	-	µA
Max AC-Load Resistance (see Figure 2 on page 8)	R_L	-	3	-	kΩ
Max Load Capacitance (see Figure 2)	C_L	-	100	-	pF
Output Impedance	Z_{OUT}	-	100	-	Ω

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE (The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.) (See note 6)

Parameter		Symbol	Min	Typ	Max	Unit
Combined Digital and On-chip Analog Filter Response			***Single Speed Mode***			
Passband (Note 2)	to -0.05 dB corner		0	-	.4780	Fs
	to -3 dB corner		0	-	.4996	Fs
Frequency Response 10 Hz to 20 kHz			-.01	-	+.08	dB
StopBand			.5465	-	-	Fs
StopBand Attenuation	(Note 3)		50	-	-	dB
Group Delay		tgd	-	10/Fs	-	s
De-emphasis Error (Note 5)	Fs = 32 kHz		-	-	+1.5/+0	dB
	Fs = 44.1 kHz		-	-	+.05/-.25	dB
	Fs = 48 kHz		-	-	-.2/-.4	dB
Combined Digital and On-chip Analog Filter Response			***Double Speed Mode***			
Passband (Note 2)	to -0.1 dB corner		0	-	.4650	Fs
	to -3 dB corner		0	-	.4982	Fs
Frequency Response 10 Hz to 20 kHz			-.05	-	+.2	dB
StopBand			.5770	-	-	Fs
StopBand Attenuation	(Note 3)		55	-	-	dB
Group Delay		tgd	-	5/Fs	-	s
Combined Digital and On-chip Analog Filter Response			***Quad Speed Mode***			
Passband (Note 2)	to -0.1 dB corner		0	-	0.397	Fs
	to -3 dB corner		0	-	0.476	Fs
Frequency Response 10 Hz to 20 kHz			0	-	+0.00004	dB
StopBand			0.7	-	-	Fs
StopBand Attenuation	(Note 3)		51	-	-	dB
Group Delay		tgd	-	2.5/Fs	-	s

Notes:
2. Response is clock dependent and will scale with Fs.
3. For Single Speed Mode, the Measurement Bandwidth is 0.5465 Fs to 3 Fs.
   For Double Speed Mode, the Measurement Bandwidth is 0.577 Fs to 1.4 Fs.
   For Quad Speed Mode, the Measurement Bandwidth is 0.7 Fs to 1 Fs.
4. Refer to Figure 2.
5. De-emphasis is available only in Single Speed Mode.
6. Amplitude vs. Frequency plots of this data are available in “Appendix” on page 21.

DIGITAL INPUT CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	(% of VA)	V_{IH}	55%	-	-	V
Low-Level Input Voltage	(% of VA)	V_{IL}	-	-	30%	V
Input Leakage Current	(Note 7)	I_{in}	-	-	±10	μA
Input Capacitance			-	8	-	pF

7. I_{in} for LRCK is ±20 μA max.

POWER AND THERMAL CHARACTERISTICS

Parameters	Symbol	5 V Nom			3.3 V Nom			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supplies								
Power Supply Current normal operation	I_A	-	22	30	-	16	21	mA
(Note 8) power-down state (Note 9)	I_A	-	220	-	-	100	-	μA
Power Dissipation normal operation		-	110	150	-	53	69	mW
power-down state (Note 9)		-	1.1	-	-	0.33	-	mW
Package Thermal Resistance	θ_{JA}	-	95	-	-	95	-	°C/Watt
Power Supply Rejection Ratio (Note 8) (1 kHz)	PSRR	-	60	-	-	60	-	dB
(60 Hz)		-	40	-	-	40	-	dB

8. Current consumption increases with increasing FS and increasing MCLK. Typ and Max values are based on highest FS and highest MCLK. Variance between speed modes is small.
9. Power down mode is defined when all clock and data lines are held static.
10. Valid with the recommended capacitor values on VQ and FILT+ as shown in the typical connection diagram in Section 3.

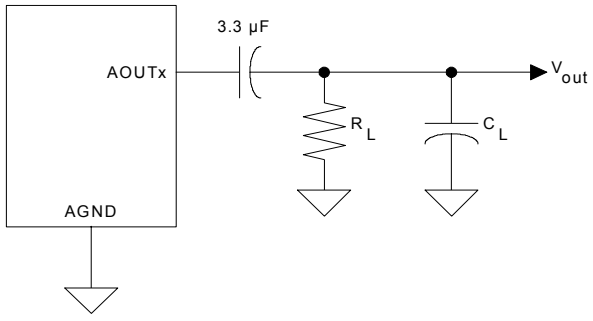


Figure 1. Output Test Load

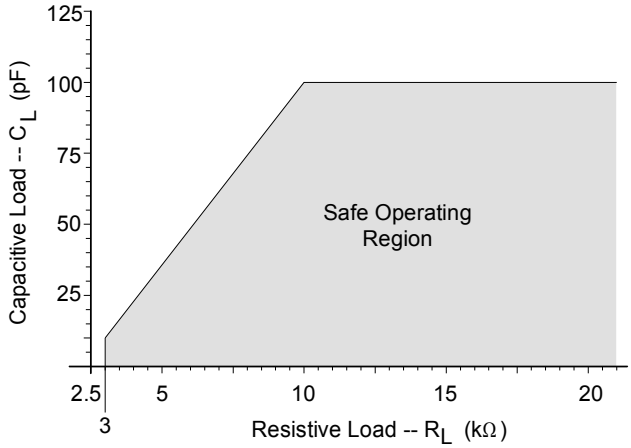


Figure 2. Maximum Loading

SWITCHING CHARACTERISTICS - SERIAL AUDIO INTERFACE

Parameters	Symbol	Min	Typ	Max	Units
MCLK Frequency		0.512	-	50	MHz
MCLK Duty Cycle		45	-	55	%
Input Sample Rate All MCLK/LRCK ratios combined	Fs	2		200	kHz
(Note 11) 256x, 384x, 1024x		2		50	kHz
256x, 384x		84		134	kHz
512x, 768x		42		67	kHz
1152x		30		34	kHz
128x, 192x		50		100	kHz
64x, 96x		100		200	kHz
128x, 192x		168		200	kHz
External SCLK Mode					
LRCK Duty Cycle (External SCLK only)		45	50	55	%
SCLK Pulse Width Low	t_{sclkl}	20	-	-	ns
SCLK Pulse Width High	t_{sclkh}	20	-	-	ns
SCLK Duty Cycle		45	50	55	%
SCLK rising to LRCK edge delay	t_{slrd}	20	-	-	ns
SCLK rising to LRCK edge setup time	t_{slrs}	20	-	-	ns
SDIN valid to SCLK rising setup time	t_{sdlrs}	20	-	-	ns
SCLK rising to SDIN hold time	t_{sdh}	20	-	-	ns
Internal SCLK Mode					
LRCK Duty Cycle (Internal SCLK only) (Note 12)		-	50	-	%
SCLK Period (Note 13)	t_{sclkw}	$\frac{10^9}{SCLK}$	-	-	ns
SCLK rising to LRCK edge	t_{sclkr}	-	$\frac{tsclkw}{2}$	-	µs
SDIN valid to SCLK rising setup time	t_{sdlrs}	$\frac{10^9}{(512)Fs} + 10$	-	-	ns
SCLK rising to SDIN hold time MCLK / LRCK =1152, 1024, 512, 256, 128, or 64	t_{sdh}	$\frac{10^9}{(512)Fs} + 15$	-	-	ns
SCLK rising to SDIN hold time MCLK / LRCK = 768, 384, 192, or 96	t_{sdh}	$\frac{10^9}{(384)Fs} + 15$	-	-	ns

Notes: 11. Not all sample rates are supported for all clock ratios. See table “Common Clock Frequencies” on page 12 for supported ratio’s and frequencies.

12. In Internal SCLK Mode, the Duty Cycle must be 50% +/– 1/2 MCLK Period.

13. The SCLK / LRCK ratio may be either 32, 48, 64, or 72. This ratio depends on part type and MCLK/LRCK ratio. (See figures 7-9)

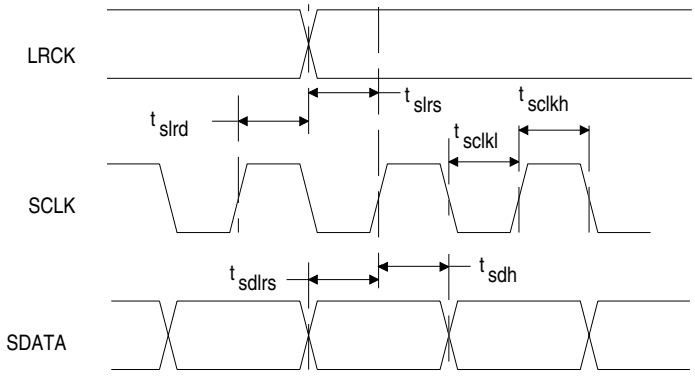


Figure 3. External Serial Mode Input Timing

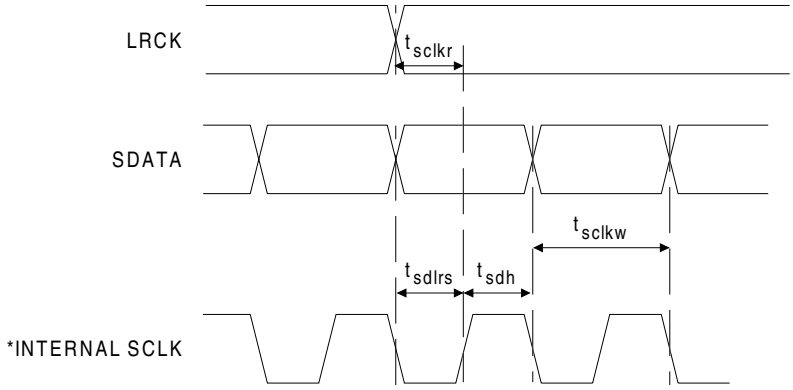


Figure 4. Internal Serial Mode Input Timing

* The SCLK pulses shown are internal to the CS4344/5/6/8.

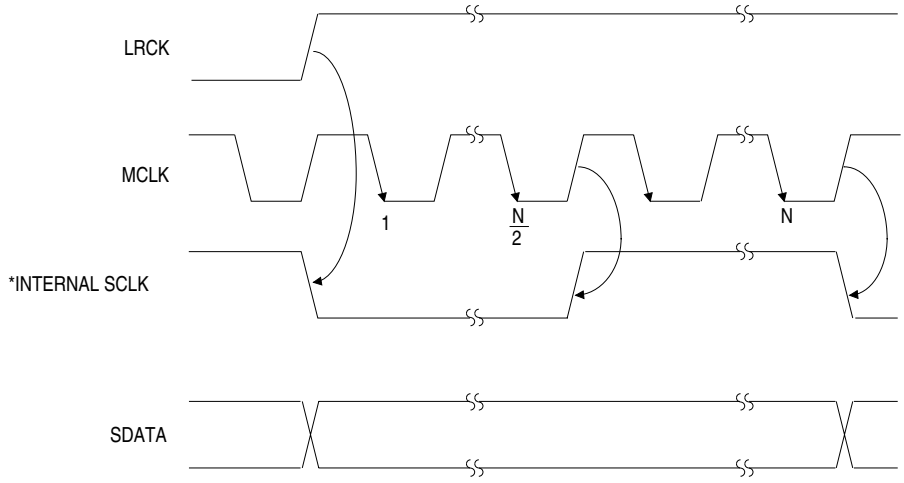


Figure 5. Internal Serial Clock Generation

* The SCLK pulses shown are internal to the CS4344/5/6/8.

N equals MCLK divided by SCLK

3.TYPICAL CONNECTION DIAGRAM

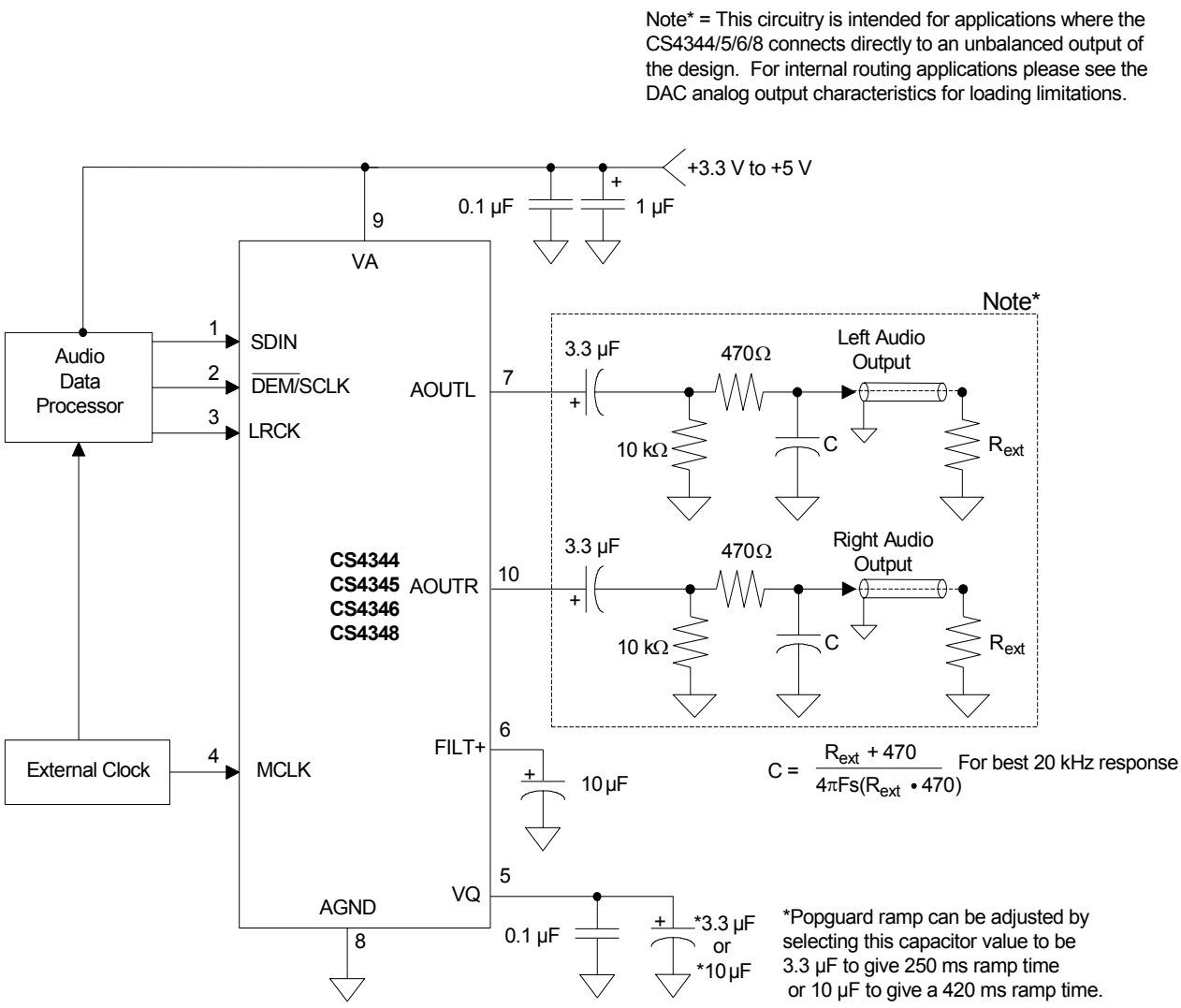


Figure 6. Recommended Connection Diagram

4.APPLICATIONS

The CS4344 family accepts data at standard audio sample rates including 48, 44.1 and 32 kHz in SSM, 96, 88.2 and 64 kHz in DSM, and 192, 176.4 and 128 kHz in QSM. Audio data is input via the serial data input pin (SDIN). The Left/Right Clock (LRCK) determines which channel is currently being input on SDIN, and the optional Serial Clock (SCLK) clocks audio data into the input data buffer. The CS4344/5/6/8 differ in serial data formats as shown in Figures 7-10.

4.1 Master Clock

MCLK/LRCK must be an integer ratio as shown in Table 1. The LRCK frequency is equal to Fs, the frequency at which words for each channel are input to the device. The MCLK-to-LRCK frequency ratio and speed mode is detected automatically during the initialization sequence by counting the number of MCLK transitions during a single LRCK period and by detecting the absolute speed of MCLK. Internal dividers are set to generate the proper clocks. Table 1 illustrates several standard audio sample rates and the required MCLK and LRCK frequencies. Please note there is no required phase relationship, but MCLK, LRCK and SCLK must be synchronous.

LRCK (kHz)	MCLK (MHz)									
	64x	96x	128x	192x	256x	384x	512x	768x	1024x	1152x
32	-	-	-	-	8.1920	12.2880	-	-	32.7680	36.8640
44.1	-	-	-	-	11.2896	16.9344	22.5792	33.8680	45.1580	-
48	-	-	-	-	12.2880	18.4320	24.5760	36.8640	49.1520	-
64	-	-	8.1920	12.2880	-	-	32.7680	49.1520	-	-
88.2	-	-	11.2896	16.9344	22.5792	33.8680	-	-	-	-
96	-	-	12.2880	18.4320	24.5760	36.8640	-	-	-	-
128	8.1920	12.2880	-	-	32.7680	49.1520	-	-	-	-
176.4	11.2896	16.9344	22.5792	33.8680	-	-	-	-	-	-
192	12.2880	18.4320	24.5760	36.8640	-	-	-	-	-	-
Mode	QSM				DSM		SSM			

Table 1. Common Clock Frequencies

4.2 Serial Clock

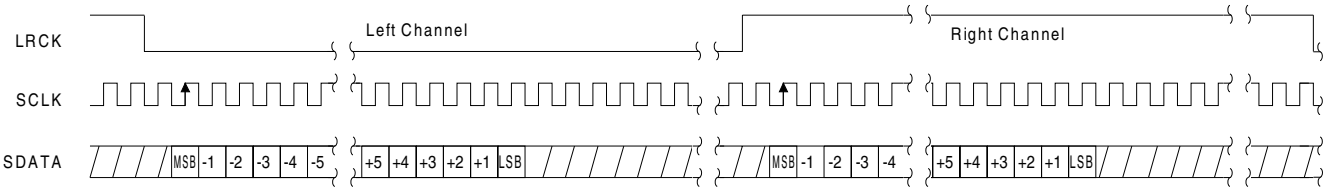
The serial clock controls the shifting of data into the input data buffers. The CS4344 family supports both external and internal serial clock generation modes. Refer to Figures 7-10 for data formats.

4.2.1 External Serial Clock Mode

The CS4344 family will enter the External Serial Clock Mode when 16 low to high transitions are detected on the $\overline{\text{DEM}}$/SCLK pin during any phase of the LRCK period. When this mode is enabled, the Internal Serial Clock Mode and de-emphasis filter cannot be accessed. The CS4344 family will switch to Internal Serial Clock Mode if no low to high transitions are detected on the $\overline{\text{DEM}}$/SCLK pin for 2 consecutive frames of LRCK. Refer to Figure 12.

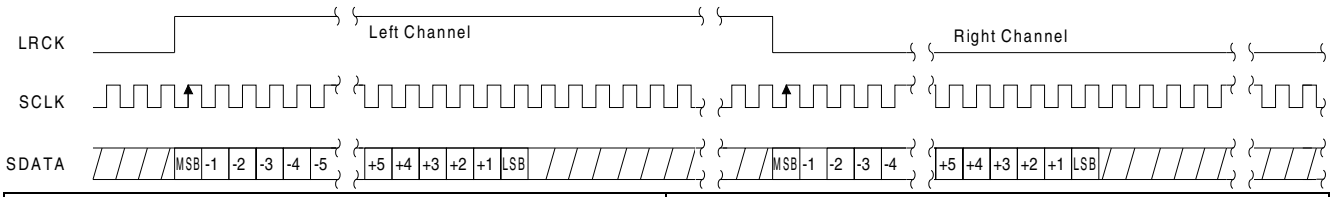
4.2.2 Internal Serial Clock Mode

In the Internal Serial Clock Mode, the serial clock is internally derived and synchronous with MCLK and LRCK. The SCLK/LRCK frequency ratio is either 32, 48, 64, or 72 depending upon data format. Operation in this mode is identical to operation with an external serial clock synchronized with LRCK. This mode allows access to the digital de-emphasis function. Refer to Figures 7 - 12 for details.



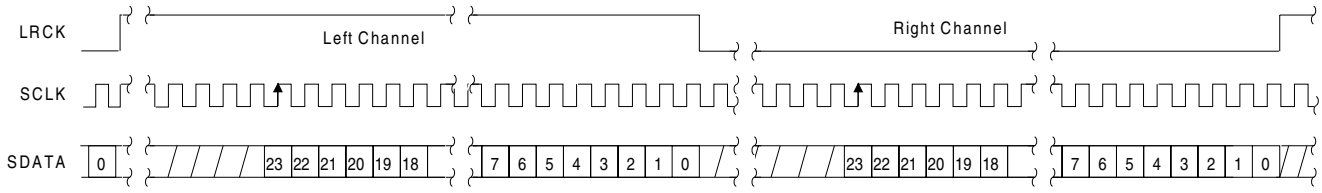
Internal SCLK Mode	External SCLK Mode
I^2S, 16-Bit data and INT SCLK = 32 Fs if MCLK/LRCK = 1024, 512, 256, 128, or 64 I^2S, Up to 24-Bit data and INT SCLK = 48 Fs if MCLK/LRCK = 768, 384, 192, or 96 I^2S, Up to 24-Bit data and INT SCLK = 72 Fs if MCLK/LRCK = 1152	I^2S, up to 24-Bit Data Data Valid on Rising Edge of SCLK

Figure 7. CS4344 Data Format (I^2S)



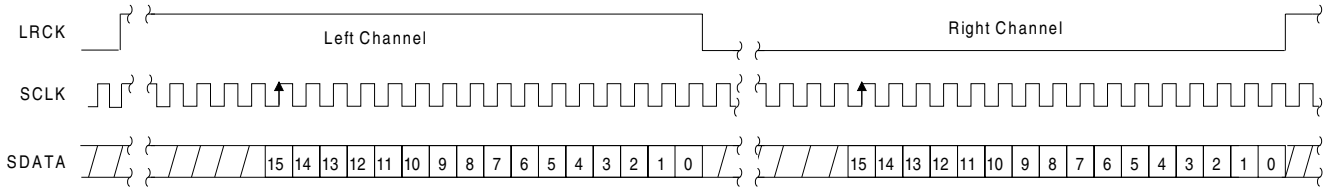
Internal SCLK Mode	External SCLK Mode
Left Justified, up to 24-Bit Data INT SCLK = 64 Fs if MCLK/LRCK = 1024, 512, 256, 128, or 64 INT SCLK = 48 Fs if MCLK/LRCK = 768, 384, 192, or 96 INT SCLK = 72 Fs if MCLK/LRCK = 1152	Left Justified, up to 24-Bit Data Data Valid on Rising Edge of SCLK

Figure 8. CS4345 Data Format (Left Justified)



Internal SCLK Mode	External SCLK Mode
Right Justified, 24-Bit Data INT SCLK = 64 Fs if MCLK/LRCK = 1024, 512, 256, 128, or 64 INT SCLK = 48 Fs if MCLK/LRCK = 768, 384, 192, or 96 INT SCLK = 72 Fs if MCLK/LRCK = 1152	Right Justified, 24-Bit Data Data Valid on Rising Edge of SCLK SCLK Must Have at Least 48 Cycles per LRCK Period

Figure 9. CS4346 Data Format (Right Justified 24)



Internal SCLK Mode	External SCLK Mode
Right Justified, 16-Bit Data INT SCLK = 32 Fs if MCLK/LRCK = 1024, 512, 256, 128, or 64 INT SCLK = 48 Fs if MCLK/LRCK = 768, 384, 192, or 96 INT SCLK = 72 Fs if MCLK/LRCK = 1152	Right Justified, 16-Bit Data Data Valid on Rising Edge of SCLK SCLK Must Have at Least 32 Cycles per LRCK Period

Figure 10. CS4348 Data Format (Right Justified 16)

4.3 De-Emphasis

The CS4344 family includes on-chip digital de-emphasis. Figure 11 shows the de-emphasis curve for Fs equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs.

The de-emphasis filter is active (inactive) if the $\overline{\text{DEM}}$/SCLK pin is low (high) for 5 consecutive falling edges of LRCK. This function is available only in the internal serial clock mode.

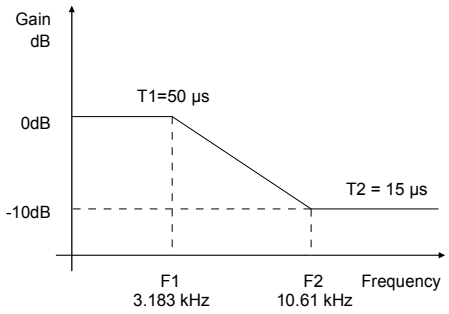


Figure 11. De-Emphasis Curve (Fs = 44.1kHz)

4.4 Initialization and Power-Down

The Initialization and Power-Down sequence flow chart is shown in Figure 12. The CS4344 family enters the Power-Down State upon initial power-up. The interpolation filters and delta-sigma modulators are reset, and the internal voltage reference, multi-bit digital-to-analog converters and switched-capacitor low-pass filters are powered down. The device will remain in the Power-Down mode until MCLK and LRCK are present. Once MCLK and LRCK are detected, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio. Power is then applied to the internal voltage reference. Finally, power is applied to the D/A converters and switched-capacitor filters, and the analog outputs will ramp to the quiescent voltage, VQ.

4.5 Output Transient Control

The CS4344 family uses Popguard™ technology to minimize the effects of output transients during power-up and power-down. This technique eliminates the audio transients commonly produced by single-ended single-supply converters when it is implemented with external DC-blocking capacitors connected in series with the audio outputs. To make best use of this feature, it is necessary to understand its operation.

4.5.1 Power-up

When the device is initially powered-up, the audio outputs, AOUTL and AOUTR, are clamped to VQ which is initially low. After MCLK is applied the outputs begin to ramp with VQ towards the nominal quiescent voltage. This ramp takes approximately 250 ms with a 3.3 µF cap connected to VQ (420 ms with a 10 µF connected to VQ) to complete. The gradual voltage ramping allows time for the external DC-blocking capacitors to charge to VQ, effectively blocking the quiescent DC voltage. Once valid LRCK and SDIN are supplied (and SCLK if used) approximately 2000 sample periods later audio output begins.

4.5.2 Power-down

To prevent audio transients at power-down the DC-blocking capacitors must fully discharge before turning off the power. In order to do this MCLK should be stopped for a period of about 250 ms for a 3.3 µF cap connected to VQ (420 ms for a 10 µF cap connected to VQ) before removing power. During this time voltage on VQ and the audio outputs discharge gradually to GND. If power is removed before this time period has passed a transient will occur when the VA supply drops below that of VQ. There is no minimum time for a power cycle, power may be re-applied at any time.

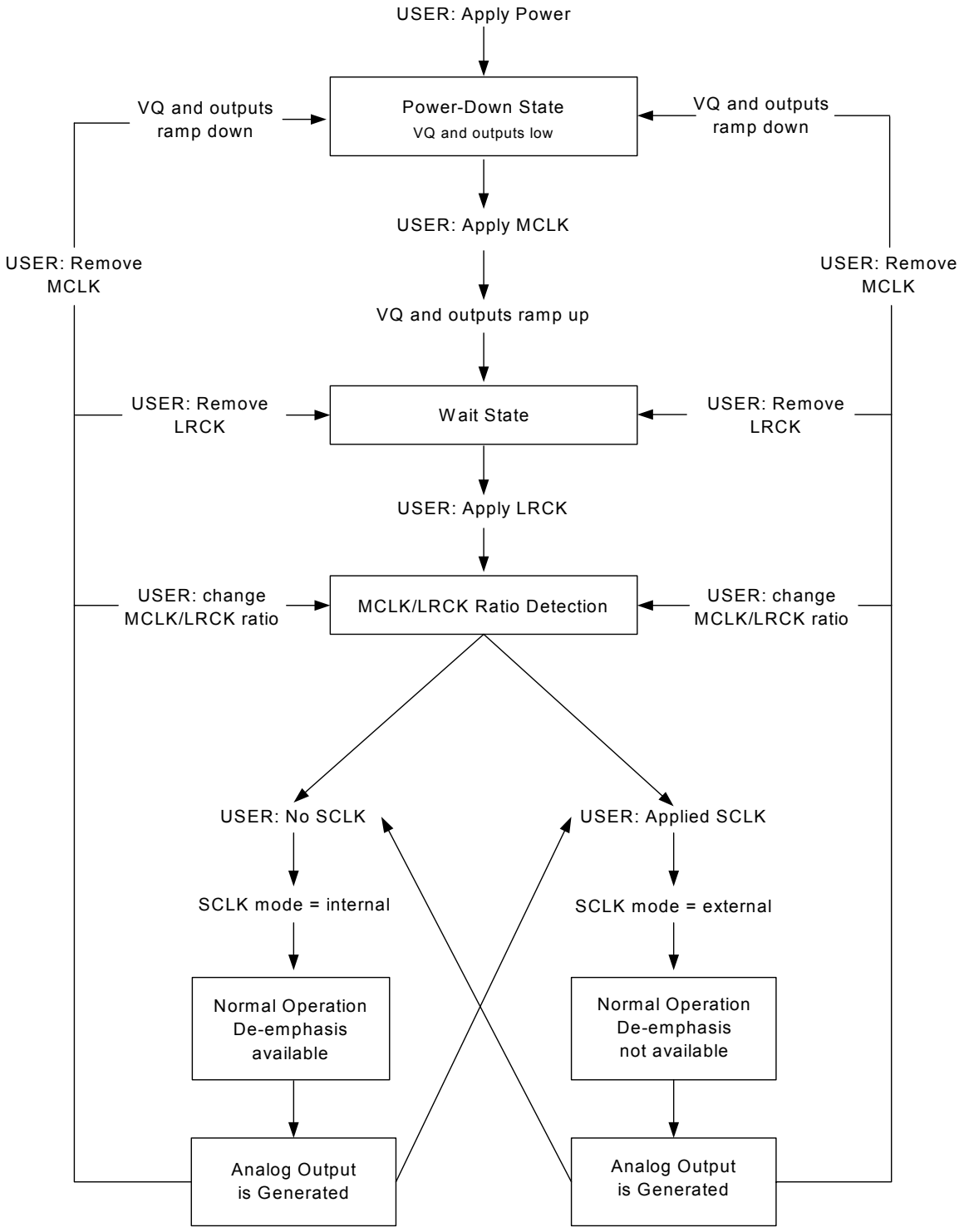


Figure 12. CS4344/5/6/8 Initialization and Power-Down Sequence

When changing clock ratio or sample rate it is recommended that zero data (or near zero data) be present on SDIN for at least 10 LRCK samples before the change is made. During the clocking change the DAC outputs will always be in a zero data state. If no zero audio is present at the time of switching, a slight click or pop may be heard as the DAC output automatically goes to it's zero data state.

4.6 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4344 family requires careful attention to power supply and grounding arrangements to optimize performance. Figure 6 shows the recommended power arrangement with VA connected to a clean +3.3 V or +5 V supply. For best performance, decoupling and filter capacitors should be located as close to the device package as possible with the smallest capacitors closest.

4.7 Analog Output and Filtering

The analog filter present in the CS4344 family is a switched-capacitor filter followed by a continuous time low pass filter. Its response, combined with that of the digital interpolator, is given in Figures 13 - 20. The recommended external analog circuitry is shown in the "Typical Connection Diagram" on page 11.

5.PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

6.ORDER INFORMATION:

Model	Temperature	Package	Serial Interface
CS4344-CZZ	-10 to +70 °C	10-pin Plastic TSSOP - Lead-Free	16 to 24-bit, I2S
CS4344-DZZ	-40 to +85 °C	10-pin Plastic TSSOP - Lead-Free	16 to 24-bit, I2S
CS4345-CZZ	-10 to +70 °C	10-pin Plastic TSSOP - Lead-Free	16 to 24-bit, left justified
CS4346-CZZ	-10 to +70 °C	10-pin Plastic TSSOP - Lead-Free	24-bit, right justified
CS4348-CZZ	-10 to +70 °C	10-pin Plastic TSSOP - Lead-Free	16-bit, right justified

7.FUNCTIONAL COMPATIBILITY

CS4334-KS ⇒ CS4344-CZZ

CS4335-KS ⇒ CS4345-CZZ

CS4336-KS ⇒ CS4346-CZZ

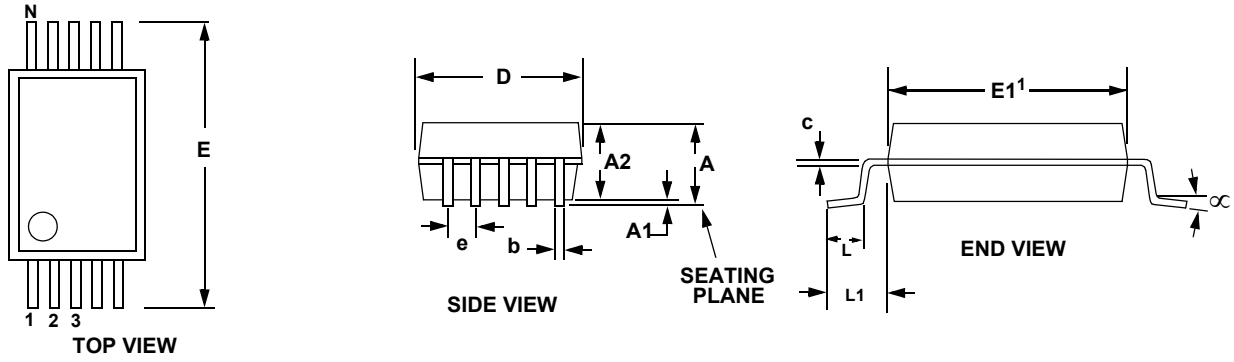
CS4338-KS ⇒ CS4348-CZZ

CS4334-BS ⇒ CS4344-DZZ

CS4334-DS ⇒ CS4344-DZZ

8.PACKAGE DIMENSIONS

10LD TSSOP (3 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**	
A	--	--	0.0433	--	--	1.10	
A1	0	--	0.0059	0	--	0.15	
A2	0.0295	--	0.0374	0.75	--	0.95	
b	0.0059	--	0.0118	0.15	--	0.30	4, 5
c	0.0031	--	0.0091	0.08	--	0.23	
D	--	0.1181 BSC	--	--	3.00 BSC	--	2
E	--	0.1929 BSC	--	--	4.90 BSC	--	
E1	--	0.1181 BSC	--	--	3.00 BSC	--	3
e	--	0.0197 BSC	--	--	0.50 BSC	--	
L	0.0157	0.0236	0.0315	0.40	0.60	0.80	
L1	--	0.0374 REF	--	--	0.95 REF	--	
∝	0°	--	8°	0°	--	8°	

Controlling Dimension is Millimeters

Notes:
1. Reference document: JEDEC MO-187
2. D does not include mold flash or protrusions which is 0.15 mm max. per side.
3. E1 does not include inter-lead flash or protrusions which is 0.15 mm max per side.
4. Dimension b does not include a total allowable dambar protrusion of 0.08 mm max.
5. Exceptions to JEDEC dimension.

9.APPENDIX

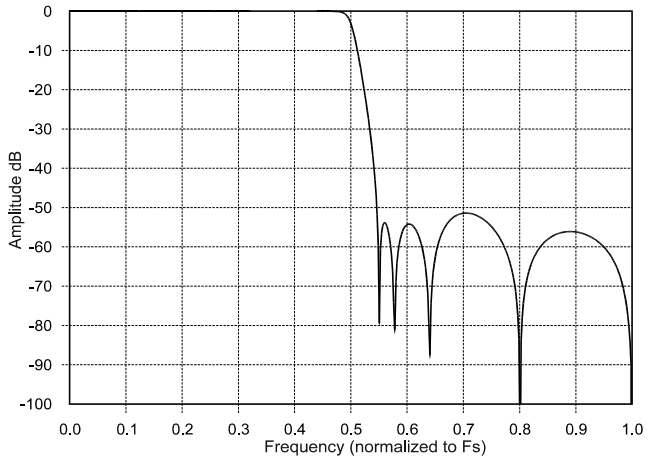


Figure 13. Single Speed Stopband Rejection

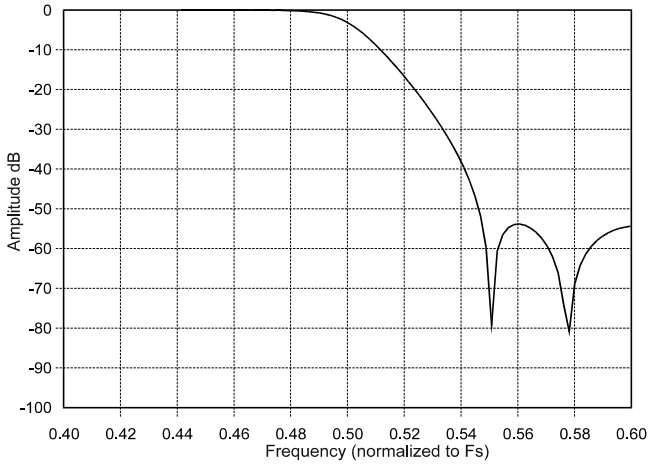


Figure 14. Single Speed Transition Band

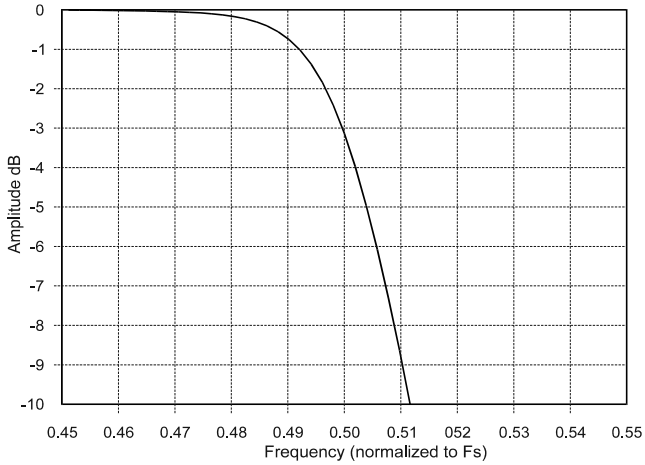


Figure 15. Single Speed Transition Band

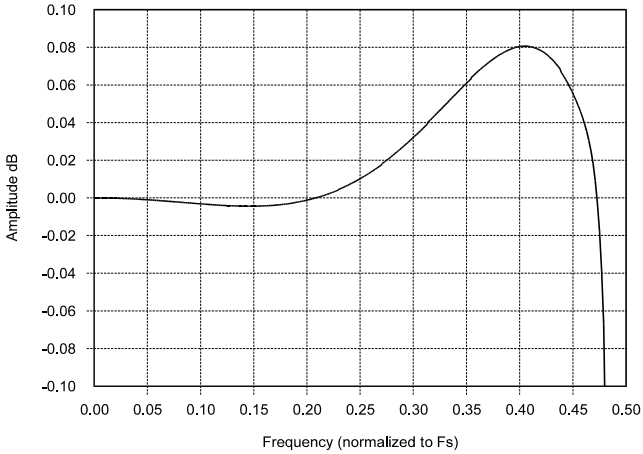


Figure 16. Single Speed Passband Ripple

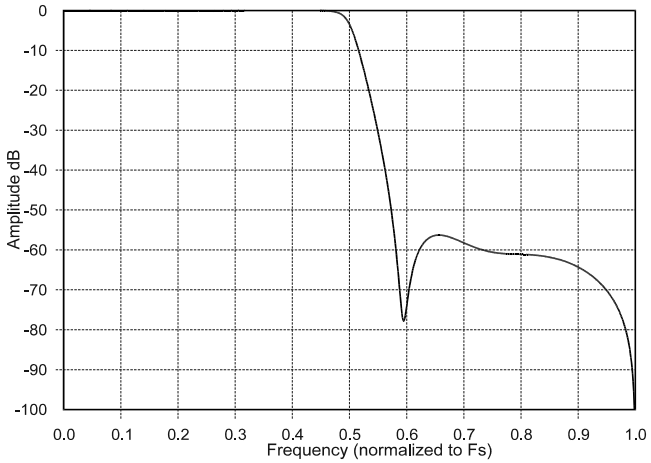


Figure 17. Double Speed Stopband Rejection

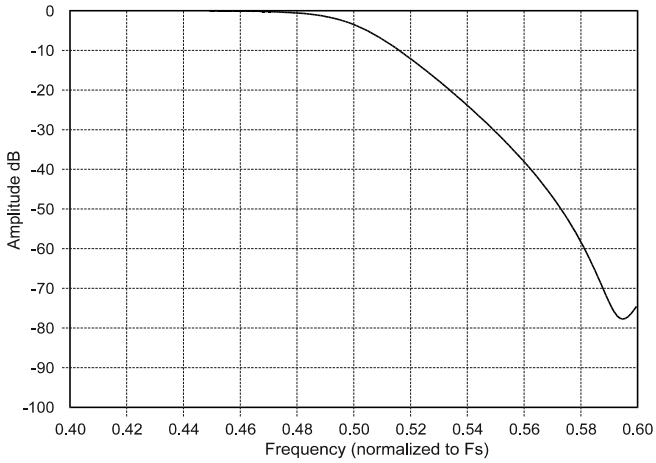


Figure 18. Double Speed Transition Band

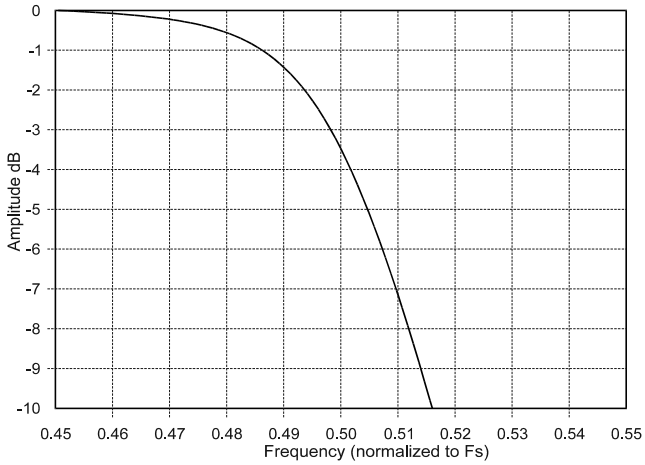


Figure 19. Double Speed Transition Band

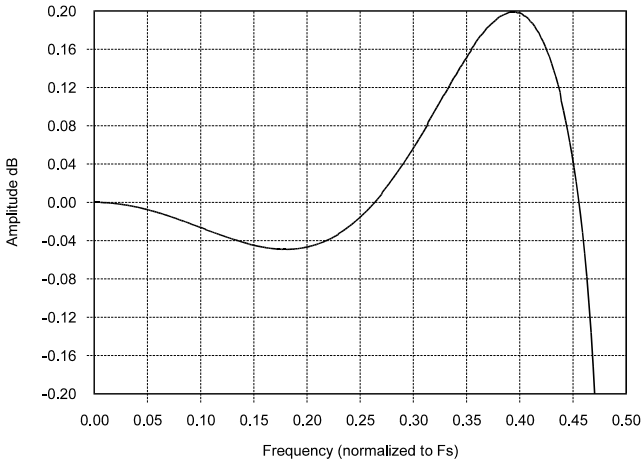


Figure 20. Double Speed Passband Ripple