EF9340 • EF9341

ADVANCE INFORMATION

SEMI-GRAPHIC CRT DISPLAY PROCESSOR

Two 40 pin circuits EF9340 (VIN) and EF9341 (GEN) and 16 K bits of standard static RAM are enough to build a complete semi-graphic display unit :

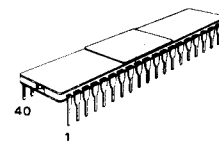
- Simple, low cost yet flexible, asynchronous interface with microprocessor
- Display of 25 or 21 rows of 40 characters
- On chip (GEN) 128 alphanumeric and 128 semi graphic character generator
- Easy extension up to 2 additional sets of 96 characters each
- One colour, double height, double width, negative (alphanumeric) or two colours (semi-graphic) and blinking are provided as parallel attributes
- Conceal, boxing, underlining as serial attributes
- Programmable roll up, roll down, zoom, and cursor display
- 50 Hz/60 Hz operation
- On chip R, G, B shift registers (VIN)
- Half dot frequency (3.5 MHz) clock input
- Vertical synchronization input
- Single +5 Volt supply
- TTL/MOS compatible I/O

MOS

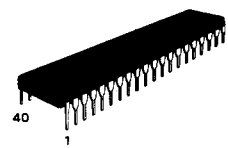
(N-CHANNEL, SILICON GATE)

SEMI-GRAPHIC CRT DISPLAY PROCESSOR

CASE CB-182



C SUFFIX
CERAMIC PACKAGE



P SUFFIX
PLASTIC PACKAGE

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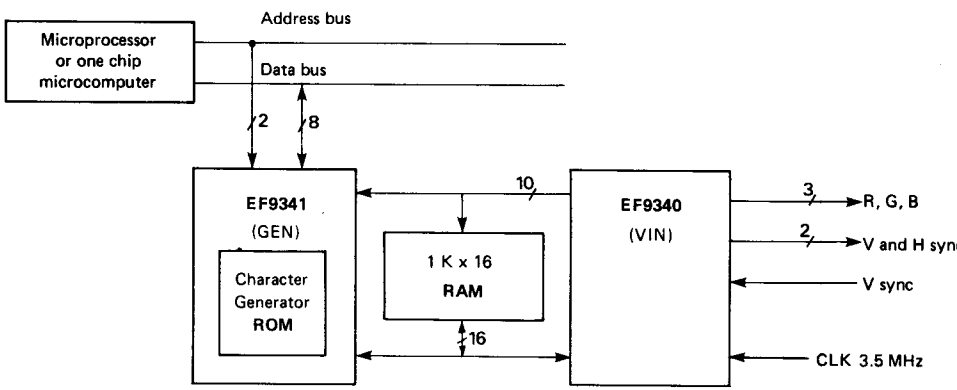
FIGURE 1 – TYPICAL DISPLAY UNIT



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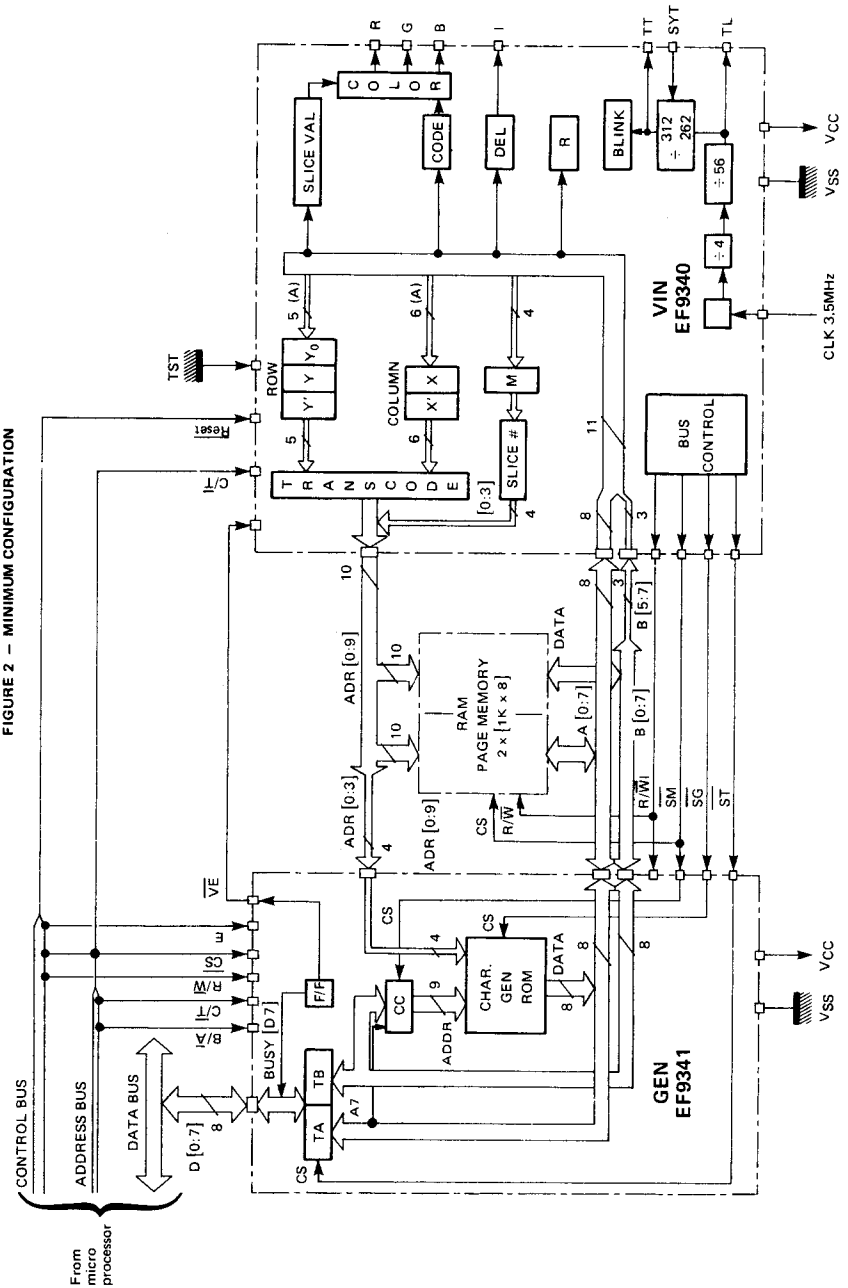


FIGURE 2 – MINIMUM CONFIGURATION

The display unit is organized around a 16 bit internal bus (fig.2) controlled by VIN. GEN contains a character generator and two 8 bit registers – TA and TB – which provide a buffered interface with a general purpose 8 bit bus. The display unit receives data and commands through these registers which perform as a mail box. VIN contains a Timing Generator, a Display Automaton and an Access Automaton.

TIMING GENERATOR

It divides the clock input at half the dot frequency (3.5 MHz) by 4 to get the window frequency. This frequency is divided to get the line frequency and the frame frequency. The size of a character being programmable, it occupies 1, 2 or 4 windows on the screen. Each window is 10 TV lines high and 8 dots wide. Timing Generator gives control over the bus to the display automaton for 40 window periods per line and 250 (or 210) lines per frame. Access automaton has control over the internal bus for the remaining time.

DISPLAY AUTOMATON

During each displayable window period ($\simeq$ 1.1 μs), the display automaton controls two read cycles on the internal bus.

On the first cycle, a window code (16 bits) is read from the page memory (table 1). Attribute field (7 bits) and character type field (4 bits) are latched in VIN.
Character code field (9 bits) is latched in CC registers.
Then window address register is incremented.
On the second cycle, address bus gives the slice number (0 – 9) to the character generator and a slice of 8 dots is read. Then Display Automaton delivers R, G, B signals and I (boxing command).
A set of 128 alphanumeric characters and a set of 128 standard semi-graphic characters are provided by GEN. Further extension is easily done using standard (1k x 8) ROM or RAM components (fig. 8).

ACCESS AUTOMATON

When TA register and then TB register of the mail box are written from the main bus with $C/\overline{T} = 1$, Access Automaton knows that a command is pending.
As soon as it gets control over the internal bus, it reads the mail box and gets the command.
A command may be :

- A cursor modification
- A display mode (ON/OFF, Roll up, etc...)
- A data transfer mode (Read/Write Page Memory, Read/Write Character Generator)

Data transfers are executed through the mail box addressed with $C/\overline{T} = 0$ and according to the current Data Transfer Mode.

The busy flip-flop gives the status of the mail box. It can be read in the MSB of the TA byte addressed with $C/\overline{T} = 1$.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} *	−0.3 to+ 7.0	Vdc
Input Voltage	V_{in} *	−0.3 to 7 V	Vdc
Operating Temperature Range	T_A	0 to+ 70	°C
Storage Temperature Range	T_{stg}	−55 to+ 150	°C
Max Power Dissipation	P_{DM}	0.75	W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

* With respect to V_{SS}

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 5 %, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{CC}	4.75	5.0	5.25	Vdc
Input Low Voltage		V_{IL}	−0.3	–	0.8	Vdc
Input High Voltage (except SYT and CLK)		V_{IH}	2.2	–	V_{CC}	Vdc
Input Hith Voltage SYT and CLK		V_{IH}	3	–	V_{CC}	Vdc
Three State and Input Leakage current (except CLK)		I_{in}	–	–	10	µA
CLK input current	V_{IN} = 0.4 V	I_{IL}	–	–	− 2	mA
Output High Voltage I_{load} = −150 µA I_{load} = −500 µA	R, G, B, I Other outputs	V_{OH}	2.4	–	–	V
Output Low Voltage I_{load} = 0.4 mA I_{load} = 1.6 mA	R, G, B, I Other outputs	V_{OL}	–	–	0.4	V
Power Dissipation VIN GEN		P_D	–	200 250	–	mW
Input Capacitance		C_{in}	–	–	10	pF

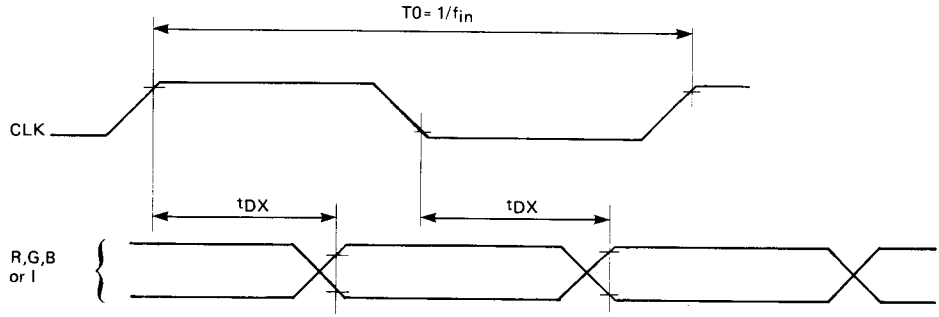
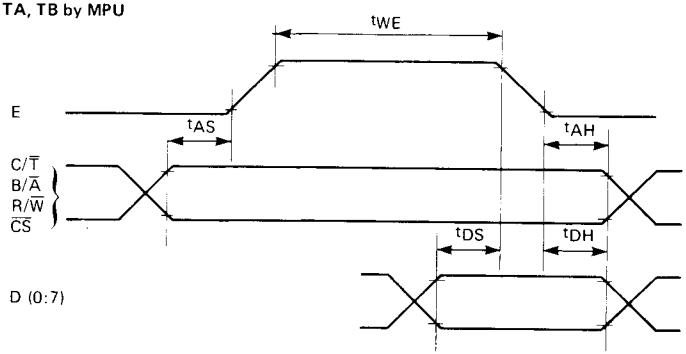


FIGURE 3 – R, G, B and I TIMING (VIN)

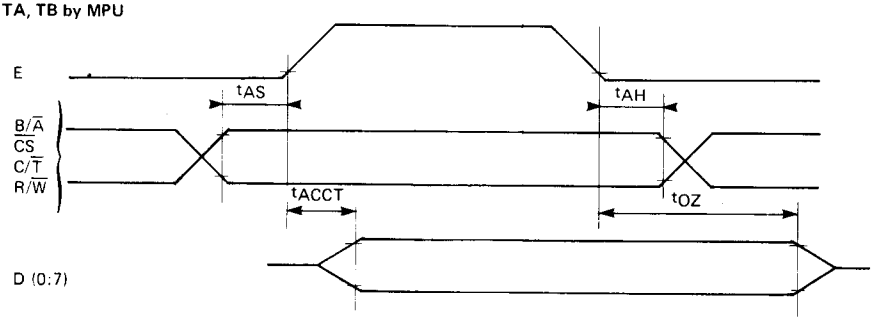
CLOCK R, G, B AND I TIMING CHARACTERISTICS (V_{CC} = 5.0 ± 5 %, V_{SS} 0, T_A = 0 – 70° C, CL = 70 pF)

Characteristic	Symbol	Min	Typ	Max	Unit
Clock frequency	f_{in}	3.4	–	3.6	MHz
R, G, B or I delay time from clock edge	t_{DX}	–	–	130	ns
R, G, B and I relative delay		–	5	–	ns

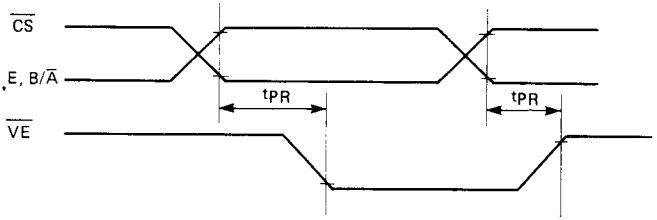
Write TA, TB by MPU



Read TA, TB by MPU



VE Output



Reference level : Input 0.8 and 2.2 V
Output 0.4 and 2.4 V

FIGURE 4 – PROCESSOR BUS TIMING CHART (GEN)

PROCESSOR BUS TIMING CHARACTERISTICS

(V_{CC} = 5.0 V ± 5 %, V_{SS} = 0, T_A = 0 to 70° C – C_L = 100 pF on all outputs

Characteristic	Symbol	Min	Typ	Max	Unit
Enable pulse duration	t_{WE}	200	—	—	ns
Address setup time	t_{AS}	40	—	—	ns
Address hold time	t_{AH}	0	—	—	ns
Data setup time	t_{DS}	140	—	—	ns
Data hold time	t_{DH}	10	—	—	ns
T_A, T_B access time	t_{ACCT}	—	—	200	ns
Data off time	t_{OZ}	0	—	—	ns
$\overline{VE}$ delay time ($\overline{CS}$ = 0 ; E = B/$\overline{A}$ = 1)	t_{PR}	—	—	140	ns

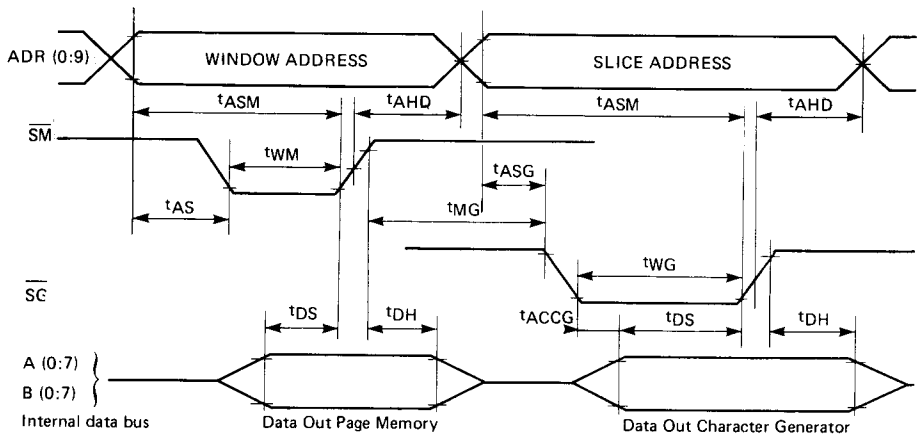


FIGURE 5 – INTERNAL BUS - DISPLAY READ CYCLES – TIMING CHART (R/$\overline{W}$I = 1)

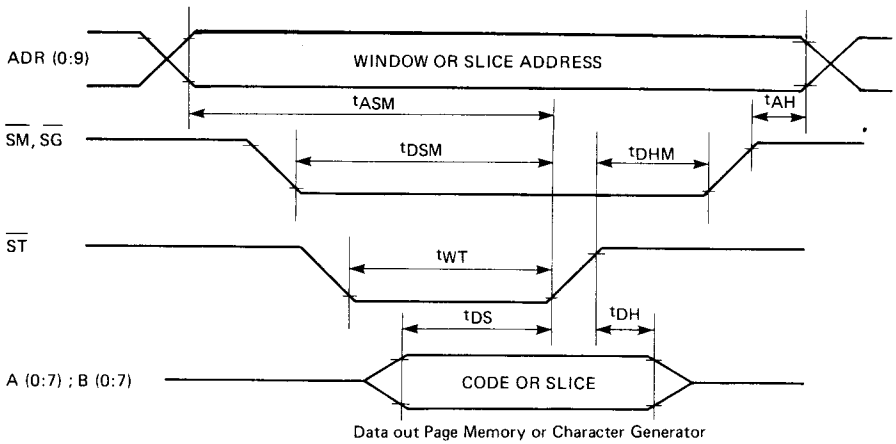


FIGURE 6 – INTERNAL BUS – FROM PAGE MEMORY OR CHARACTER GENERATOR TO MAIL BOX TRANSFER CYCLES (R/$\overline{W}$I = 1)

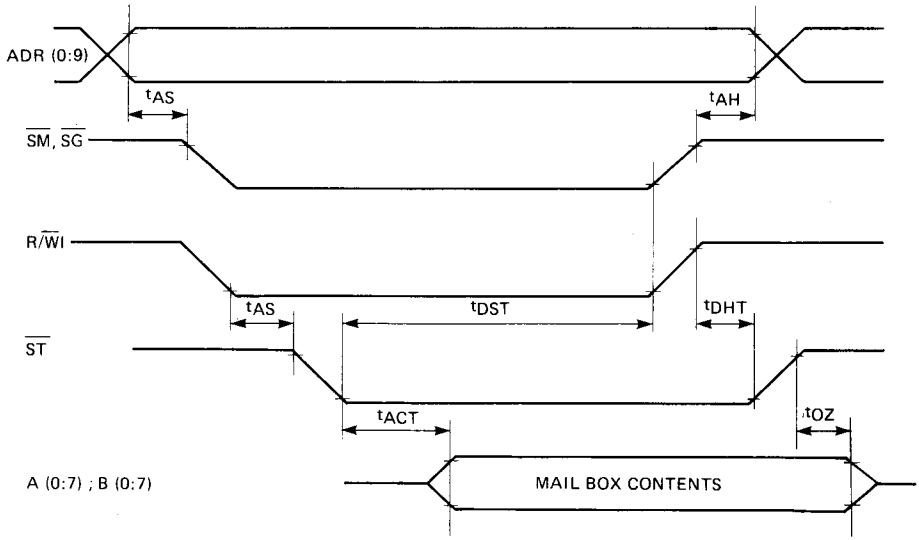


FIGURE 7 – INTERNAL BUS – FROM MAIL BOX TO PAGE MEMORY OR CHARACTER GENERATOR OR VIN TRANSFER CYCLES

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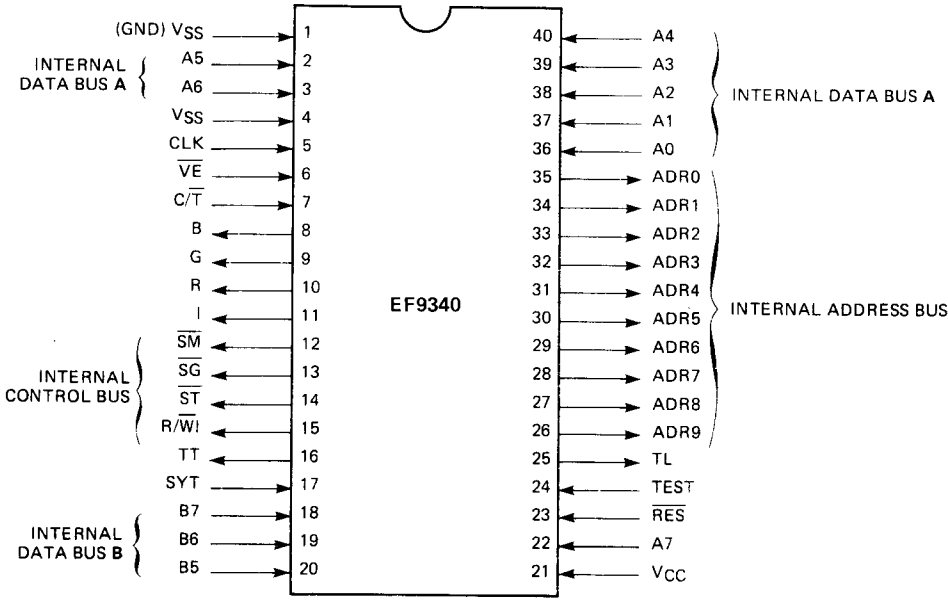
INTERNAL BUS TIMING CHARACTERISTICS

(V_{CC} = 5.0 V ± 5 %, V_{SS} = 0, T_A = 0 to 70° C, C_L = 100 pF on all outputs, f_{in} = 3.5 MHz)

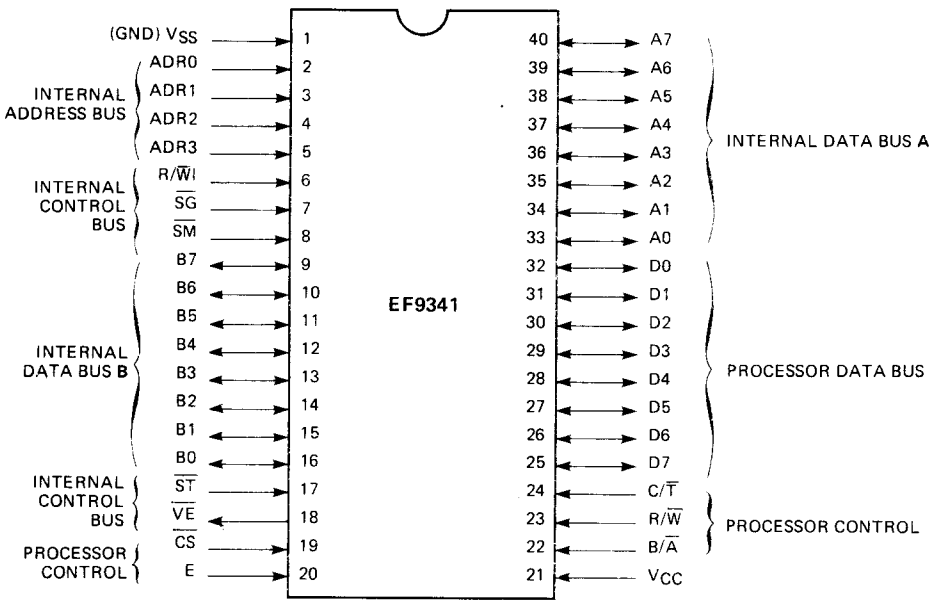
Characteristic	Symbol	Min	Typ	Max	Unit
Address setup time	t_{ASM}	460	–	–	ns
Address hold time	t_{AH}	0	–	–	ns
Strobe duration (display cycles)	t_{WM}	300	–	–	ns
	t_{WG}	380	–	–	ns
Address hold time (display cycles) (Ref. 1.5 V for $\overline{SM}$, $\overline{SG}$, ADR)	t_{AHD}	0	0	–	ns
Address to strobe	t_{ASG}	40	–	–	ns
Data setup time	t_{DS}	140	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Precharge Character Generator (in GEN)	t_{MG}	60	–	–	ns
Access to Character Generator (in GEN)	t_{ACCG}	–	–	240	ns
From $\overline{SM}$ or $\overline{SG}$ to $\overline{ST}$	t_{DSM}	400	–	–	ns
$\overline{SM}$ or $\overline{SG}$ hold time	t_{DHM}	0	–	–	ns
Write Mail Box strobe duration	t_{WT}	250	–	–	ns
Write setup time	t_{AS}	40	–	–	ns
From $\overline{ST}$ to $\overline{SM}$ or $\overline{SG}$	t_{DST}	350	–	–	ns
Access time to Mail Box (in GEN)	t_{ACT}	–	–	200	ns
$\overline{ST}$ hold time	t_{DHT}	60	–	–	ns
Mail Box off time	t_{OZ}	0	–	270	ns

Reference level : 0.8 V and 2 V on any input
0.4 V and 2.4 V on any output
} unless otherwise specified.

VIN PIN ASSIGNMENT



GEN PIN ASSIGNMENT



VIN SIGNAL DESCRIPTION

VIN controls several types of data transfers on the internal bus.

- From the mail box to VIN
- From the Page Memory to VIN
- From the Character Generator to VIN
- Between Mail Box and Page Memory
- Between Mail Box and Character Generator

VIN delivers R, G, B and synchronization signals to the CRT.

INTERNAL BUS INTERFACE

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
A(0:7) B(5:7)	I I	36, 37 38, 39 40, 2 3, 22 20-18	Internal data bus	VIN gets only eleven inputs out of the sixteen lines of the bidirectional internal data bus.
ADR(0:9)	O	35-26	Internal address bus	These ten TTL compatible outputs multiplex the page memory address with the slice number – ADR(0:3) – and the selection of an external character generator – ADR4.
R/$\overline{W}$I	O	15	Read/Write on Internal Bus	This TTL compatible output determines whether the page memory or the character generator gets read or written. A write is active low ("0").
$\overline{SM}$	O	12	Memory strobe	This TTL compatible output, when active, selects the page memory as source (R/$\overline{W}$I high) or destination (R/$\overline{W}$I low) on the internal bus. When $\overline{SM}$ goes active (low), ADR(0:9) and R/$\overline{W}$I are stable.
$\overline{SG}$	O	13	Character generator strobe	This TTL compatible output, when active, selects a character generator as source (R/$\overline{W}$I high) or destination (R/$\overline{W}$I low) on the internal bus. When $\overline{SG}$ goes active (low), ADR(0:4) and R/$\overline{W}$I are stable. $\overline{SM}$ and $\overline{SG}$ are never active at the same time.
$\overline{ST}$	O	14	Mail box strobe	This TTL compatible output, when active, selects the mail box as source (R/$\overline{W}$I low) or destination (R/$\overline{W}$I high) on the internal bus. $\overline{ST}$ may be active (low) at the same time as $\overline{SM}$ or $\overline{SG}$.

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VIDEO INTERFACE

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
R G B	O	10 9 8	Red Green Blue	These three TTL/LS compatible outputs deliver the video signal. They are low during the vertical and horizontal blanking intervals.
TT	O	16	Vertical synchronization	This TTL compatible output is active (low) for two lines each field period. The field period is programmable at 262 lines (60 Hz) or 312 lines (50 Hz).
TL	O	25	Horizontal synchronization	This TTL compatible output is at line frequency. It can be programmed active low for 4 window periods (for composite signal generation) or active high for 16 window periods (to directly drive a monitor).
I	O	11	Boxing command	This TTL/LS compatible output is active high. I allows to insert R,G,B in an external video signal for captioning purposes, for example.
SYT	I	17	Vertical synchronization input	This high impedance, high noise margin input is internally sampled and memorized on the 12 th window period of each line. When the memorized signal goes from high to low, the line count is reset at the end of the present line. This input allows to vertically synchronize VIN on an external composite or AC line signal. This input should be grounded if not used.

OTHER PINS

V_{SS}	I	4		This input has to be grounded.
CLK	I	5	Clock input	External TTL clock input. (nominal value : 3.5 MHz)
$\overline{VE}$	I	6	VIN select	This TTL/MOS high impedance input must be wired to the corresponding GEN output. This input is active (low) each time the TB register of the mail box is accessed by the microprocessor.
$C/\overline{T}$	I	7	Command or transfer select	This TTL/MOS high impedance input determines whether a command ($C/\overline{T}$ high) or data ($C/\overline{T}$ low) is accessed by the processor in the mail box. $C/\overline{T}$ is latched on the falling edge of $\overline{VE}$ and the request is memorized.
$\overline{RES}$	I	23	Restart	When this TTL/MOS high impedance input goes low, the TL output goes high and remains in this state until the display mode register is loaded.
TST	I	24	Test	This pin must be grounded for normal operation.
V_{CC}	S	21	Power supply	+5 V
GND	S	1	Power supply	Ground.

GEN SIGNAL DESCRIPTION

GEN takes place in the video display unit between the internal 16 bit bus controlled by VIN and a general purpose 8 bit bus controlled by a processor. GEN contains :

- A character generator with 128 alphanumeric characters and 128 semigraphic characters.
- Two 8 bit registers - TA and TB - which perform as a mail box between the two buses.

PROCESSOR INTERFACE

GEN interfaces to a processor bus on the bidirectional data bus D (0:7) using $\overline{CS}$, B/$\overline{A}$, C/$\overline{T}$, $\overline{E}$ and R/$\overline{W}$ as control signals.

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
D(0:7)	I/O	32-25	Data bus	The bidirectional data lines D(0:7) allow command and data transfers between the GEN internal mail box and the processor. Data bus output drivers are 3-state buffers which remain in the high impedance state except when the processor performs a display unit read operation. A high level on a data pin is a logical "1".
E	I	20	Enable	The enable signal is a high impedance TTL/MOS compatible input which enables the data bus input/output buffers and clocks data to and from the mail box. This signal is usually derived from the processor clock.
$\overline{CS}$	I	19	Chip select	The $\overline{CS}$ line is a high impedance TTL/MOS compatible input which selects the display unit, when low, to read or write the internal mail box.
R/$\overline{W}$	I	23	Read/Write	This high impedance TTL/MOS compatible input determines whether the internal mail box gets written or read. A write is active low ("0").
B/$\overline{A}$	I	22	Register TA or TB select	This high impedance TTL/MOS compatible input selects either the TA register (B/$\overline{A}$ = 0) or the TB register (B/$\overline{A}$ = 1) of the mail box.
C/$\overline{T}$	I	24	Command or data transfer select	This high impedance TTL/MOS compatible input defines the contents of the mail box either as a command ($\overline{CT}$ = 1) or as a data transfer (C/$\overline{T}$ = 0). The C/$\overline{T}$ input of GEN and the C/$\overline{T}$ input of VIN must be wired together for correct operations.

VIN INTERFACE

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
$\overline{VE}$	O	18	VIN select	This TTL compatible output must be wired to the corresponding VIN input. This signal goes active (low) when the TB register is accessed by the processor.
A(0:7) B(0:7)	I/O	33-40 16-9	Internal data bus	These 16 bidirectional data lines allow data transfers between GEN, VIN and memory.
R/$\overline{WI}$ $\overline{SM}$ $\overline{SG}$ $\overline{ST}$	I	6 7 8 17	Control signals from VIN	These inputs must be wired to the corresponding VIN outputs.
ADR(0:3)	I	2-5	Slice address	These four inputs must be wired to the corresponding four outputs of VIN. When $\overline{SG}$ is active, they are stable and determine the BCD address of a character slice in the character generator.
V_{CC}	S	21	Power supply	+5 V
V_{SS}	S	1	Power supply	Ground.

MICROPROCESSOR INTERFACE

The complete display unit is accessed by the processor through 4 addresses when $\overline{CS}$ is low and E is high.

ADDRESS		ADDRESSED REGISTER		
C/$\overline{T}$	B/$\overline{A}$	R/$\overline{W}$ = 1 Read	R/$\overline{W}$ = 0 Write	Comments
0	0	TA	TA	A 16 bit data is read or written from/into the mail box
0	1	TB (1)	TB (1)	
1	0	Busy (2)	TA	A 16 bit command is written in the mail box or the busy flip-flop is read (4).
1	1	– (3)	TB (1)	

(1) Sets the busy flip-flop and activates $\overline{VE}$.
(2) Busy is read MSB on the MPU bus (D7). Other bits are don't care.
(3) Illegal operation.
(4) A valid command should be loaded at least 64 µs after power on or RESET without testing busy to reset it.

COMMAND – (C/$\overline{T}$ = 1)

When the mail box is written with a command, the busy flip-flop is set and GEN activates $\overline{VE}$. A Read command request ($\overline{VE}$ low and C/$\overline{T}$ high) is memorized by the access automaton of VIN. As soon as the access automaton takes control over the internal bus, it reads the command in the mail box ; this resets the busy flip-flop. 11 bits only out of the 16 bits of the command are read :

B (5:7) give the address of the register or the operation to perform.
A (0:7) give a parameter.
4 registers may be modified by a command :
the Cursor Register C, the Origin Register Y0, the Access Mode Register M and the Display and Timing Mode Register R.

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COMMAND CODE																NAME	OPERATION
B7	B6	B5	B4	B3	B2	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0		
0	0	0									K (0 : 4)					Begin Row	X (0 : 5) ← 0 Y (0 : 4) ← K (0 : 4)
0	0	1									K (0 : 4)					Load Y	Y (0 : 4) ← K (0 : 4)
0	1	0									K (0 : 5)					Load X	X (0 : 5) ← K (0 : 5)
0	1	1														INC C	C ← C+ 1
1	0	0						K (0 : 7)								Load M	M (0 : 7) ← K (0 : 7)
1	0	1						K (0 : 7)								Load R	R (0 : 7) ← K (0 : 7)
1	1	0									K (0 : 5)					Load Y0	Y0 (0 : 5) ← K (0 : 5)
1	1	1															Not interpreted

The first 4 commands allow cursor handling :

- Initialization at the beginning of a row
- Vertical movement
- Horizontal movement
- Incrementation

DISPLAY AND TIMING MODE REGISTER R(0:7)

R(0:7) is an 8-bit register.
This register is loaded through a LOAD R command.
The 6 bits R(0:4) and R7 define the display modes.
The 2 bits R(5:6) define the timing modes.

Bit 0 : When R0 = 0, the display automaton is disabled. R, G, B and I outputs stay low.
When R0 = 1, the display automaton is enabled. When the display automaton is disabled, loading the R register with R0 = 1 may alter the page memory contents if not done during the vertical blanking intervals.

Bit 1 : When R1 = 0, the boxing attribute is disabled. I stays high, during the display periods.
When R1 = 1, the boxing attribute is enabled. R, G, B and I outputs are low out of the boxing zone. I is high in the boxing zone.
The CRT and VIN are supposed to be synchronized by a composite external video signal. I switches the boxed windows on the screen.

Bit 2 : When R2 = 0, the conceal attribute is disabled.
When R2 = 1, the conceal attribute is enabled.

Bit 3 : When R3 = 1, the service row is displayed at the top of the screen.
When R3 = 0, it is concealed.

R0	R1	Condition	I	R G B
0	–	–	0	Black
1	0	–	–	–
1	1	In boxing zone	1	–
1	1	Outside boxing zone	0	Black

Bit 4 : When R4 = 1, the cursor position is displayed. The character in the window alternates between normal and reverse video at blinking frequency. When blinking is disabled (R7 = 0), it is permanently reversed.
When R4 = 0, the cursor position is not displayed.

Bit 5 : When R5 = 0, TL is active low during 4 window periods.
When R5 = 1, TL is active high during 16 window periods.

Bit 6 : When R6 = 0, TT period is 262 lines (60 Hz).
When R6 = 1, TT period is 312 lines (≃ 50 Hz).

Bit 7 : When R7 = 0, blinking is disabled.
When R7 = 1, blinking is enabled.

CURSOR REGISTER C

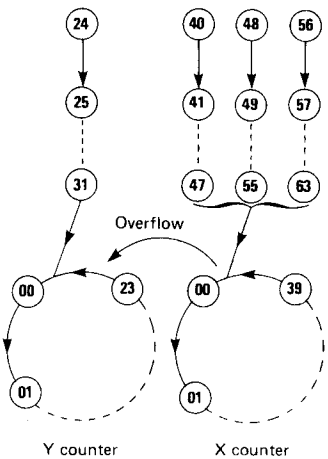
The cursor register C points to the page memory. It is subdivided into two counters X and Y :

X(0:5) points to a column. The decimal value of X comes from 00 to 39 when columns are addressed from left to right.

Y(0:4) points to a row. The decimal address of the service row is 31. The other rows are addressed from 00 to 23.

When the cursor is incremented, X is incremented. When X overflows, Y is automatically incremented as shown in the state diagram below.

Nota : the 11 bits of X and Y are transcoded to get a 10 bit binary address in the page memory.



STATE DIAGRAM

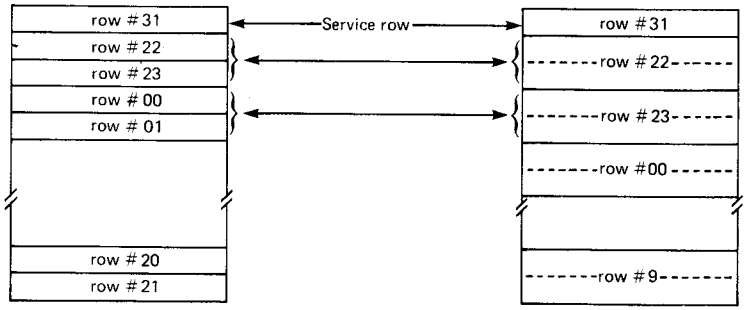
Y_4 Y_3		ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
00	X5 = 0	Y4	Y3	Y2	Y1	Y0	X4	X3	X2	X1	X0
10											
01	X5 = 1	1	1	Y2	Y1	Y0	Y4	Y3	X2	X1	X0
11	–	1	1	X5	X4	X3	1	1	X2	X1	X0

ORIGIN REGISTER Y0(0:5)

Y0(0:5) is a 6 bit register.
This register is loaded through a LOAD Y0 command.

Bit 0 to 4 : Y0 (0:4) give the number of the first row displayed directly after the service row.
A circular roll up or roll down may be commanded by incrementing or decrementing modulo 24 the value of Y0(0:4).

Bit 5 : Y0(5) = 1 sets the zoom mode : the first 12 rows are displayed in double height. If a character was already displayed in double height, it is now in quadruple height. The service row is always displayed in single height.
Y0(5) = 0 resets the zoom mode.



No zoom mode
First displayed row = 22

Zoom mode
First displayed row = 22

5

ACCESS MODE REGISTER M(0:7)

M(0:7) is an 8 bit register.
This register is loaded through a LOAD M command.
Subsequent data transfers are executed according to the current access mode (see "Data transfer".)

ACCESS MODE REG.								ACCESS MODE	SUBSEQUENT DATA TRANSFER
M7	M6	M5	M4	M3	M2	M1	M0		
0	0	0						Write	MP (C) ← T ; C ← C+1
0	0	1						Read	T ← MP (C) ; C ← C+1
0	1	0						Write without INC	MP (C) ← T
0	1	1						Read without INC	T ← MP (C)
1	0	0			N T			Write slice	GC (MP(C), NT) ← T ; NT ← NT+1
1	0	1			N T			Read slice	T ← GC (MP(C), NT) ; NT ← NT+1
1	1							Illegal	

NT : Slice number T : Mail Box C : Cursor MP : Page Memory GC : Character Generator

DATA TRANSFERS ($C/\overline{T} = 0$)

When the mail box is written or read with $C/\overline{T} = 0$, the busy flip flop is set and GEN activates $\overline{VE}$. A data transfer request is memorized by the access automaton of VIN. As soon as the access automaton takes control over the internal bus, it executes the request according to the contents of the M register.
M(0 : 3) is a modulo 10 counter referred to as NT (slice number)
M(5:7) defines an access mode (see table 3).

WRITE

It is the most commonly used data transfer : the contents of the mail box is written into the page memory location addressed by the cursor. Then the cursor is incremented.

READ

The page memory location addressed by the cursor is written into the mail box.
Then the cursor is incremented.
These two modes give sequential access to the page memory.

WRITE, READ WITHOUT INCREMENTATION

Same as above but the cursor is not incremented.

WRITE SLICE

This mode is used to load a RAM used as extended character generator.

The execution takes two cycles :

- A read without incrementation cycle is performed on the page memory. The character code is latched in the extended character code register. A7, B(5:7) are latched in VIN.
- The contents of the TA register of the mail box is written into the character generator. The address is given by the extended character code register and the contents of NT, which is sent on ADR(0:3). The extension condition B7 ∧ (B5 ∨ B6) is sent on ADR4. Then NT is incremented modulo 10.

READ SLICE

This mode is used to read a slice in any character generator.

The execution takes 2 cycles :

- The first cycle is identical to the first cycle of WRITE SLICE.
- On the second cycle, a character 8-bit slice is written into the mail box.

NOTA :

1. In READ or WRITE SLICE mode, the character code address is indirectly given by the cursor. The page memory must have been previously initialized.
2. **The first data transfer following the loading of any READ mode into the M register is triggered by a mail box read by the microprocessor. Consequently these first data are invalid.**
3. Any access of the mail box by the internal bus resets the busy flip flop. If the display is disabled, then the busy flip flop remains set for a maximum of 4 window periods, otherwise a maximum of 44 window periods.

TIMING GENERATOR AND INTERNAL BUS CYCLES

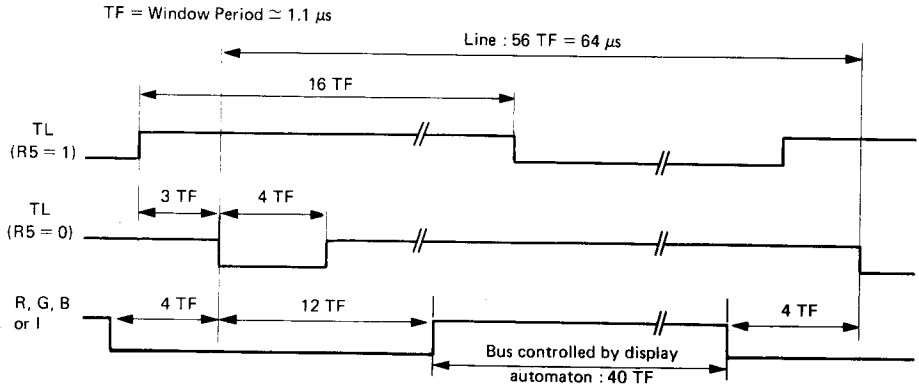
LINES AND FRAME

The input clock is at half the dot frequency (3.5 MHz). 8 dot periods (4 clock periods) make a window period. 56 window periods make a line period (≃ 64 μs).

TL output is at line frequency. The duration of TL is programmable through R5 (Display and Timing Generator Mode Register).

With R5 = 0, TL output is at "0" (low level) for 4 window periods (≃ 4.5 μs).

With R5 = 1 (Monitor Mode), TL output is at "1" (high level) for 16 window periods (18.3 μs). In this mode, TL may directly drive the horizontal deflection circuitry. To protect the Darlington from overloading, the TL output is set to "1" when a low level is applied on $\overline{RES}$ and remains in this state until reception of a LOAD R command.



262 line periods (if R6 = 0) or 312 line periods (if R6 = 1) make a frame period. The TT output is at frame period (60 Hz/50 Hz) and is low during 2 lines. SYT input resets the line count inside the frame : this input is triggered, then sampled when the 12th window of each line occurs. When the sample transits from 1 to 0, the line count will be reset on the next TL.

TIME SHARING OF THE BUS

When the display is enabled (R0 = 1), the timing generator gives control over the bus to the display automaton from the 40th line after TT to the 290th (if R6 = 1) or from the 32nd line to the 242nd (R6 = 0) and from the 13th to the 53rd window period of each line.

When the display is disabled (R0 = 0), the access automaton keeps control over the bus.

READING WINDOW CODES AND CHARACTER SLICES

During each displayable window period (≃ 1.1 µs), the display automaton controls two read cycles on the internal bus.

On the first cycle, ADR(0:9) address a window code in the page memory.

The page memory is strobed by $\overline{SM}$ and a 16 bit window code is read (table 1).

The 11 bits of the attribute field A (0 : 6) and type field, A7, B(5 : 7) are latched in the display automaton.

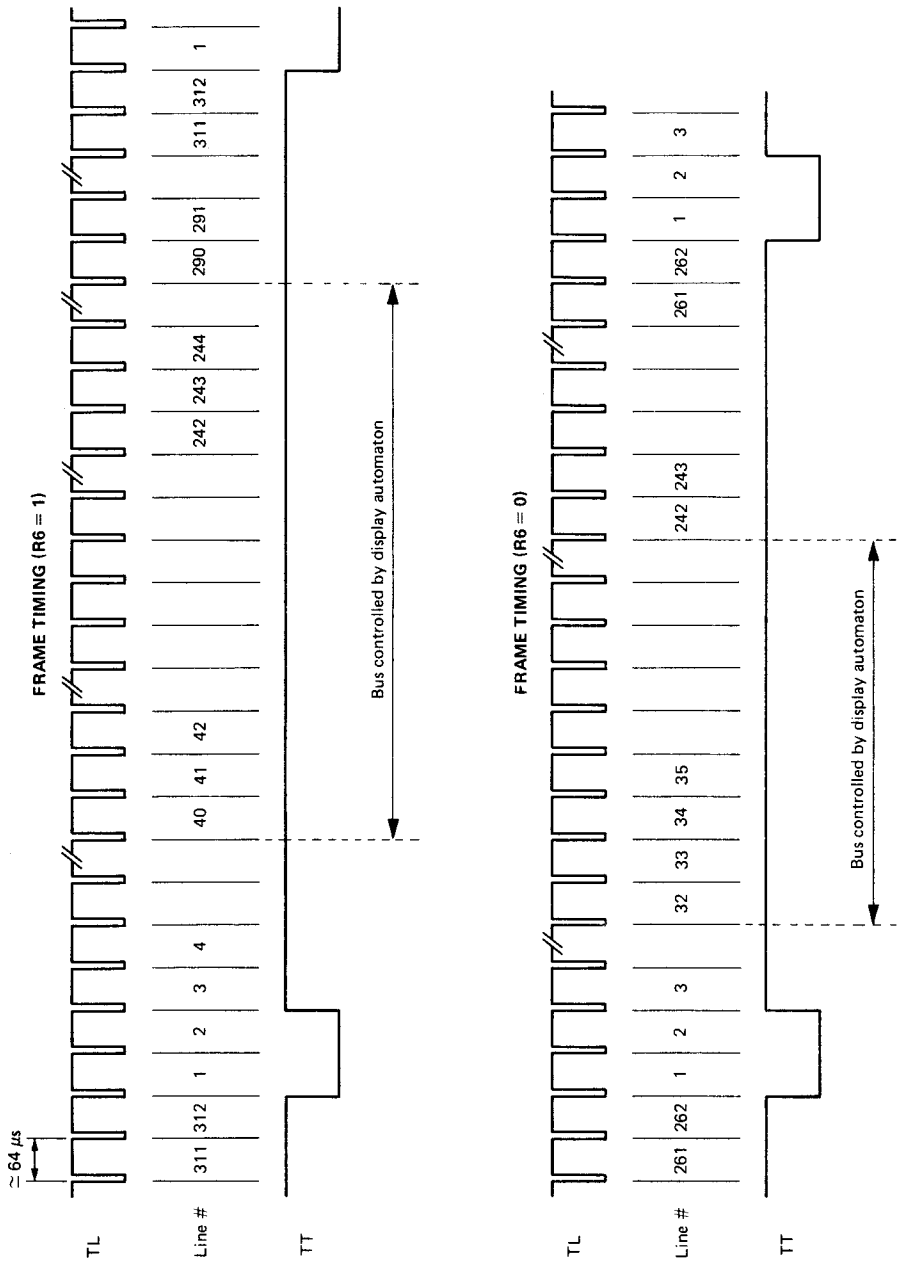
The 9 bits of the character code field A7, B(0 : 7) are latched in CC registers of the character generator.

CC register addresses one set of character and one character in the set.

A character is 10 slices of 8 bits each.

On the second cycle the slice number is given by ADR(0:3) and the extension select by ADR4. The character generator is strobed by $\overline{SG}$ and the value of the slice is read by the display automaton on the internal A(0:7) bus.

When a delimitor is addressed by CC, its contents is read in place of the value of the slice.


FRAME TIMING (R6 = 1)
≃ 64 µs
TL
Line #
TT
311 312 1 2 3 4 40 41 42 242 243 244 290 291 311 312 1
Bus controlled by display automaton
FRAME TIMING (R6 = 0)
TL
Line #
TT
261 262 1 2 3 32 33 34 35 242 243 261 262 1 2 3
Bus controlled by display automaton

INTERNAL BUS CYCLES

The different types of internal bus cycles are given in the table below :

CONTROL				ADDRESS BUS AD (0 : 9)	DATA BUS A(0:7), B(0:7)	CYCLE TYPE
R/$\overline{W}$I	$\overline{SM}$	$\overline{SG}$	$\overline{ST}$			
Read	Active			WINDOW ADDRESS (X', Y') or CURSOR (X, Y)	MP → VIN, MP → CC	1
Read		Active		SLICE ADDRESS (NT')	GC or CC → VIN	2
Write			Active	–	T → VIN	3
Read	Active		Active	CURSOR (X, Y)	MP → T	4
Write	Active		Active	CURSOR (X, Y)	T → MP	5
Read		Active	Active	SLICE ADDRESS (NT)	GC → T	6
Write		Active	Active	SLICE ADDRESS (NT)	T → GC	7

MP : Page Memory T : Mail Box GC : Character Generator CC : Character Code Register

1, 2 : Used by display automaton
3 : Load command in access automaton
4 : Read MP
5 : Write MP
6 : Read Slice
7 : Write Slice

} Controlled by access automaton

NOTA :
In cycle type 2, slice address is at ADR(0:3).
ADR4 gives the extension condition B7 ∧ (B5 ∨ B6) which has been latched on the previous type 1 cycle.
ADR(5:9) are not used.

In cycle types 6 and 7, slice address is at ADR(0:3). ADR4 gives the extension condition B7 ∧ (B5 ∨ B6) which has been latched on the previous type 1 cycle (with cursor address).

In cycle types 4 to 7, two strobes are simultaneously active. When a memory is read, T is written and reciprocally.

CHARACTER ATTRIBUTES

SERIAL ATTRIBUTES, PARALLEL ATTRIBUTES

The shape to be displayed in a window is defined by :
- a pattern held in the character generators and addressed by the CC field of the window code.
- the actual value of the attributes.

The attributes are :
- C_0 (3 bits) and C_1 (3 bits) : 2 colours
- Blinking (1)
- Double height (1) , Double width (1)
- Reverse video (1)
- Boxing (1)
- Conceal (1)
- Underlining (1)

In any column 0 window, their implicit value is Co = black, not boxed, not concealed, not underlined. The window code defines the type of the character to be displayed in this window and the value of its parallel attributes (see table 1). The value of the remaining attributes is serially defined by scanning the windows from left to right (column 0 to 39) then up to down. Therefore, any other type of character gives the values of C_0 for a subsequent string of alphanumerics. Besides, a delimitor gives the value of the boxing, conceal and underlining attributes for the following windows. A boxing zone is a string of windows belonging to the same row, in which the boxing attribute value is 1.

DOUBLE HEIGHT, DOUBLE WIDTH

- A correct operation assumes that the same window code had been repeated in the page memory (twice for double height or double width, four times for double size).

- No double height windows are supposed to be held in service row.

- No double width character should begin in column 39.

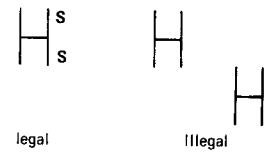
- Single sized, double width, double height and double sized characters may be mixed on a given row.

- But couple of rows bearing double height character should not be interleaved :

More precisely, this attribute defines a H parity for each row :

- service row is H even
- any row is H even if the preceding row does not hold any double height window.
- any row has an H parity reverse to the preceding row if the latter holds at least one double height window.

In the same way, double width define a W parity for the windows as double height for the rows.



DISPLAY OF NON DELIMITOR TYPES OF CHARACTERS

The display automaton interprets the attributes in the following order :

Underlining

- type α : slice 9 is set in the pattern.

Blinking

- blinking : the pattern is periodically (0.5 Hz) reset. If the video is reversed (α type only), the phase of the blinking clock is complemented. In "cursor" position, the reset does not occur.

Reverse video — Cursor position

- reverse video : (α only). The pattern is complemented.
- cursor position : (any type). The pattern is periodically complemented. If blinking is disabled (R7 = 0), the pattern is permanently complemented.

Double height, double width (α only)

- double width : each bit of the pattern is horizontally doubled so as to get a 10 x 16 double pattern. If the window is W even, only the left pattern is kept. The right pattern is kept if the window is W odd.

- double height : the slices of the pattern are repeated so as to get a 20 x 8 double pattern. If the row is H even, the upper pattern is kept, otherwise lower pattern is kept.
  The double pattern is obtained by :

  – tripling slice 0
  – doubling slice 1 to 8
  – keeping slice 9

  Double height and double width may be combined to get a double size.

Colors

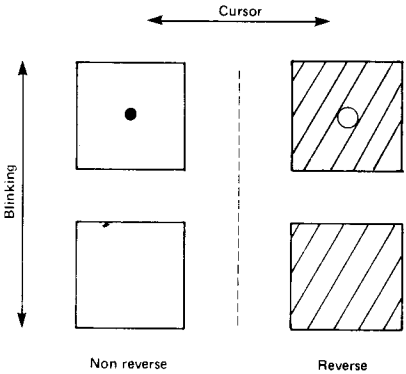
Each bit of the final 10 x 8 pattern corresponds to a pixel.

The color of the pixel is C_0 if the bit value is 0. Otherwise, it is C_1.

Boxing, conceal

If the conceal is enabled (R2 = 1), and if the window is in a conceal zone, then the colors in the window are reset to black.

If the boxing is enabled (R1 = 1), and if the window is out of a boxing zone, the color resets to black in the window and I output is low. The window is "transparent".



Non Reverse and reverse character display with blinking or in cursor position.

DISPLAY OF DELIMITORS

In the 10 x 8 implicit pattern associated with a delimitor, all the bits have the same value : 1.

"cursor" position : the pattern is periodically reset.

colors : same as any other type : a delimitor is displayed as a space in color C_1.

boxing : if the boxing is enabled (R5 = 1), and if the delimitor defines a boxing zone border, half of the window is transparent. Out of boxing zone, a delimitor is completely transparent.

Remark : the value of the lining and the conceal bits given by a delimitor is ignored in the window associated with this delimitor.

CHARACTER GENERATORS

GEN contains a CC register ; a standard 128 character α_0 set and a standard 128 semi graphic γ set.

Further extension of these character sets is easily done by adding 1 K x 8 standard ROM or RAM components (fig 8).

A latch CCE is loaded by the character code with $\overline{SM}$.

A quad 2 to 1 multiplexer transcodes 11 bits of logical address. – 96 character codes CCE (0 : 6) by 10 slice address codes ADR(0:3) – to 10 bits of physical address.

Logical Address

ADR3 = 0	CCE6	CCE5	CCE4	CCE3	CCE2	CCE1	CCE0	ADR2	ADR1	ADR0
ADR3 = 1	0	0	CCE4	CCE3	CCE2	CCE1	CCE0	CCE6	CCE5	ADR0

The external character generator is selected by ADR4 high and $\overline{SG}$ low. It is read or written whether R/$\overline{W}$I is high or low.

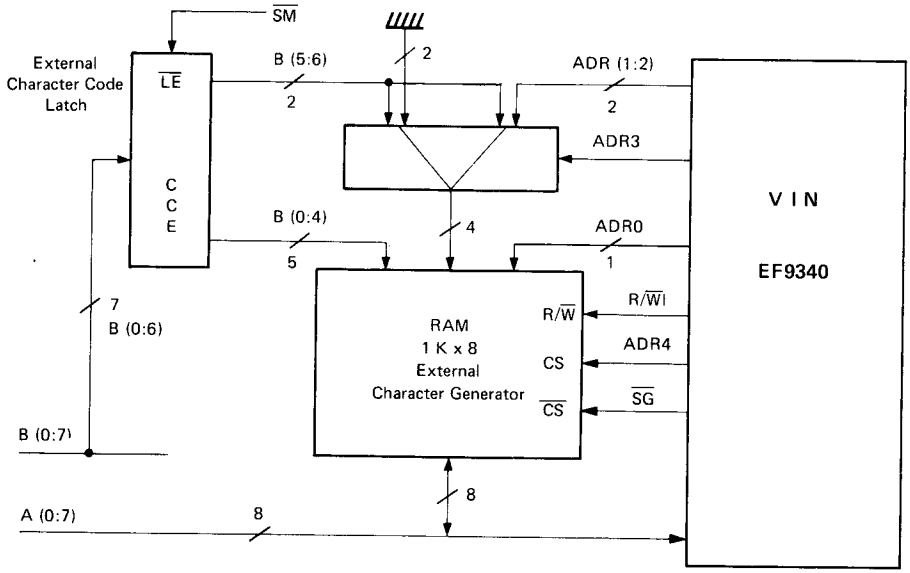


FIGURE 8 – ADDING AN EXTERNAL CHARACTER GENERATOR

TABLE 1 – CHARACTER CODES

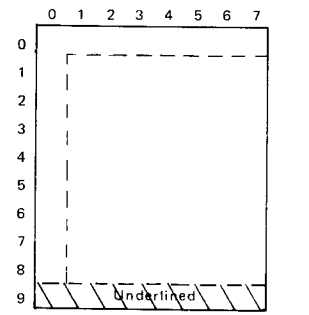
WINDOW CODE IN PAGE MEMORY																COMMENTS			
Type and character code field									Attribute field							Type	Implicite Attribute	Ad - hoc Serial Attribute	Remark
B7	B6	B5	B4	B3	B2	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0				
0	X	X	X	X	X	X	X	0	N	L	H	S	B_1	G_1	R_1	α_0 (128)		Underlined, C_0	in GEN
1	0	0	—	—	s	i	m	0	B_0	G_0	R_0	—	B_1	G_1	R_1	DEL			
1 1 1	0 1 1	1 0 1	X	X	X	X	X	0	N	L	H	S	B_1	G_1	R_1	α_1 (96)		C_0	EXTENSION
0	0	X	X	X	X	X	X	1	B_0	G_0	R_0	S	B_1	G_1	R_1	γ_S (64)	Normal size, positive		in GEN
0	1	X	X	X	X	X	X	1	B_0	G_0	R_0	S	B_1	G_1	R_1	γ_M (64)			
1	0	0	—	—	—	—	—	1	—	—	—	—	—	—	—	ILLEGAL			
1 1 1	0 1 1	1 0 1	X	X	X	X	X	1	B_0	G_0	R_0	S	B_1	G_1	R_1	γ_1 (96)	Normal size		EXTENSION

Nota : Extension for α 1 and γ 1 may be mapped in only one 1 K x 8 RAM or ROM.

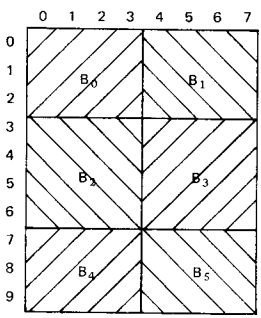
GLOSSARY :

α	:	Alphanumeric
γ	:	Semi-graphic
γS	:	Separated semi-graphic
γM	:	Mosaïc semi-graphic
DEL	:	Delimitor
m	:	Blanking
i	:	Boxing
s	:	Underlining

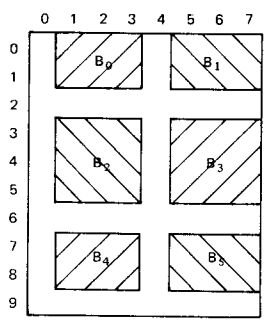
C_0 (R_0, G_0, B_0)	:	Background colour
C_1 (R_1, G_1, B_1)	:	Foreground colour
H	:	Double height
L	:	Double width
N	:	Reverse video (negative)
S	:	Stable (non blinking)
X	:	Character code
–	:	Don't care



α : ALPHANUMERIC



γM : Mosaïc



γS : Separated

γ : SEMI-GRAPHIC

TABLE 2 – COMMAND CODE

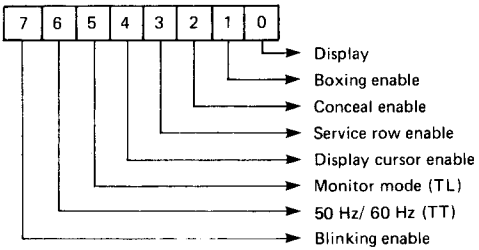
COMMAND CODE																NAME	OPERATION
B7	B6	B5	B4	B3	B2	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0		
0	0	0									K (0 : 4)					Begin Row	X (0 : 5) ← 0 Y (0 : 4) ← K (0 : 4)
0	0	1									K (0 : 4)					Load Y	Y (0 : 4) ← K (0 : 4)
0	1	0									K (0 : 5)					Load X	X (0 : 5) ← K (0 : 5)
0	1	1														INC C	C ← C+ 1
1	0	0						K (0 : 7)								Load M	M (0 : 7) ← K (0 : 7)
1	0	1						K (0 : 7)								Load R	R (0 : 7) ← K (0 : 7)
1	1	0									K (0 : 5)					Load Y0	Y0 (0 : 5) ← K (0 : 5)
1	1	1															Not interpreted

TABLE 3 – ACCESS MODE REGISTER

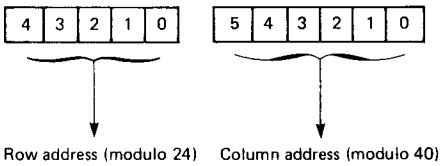
ACCESS MODE REG.								ACCESS MODE	SUBSEQUENT DATA TRANSFER
M7	M6	M5	M4	M3	M2	M1	M0		
0	0	0						Write	MP (C) ← T ; C ← C+ 1
0	0	1						Read	T ← MP (C) ; C ← C+ 1
0	1	0						Write without INC	MP (C) ← T
0	1	1						Read without INC	T ← MP (C)
1	0	0			N T			Write slice	GC (MP(C), NT) ← T ; NT ← NT+ 1
1	0	1			N T			Read slice	T ← GC (MP(C), NT) ; NT ← NT+ 1
1	1							Illegal	

NT : Slice number T : Mail Box C : Cursor MP : Page Memory GC : Character Generator

DISPLAY AND TIMING MODE REGISTER R



CURSOR REGISTER C



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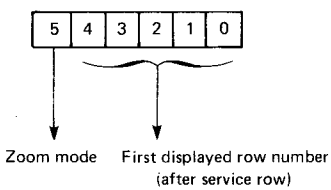
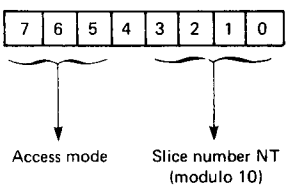
ORIGIN REGISTER Y0



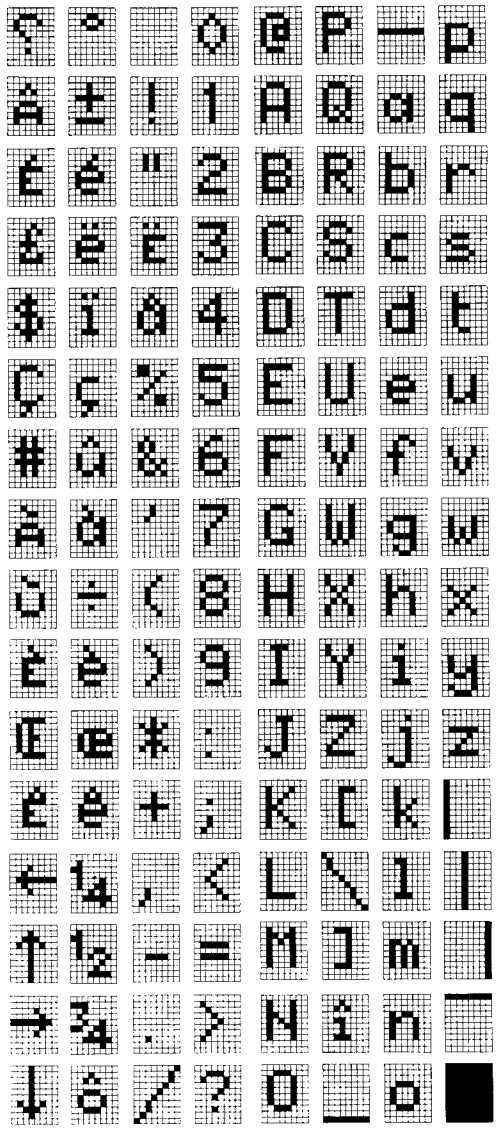
ACCESS MODE REGISTER M



ALPHANUMERIC CHARACTER SET

B7	0	0	0	0	0	0	0	0
B6	0	0	0	0	1	1	1	1
B5	0	0	1	1	0	0	1	1
B4	0	1	0	1	0	1	0	1

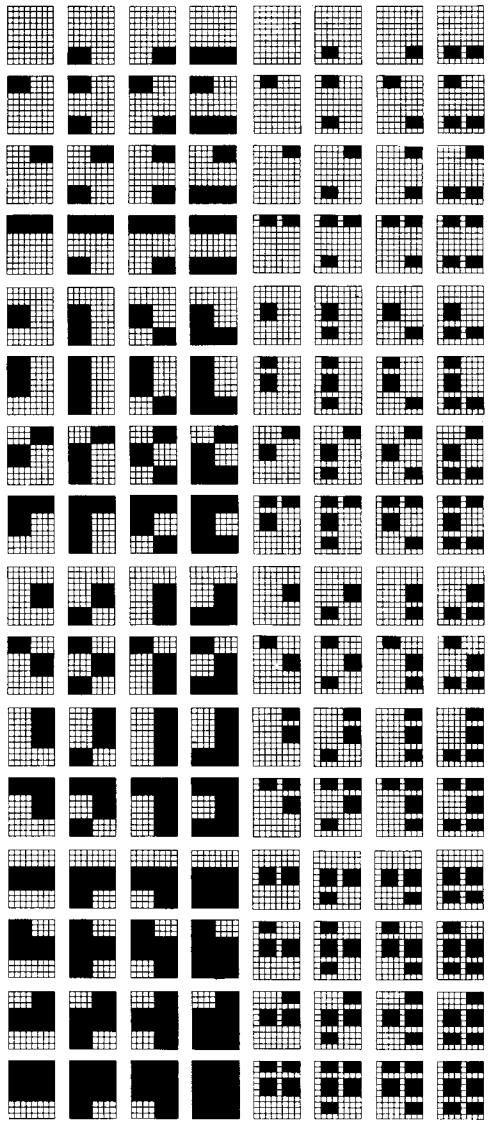
B3	B2	B1	B0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1



NOTA : Black dot = output high (GEN)

	MOSAIC Semi-graphic				SEPARATED Semi-graphic			
B7	0	0	0	0	0	0	0	0
B6	1	1	1	1	0	0	0	0
B5	0	0	1	1	0	0	1	1
B4	0	1	0	1	0	1	0	1

B3	B2	B1	B0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1



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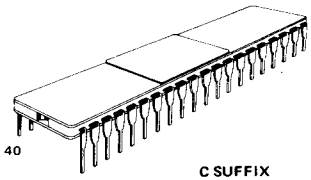
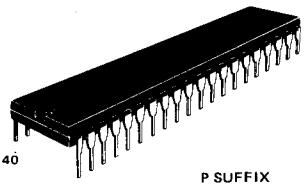
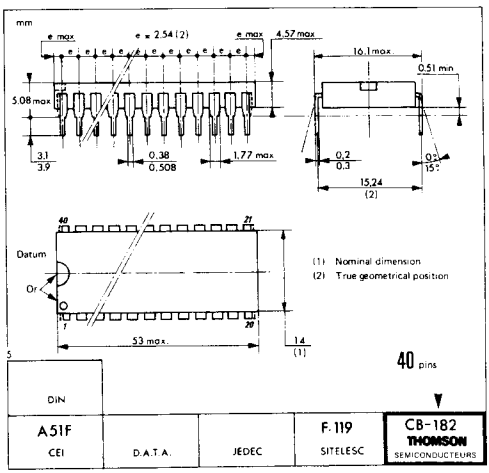


C SUFFIX
CERAMIC PACKAGE



P SUFFIX
PLASTIC PACKAGE



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