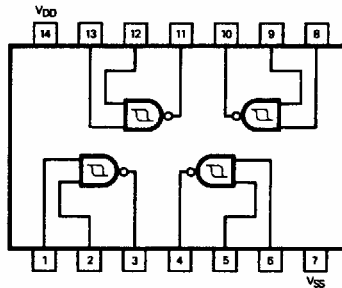


GD4093B

QUAD 2-INPUT NAND SCHMITT TRIGGER

GENERAL DESCRIPTION — The 4093B is a Quad 2-Input NAND Schmitt Trigger offering positive and negative threshold voltages, V_{T+} and V_{T-} which show very low variation with temperature (typically $0.0005 \text{ V/}^\circ\text{C}$ at $V_{DD} = 10 \text{ V}$) and typical hysteresis, V_{T+} to $V_{T-} \geq 0.33 V_{DD}$. Outputs are fully buffered for highest noise immunity.

**LOGIC AND CONNECTION
DIAGRAM DIP (TOP VIEW)**



NOTE:
The SO Package has the same pinouts (Connection Diagram) as the Dual In-line Package.

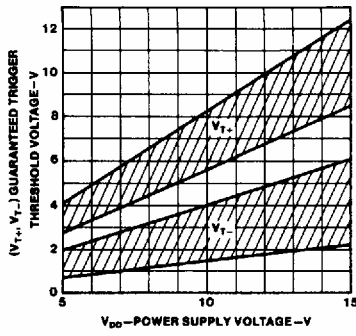
DC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0 \text{ V}$ (Note 1)

SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS	
		$V_{DD} = 5 \text{ V}$			$V_{DD} = 10 \text{ V}$			$V_{DD} = 15 \text{ V}$						
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX				
V_{T+}	Positive-Going Threshold Voltage	2.9	3.6	4.3	6.0	6.8	8.6	9	10	12.9	V	ALL	$V_{IN} = V_{SS}$ to V_{DD}	
V_{T-}	Negative-Going Threshold Voltage	0.7	1.4	1.9	1.4	3.2	4.0	2.1	5	6	V	ALL	$V_{IN} = V_{DD}$ to V_{SS}	
V_{T+} to V_{T-}	Hysteresis	1.0	2.2	3.6	2.0	3.6	7.2	3	5	6	V	ALL	Guaranteed Hysteresis = V_{T+} Minus V_{T-}	
I_{DD}	Quiescent Power Supply Current	XC	1			2			4			μA	MIN, 25°C	All Inputs at 0V or V_{DD} .
			7.5			15			30				MAX	
		XM	0.25			0.5			1			μA	MIN, 25°C	
			7.5			15			30				MAX	

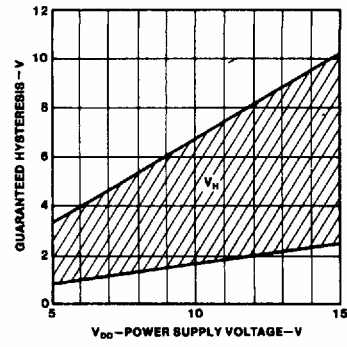
NOTES:

1. Additional dc characteristics are listed in this section under Goldstar 4000B series CMOS family characteristics.

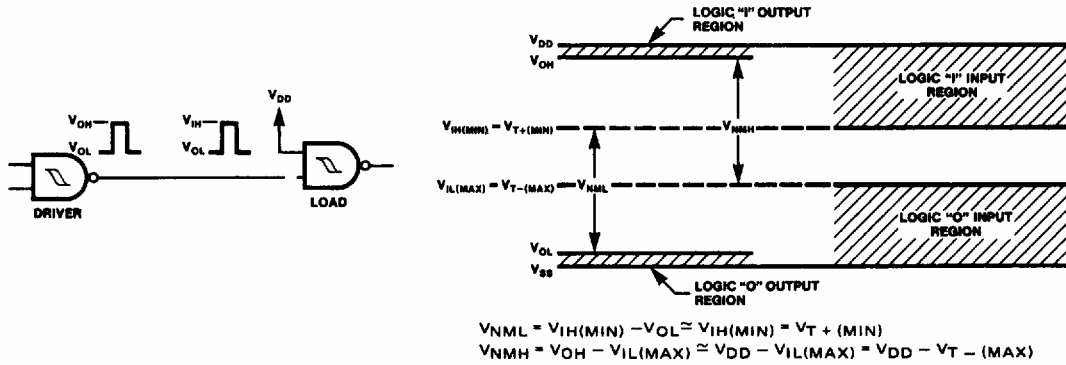
GUARANTEED TRIGGER THRESHOLD VERSUS V_{DD}



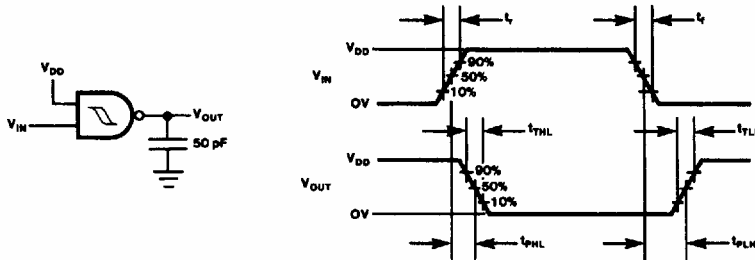
GUARANTEED HYSTERESIS VERSUS V_{DD}



INPUT AND OUTPUT CHARACTERISTICS



AC TEST CIRCUITS AND SWITCHING TIME WAVEFORMS



AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS See Note 2
		V _{DD} = 5 V			V _{DD} = 10 V			V _{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t _{PLH}	Propagation Delay		60	110		25	60		20	48	ns	C _L = 50 pF, R _L = 200 kΩ
t _{PHL}			60	110		25	60		20	48		
t _{TLH}	Output Transition Time		60	135		30	70		20	45	ns	Input Transition Times < 20 ns
t _{THL}			60	135		30	70		20	45		

NOTE
Propagation Delays and Output Transitions Times are Graphically Described in Section Under Series CMOS Family Characteristics.