Ordering number : ENN*6685

CMOS IC

LC7454A/M

CMOS Data Slicer

Preliminary

Overview

The LC7454A/M is a data slicer IC for the Index Plus + signals. The LC7454A/M extracts the Caption and the Index Plus + data form the Vertical Blanking Period of the TV signal and send it out to the decoder IC (Usually Microcomputer).
The LC7454A/M can be used to extract the Closed Caption signals, the XDS signals and the Index Plus + signals.

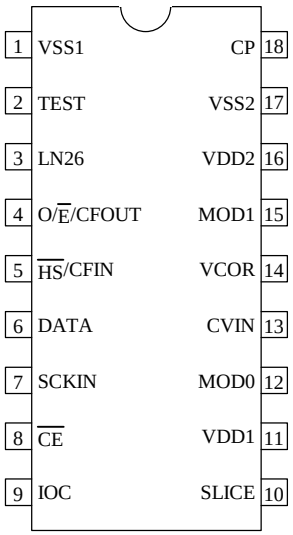
Features

(1) Low power dessipation by CMOS process
(2) Stable signal extraction by integrated peak hold circuit and digital circuit.
(3) Operation Voltage range : 5V ± 10%
(4) Package LC7454A : DIP18
LC7454M : MFP20

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

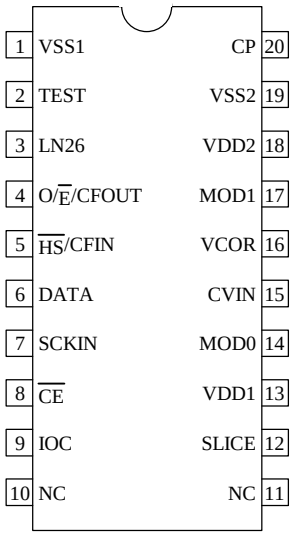
Pin Assignment

DIP18



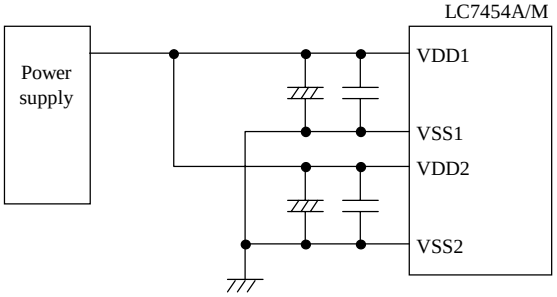
LC7454A

MFP20



LC7454M

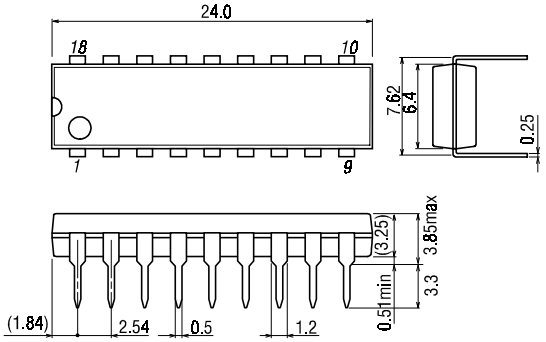
* VDD1and VSS1are power supply terminals for digital circuit. VDD2 and VSS2 are power supply terminals for analog circuit. Connect there terminals as the following diagram in order to reduce the noise disturbance between two powers.



Package Dimension

(unit : mm)

3007B

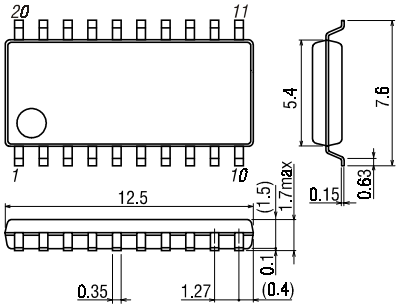


SANYO : DIP-18

Package Dimension

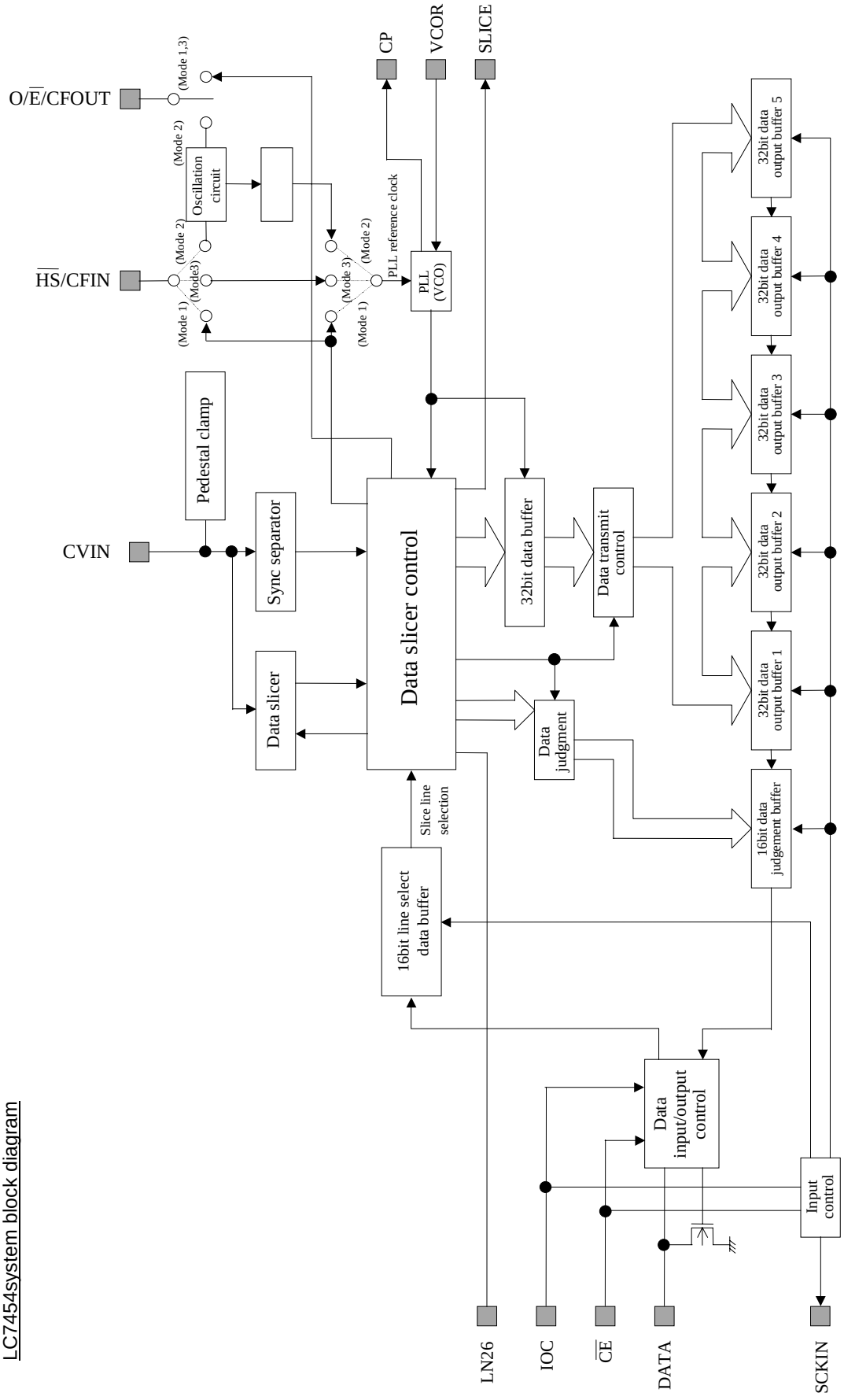
(unit : mm)

3036C



SANYO : MFP-20

LC7454system block diagram



Operation on each mode

The LC7454 has three operating modes. The operation mode be selected by the status of MOD0 and MOD1 terminals. The functionality of three modes are the same. Only the PLL reference frequency which is used to generate operation clock is different. Use mode1 or mode3 only in the application which uses 2x data. Any mode (Mode1,2 or 3) can be used in the 1x data only application.

Terminal		MODE	Applications	PLL reference
MOD1	MOD0			
Open	Open	Mode1	NTSC-VCR	Use H-sync signal which is separated from C-Video signal.
Open	VDD1	Mode2	NTSC-VCR	Use 1/32 divided signal 503 KHz which is generated by external ceramic resonator.
VDD	Open	Mode3	NTSC-TV	Use H-sync signal from Fly Back.

Terminal Functions

Terminal # (DIP18)	Terminal name	Function Description		
		Mode 1	Mode 2	Mode 3
1	VSS1	Ground		
2	TEST	Test terminal, Open in normal operation		
3	LN26	32μs Pulse output at line 26 timing on both field		
4	O/$\overline{E}$/CFOUT	Pulse output for field judgment *1	Output terminal for ceramic resonator	Pulse output for field judgment *1
5	$\overline{HS}$/CFIN	Sync separated $\overline{HS}$ pulse output	Input terminal for Ceramic resonator	External $\overline{HS}$ pulse input
6	DATA	Line select data input and slice data output *2		
7	SCKIN	Data transmit clock input		
8	$\overline{CE}$	Chip select input *3		
9	IOC	Data direction control signal input *4		
10	SLICE	Pulse output at selected slice line		
11	VDD1	Power terminal		
12	MOD0	Open	Connect to VDD	Open
13	CVIN	Conposit video input		
14	VCOR	Connect resister for internal VCO oscillation frequency control		
15	MOD1	Open	Open	Connect to VDD
16	VDD2	Power terminal		
17	VSS2	Ground		
18	CP	Filter terminal for internal PLL		

*1 'H' level in Odd field, 'L' level in Even field.

*2 N-ch open drain in output mode.

*3 Feed 'L' level only when data transmission is in effect. If CE='H', data terminal will become input/output disable, SCKIN terminal will become input disable.

*4 'H' level : Output mode
'L' level : Input mode

1. Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min.	typ.	max.	
Maximum Supply voltage	VDDMAX	VDD1,VDD2	VDD1=VDD2	-0.3		+7.0	V
Input voltage	VI	CVIN,SCKIN, $\overline{CE}$,IOC		-0.3		VDD+0.3	
Output voltage	VO	LN26, O/$\overline{E}$ /CFOUT,SLICE		-0.3		VDD+0.3	
Input/output voltage	VIO	DATA, $\overline{HS}$ /CFIN		-0.3		VDD+0.3	
Allowable power dissipation	Pdmax	DIP18				300	mW
		MFP20				150	
Operating temperature	Topr			-30		+70	°C
Storage temperature	Tstg			-55		+150	

* VSS1 and VSS2 must be the same level.
  VDD1 and VDD2 must be the same level.

2. Allowable Operating Conditions at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Operating Supply voltage	VDD	VDD1,VDD2	VDD1=VDD2		4.5		5.5	V
'H' level input voltage	VIH	$\overline{HS}$ /CFIN, DATA, SCKIN, $\overline{CE}$, IOC		4.5 to 5.5	0.75VDD		VDD	
'L' level input voltage	VIL	$\overline{HS}$ /CFIN, DATA, SCKIN, $\overline{CE}$, IOC		4.5 to 5.5	VSS		0.25VDD	
CVIN input amplitude	CVSYNC	CVIN	SYNC-WHITE=1.0V	4.5 to 5.5	1Vp-p -3dB	1V	1Vp-p +3dB	
$\overline{HS}$ input frequency range	fH	$\overline{HS}$ /CFIN	Mode3	4.5 to 5.5	15.23	15.73	16.23	kHz
Oscillation frequency range (Note 1)	FmCF	$\overline{HS}$ /CFIN O/$\overline{E}$ /CFOUT	•Mode2 •Refer to figure 1	4.5 to 5.5		503		
Oscillation stabilizing time period (Note 2)	tmsCF	$\overline{HS}$ /CFIN O/$\overline{E}$ /CFOUT	•MODE2 •Refer to figure 2	4.5 to 5.5		0.5	5	ms

(Note 1) Refer to table 1 for oscillator constants.
(Note 2) Oscillation stabilizing period is the time needed to stabilize the oscillation after power is fed.
Refer to figure 2.

3. Electrical Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
'H' level input current	IIH	$\overline{HS}$ /CFIN, DATA, SCKIN, $\overline{CE}$, IOC	VIN=VDD	4.5 to 5.5			1	µA
'L' level input current	IIL	$\overline{HS}$ /CFIN, DATA, SCKIN, $\overline{CE}$, IOC	VIN=VSS	4.5 to 5.5	-1			
'H' level output voltage	VOH	LN26, SLICE, O/$\overline{E}$ /CFOUT, $\overline{HS}$ /CFIN	IOH=-4mA	4.5 to 5.5	VDD-1.2			V
'L' level output voltage	VOL	LN26, DATA, O/$\overline{E}$ /CFIN, $\overline{HS}$ /CFIN, SLICE	IOL=10mA	4.5 to 5.5			1	
Input clamp voltage	VCLMP	CVIN		5.0	2.3	2.5	2.7	
Clamp input current	CII	CVIN	CVIN=3V	5.0	5	10	18	µA
Clamp output current	COI	CVIN	CVIN=2V	5.0	-120	-70	-30	
Power dissipation	IDD	VDD1,VDD2		4.5 to 5.5		8	20	mA

4. Serial Input/Output Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter			Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Serial clock	Input clock	Cycle	tCKCY	SCKIN	Refer to figure 3	4.5 to 5.5	1			µs
		'L' Level pulse width	tCKL	SCKIN	Refer to figure 3	4.5 to 5.5	0.5			
		'H' Level pulse width	tCKH	SCKIN	Refer to figure 3	4.5 to 5.5	0.5			
	Set up time		tICK	SCKIN	•Applied to $\overline{CE}$ falling edge. •Refer to figure 3	4.5 to 5.5	1			
Serial input	Data set up time		tIDO	DATA	•Applied to SCKIN rising edge. •Refer to figure 3	4.5 to 5.5	0.1			
	Data hold time		tHDO			4.5 to 5.5	0.1			
Serial output	Output delay		tODT	DATA	•Applied to SCKIN falling edge. •Use external 1kΩ pull-up resister. •Refer to figure 3	4.5 to 5.5			0.5	

Table 1. Ceramic resonator constants

Type of oscillation	Maker	Resonator	C1	C2
503kHz ceramic oscillation	Murata	CSB 503E9	150pF	150pF

* Both C1 and C2 must be use K rank (±10%) and SL characteristics.

(Notes) • Please place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length since the circuit pattern affects the oscillation frequency.
• If you use other oscillators herein, we provide no guarantee for the characteristics.

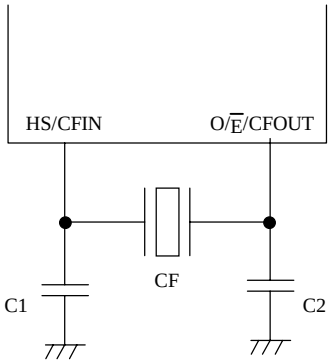


Figure 1 Ceramic resonator oscillation

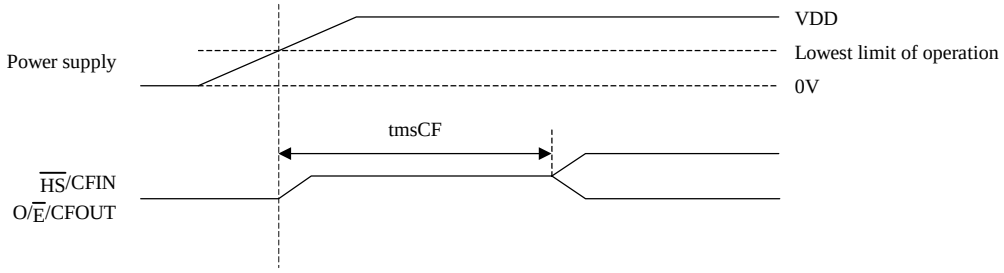


Figure 2 Oscillation stable time period

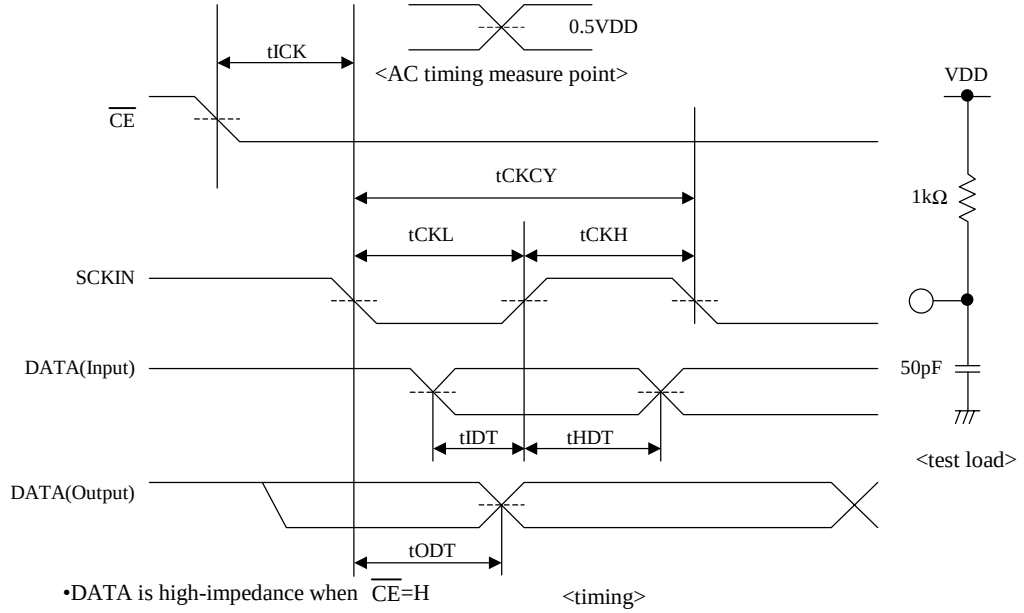
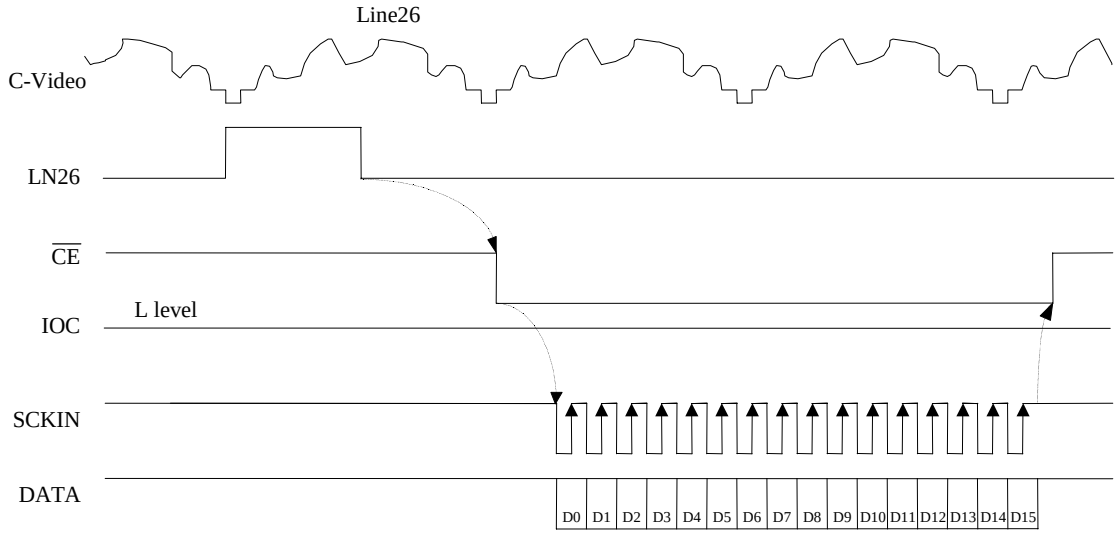


Figure 3 Serial output test condition

Slice line selection

<Input timing of slice selection data>



Slice line selection data is sent to the LC7454 in serial format . When sending the data to LC7454, the IOC terminal has to be 'L' level (It will change the Data line to the input mode). The data has to be transmitted after sensing the LN26 signal. Before sending the data, set the CE terminal to the 'L' level. Each bit of the data has to be changed at the falling edge of the SCKIN and the data is captured into the LC7454 at raising edge of the SCKIN signal.

<Selection of slice line>

Maximum of 5 lines between line 10 and 25 can be selected at a time in a field. The LC7454 can slice 1x and 2x data format signals.

Each D0 to D15 corresponds to line 10 to line 25. Set specific bit to 'H' to select the corresponding line.

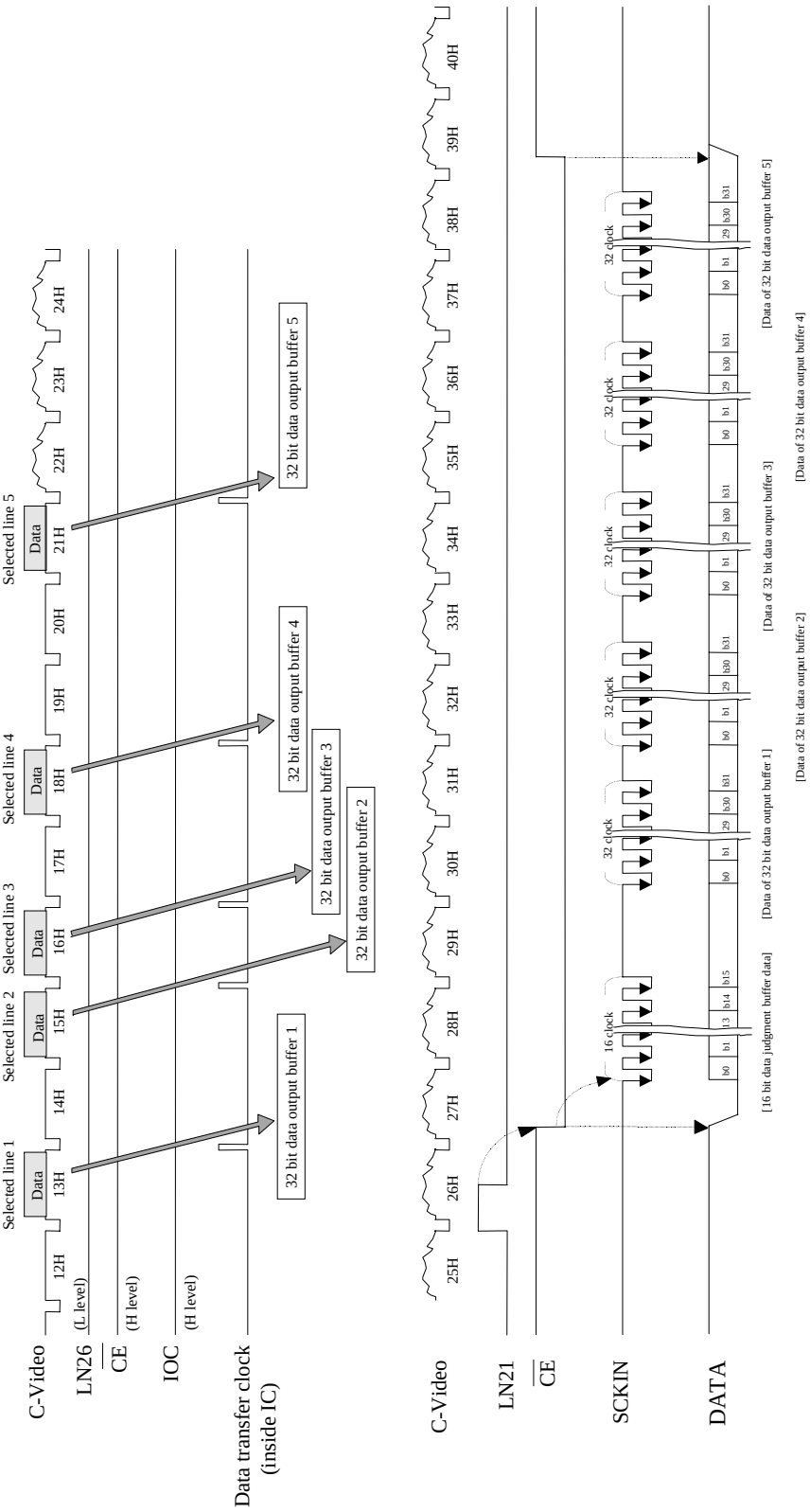
Example: To select 15, 18, 19, 21 and 23 lines

Send D0 - D15 = [0000010011010100]

Note: If more than 6 line are selected, data extraction will be made on the first 5 lines. The data on the 6th line and after are not extracted.

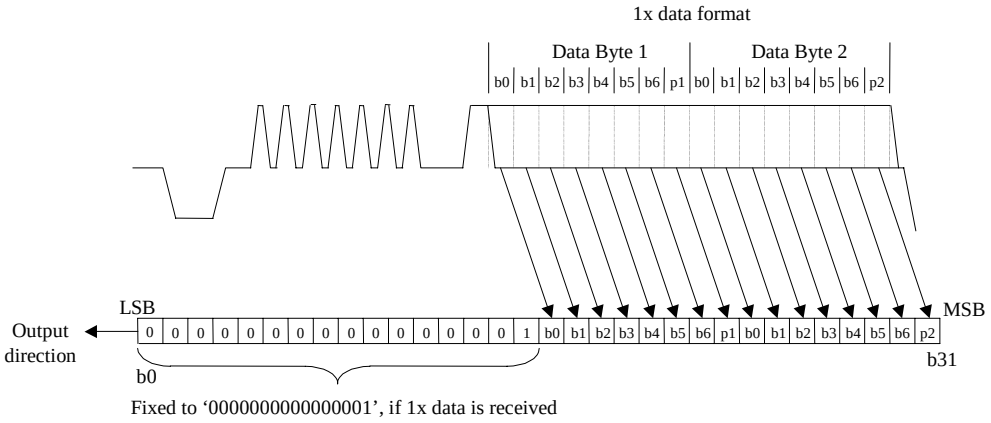
The new data sent to the LC7454 takes effects from the next field.

Data output timing

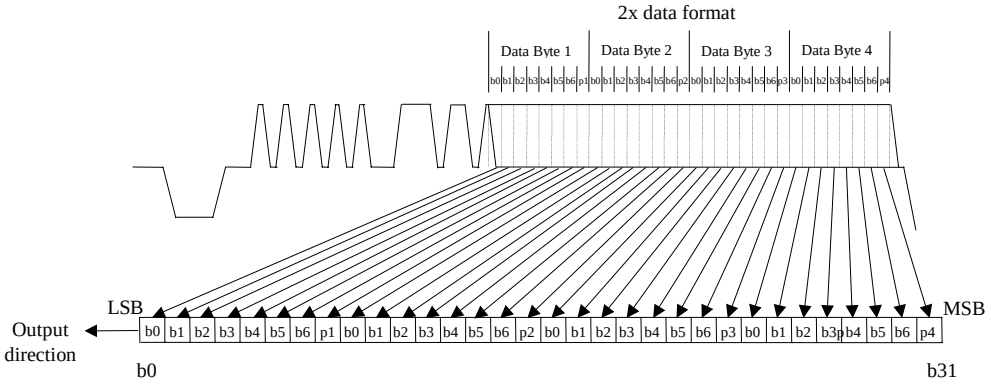


<Data format>

The LC7454 can extract the Index Plus + format data.
If the line contains the 1x format data, the first 15 bits of the 32 bit data buffer are filled with '0' and 16th bit becomes '1'. The extracted data is stored is stored form 16th to 31st bit.



32 bit data output buffer

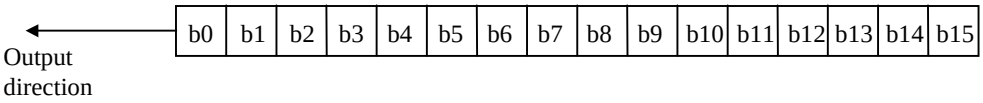


32 bit data output buffer

Five 32 bit data buffer are provided to store maximum of 5 line data in a field. If the data with correct format exists in the selected lines, the extracted data are stored into the buffers by the order of line number. If correct data is not found on the selected line, the data buffer is filled with '0'. All five data buffers are cleared by the line 10 sensing signal in the next field. Therefore, the data have to be read out between LN26 and the line 10 of the next field.
Please read only the selected buffers. For example, if three lines are selected, read the first three 32 bit buffers only.

<16 bit data judgment buffer>

The data judgment buffer includes the data which indicates the existence of the Index Plus + format data and data rate (1x or 2x). Bit 0 to 4 contain the existence of the signal and bit 8 to 15 contain the data rate. Bit 7 contains the field information (Odd or Even). The following table shows functions of each bit.



b0 to b7 : Existence of 1x or 2x data format.

Bit	Contents	Note
b0	0 : Data do not exist on the first selected line. 1 : Data exist on the first selected line.	'0' if no line is selected.
b1	0 : Data do not exist on the second selected line. 1 : Data exist on the second selected line.	'0' if one or less line is selected.
b2	0 : Data do not exist on the third selected line. 1 : Data exist on the third selected line.	'0' if two or less line is selected.
b3	0 : Data do not exist on the fourth selected line. 1 : Data exist on the fourth selected line.	'0' if three or less line is selected.
b4	0 : Data do not exist on the fifth selected line. 1 : Data exist on the fifth selected line.	'0' if four or less line is selected.
b5 b6	NOT USE always"0"	
b7	0 : Even field 1 : Odd field	

b8 to b15 : Data format judgment on the selected line.

Bit	Contents	Note
b8	0 : 1x data format on the first line. 1 : 2x data format on the first line.	'0' if no line is selected.
b9	0 : 1x data format on the second line. 1 : 2x data format on the second line.	'0' if one or less line is selected.
b10	0 : 1x data format on the third line. 1 : 2x data format on the third line.	'0' if two or less line is selected.
b11	0 : 1x data format on the fourth line. 1 : 2x data format on the fourth line.	'0' if three or less line is selected.
b12	0 : 1x data format on the fifth line. 1 : 2x data format on the fifth line.	'0' if four or less line is selected.
b13 b14 b15	NOT USE always"0"	

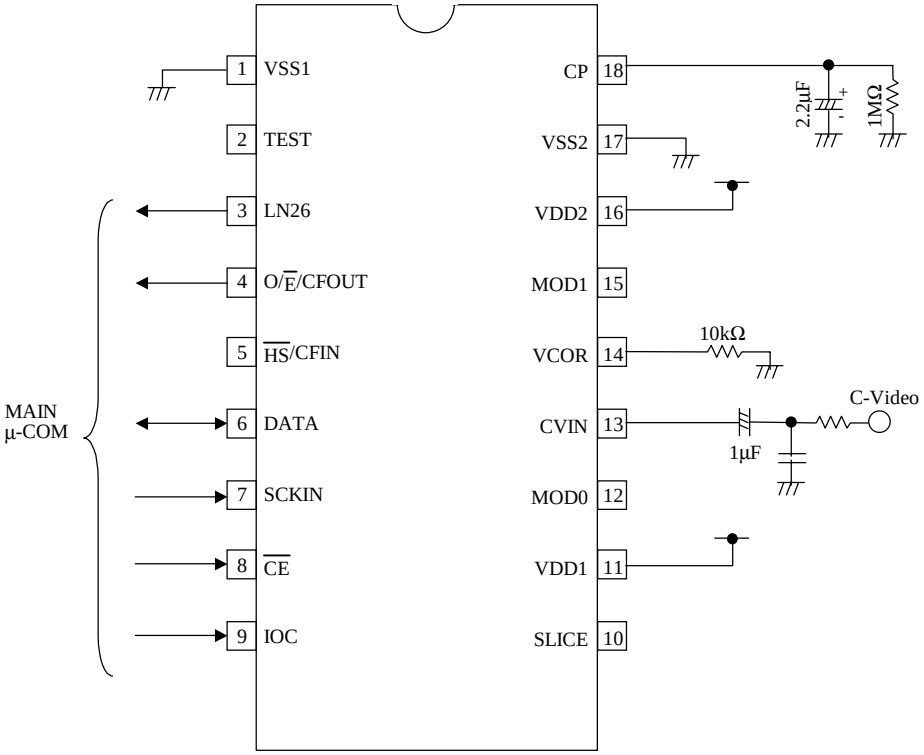
*If neither 1x nor 2x data are sensed on the selected line, these bits become '0'.

*16 bit data judgment buffer is cleared at the next line 10 as well as 32 bit data output buffer 1-5.

*Even though the data judgment buffer indicates the existence of the data, it is recommended that the existence of the data should be verified by checking the parity bit of the data.

Applications (Mode 1)

DIP18



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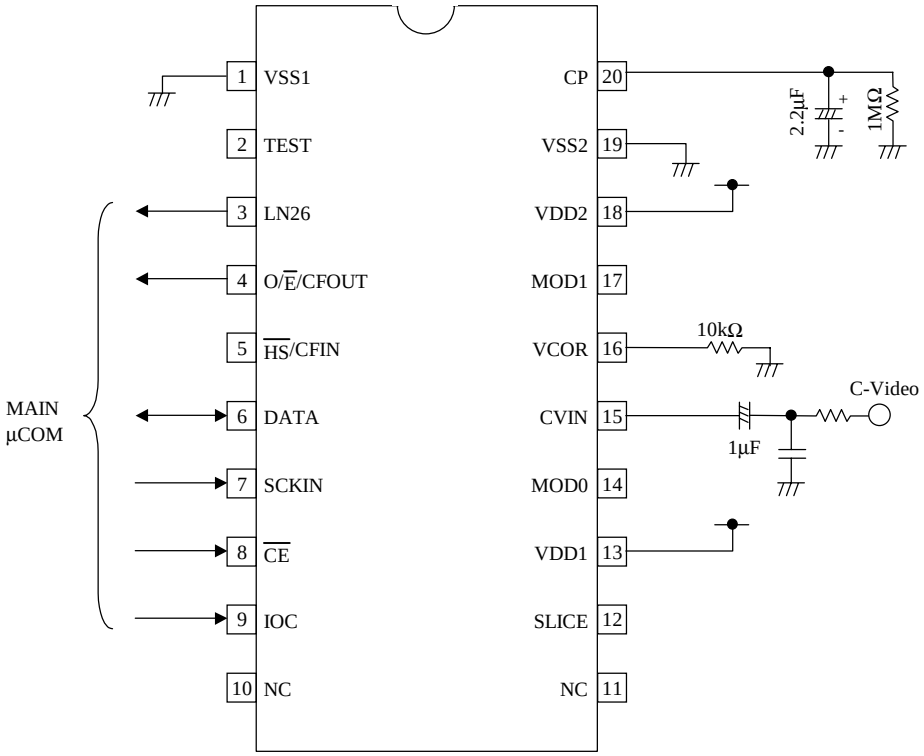
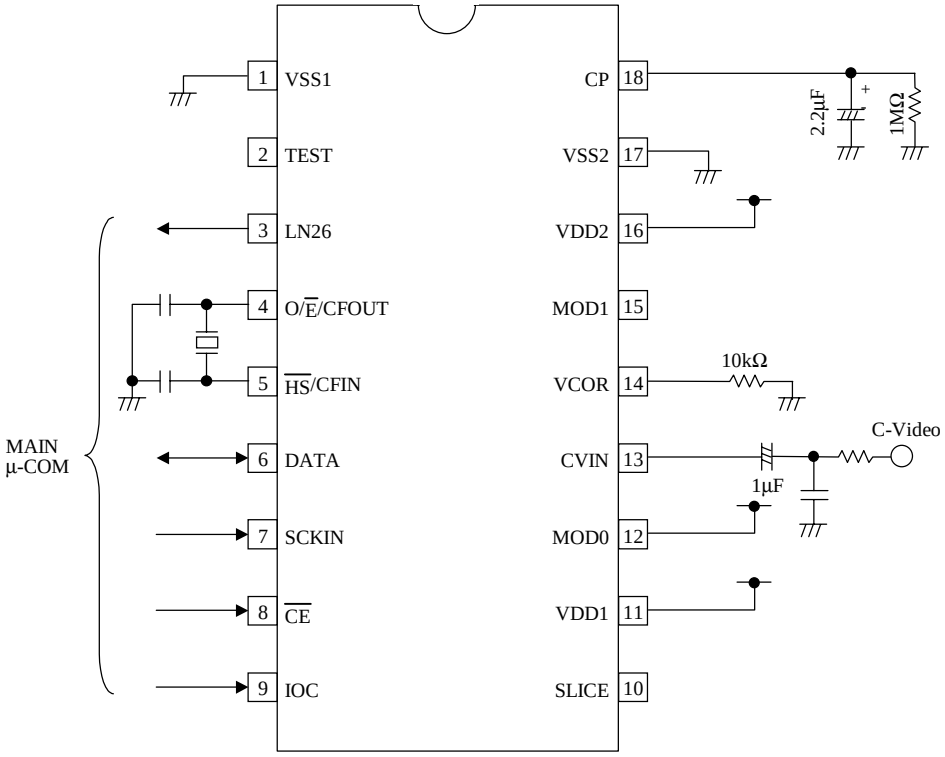


Applications (Mode 2)

DIP18



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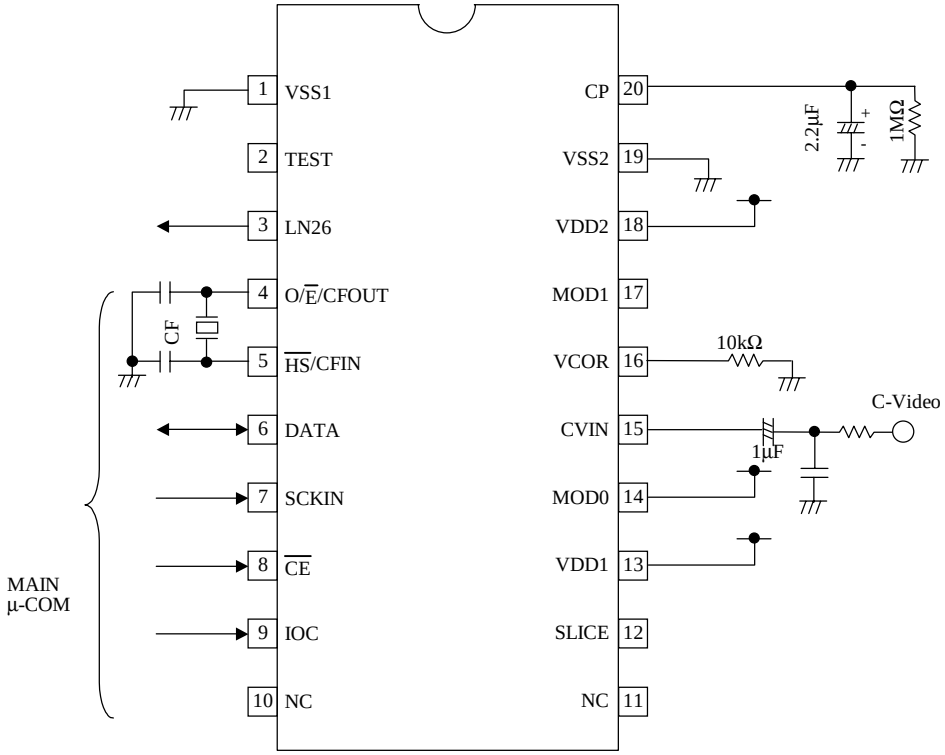
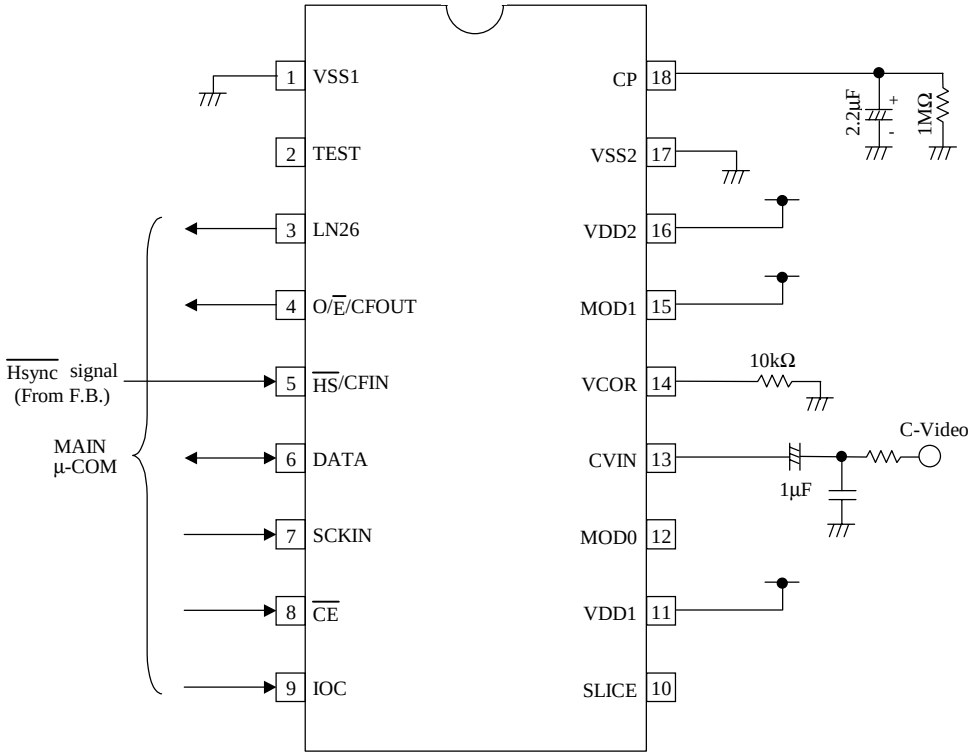


Applications (Mode 3)

DIP18



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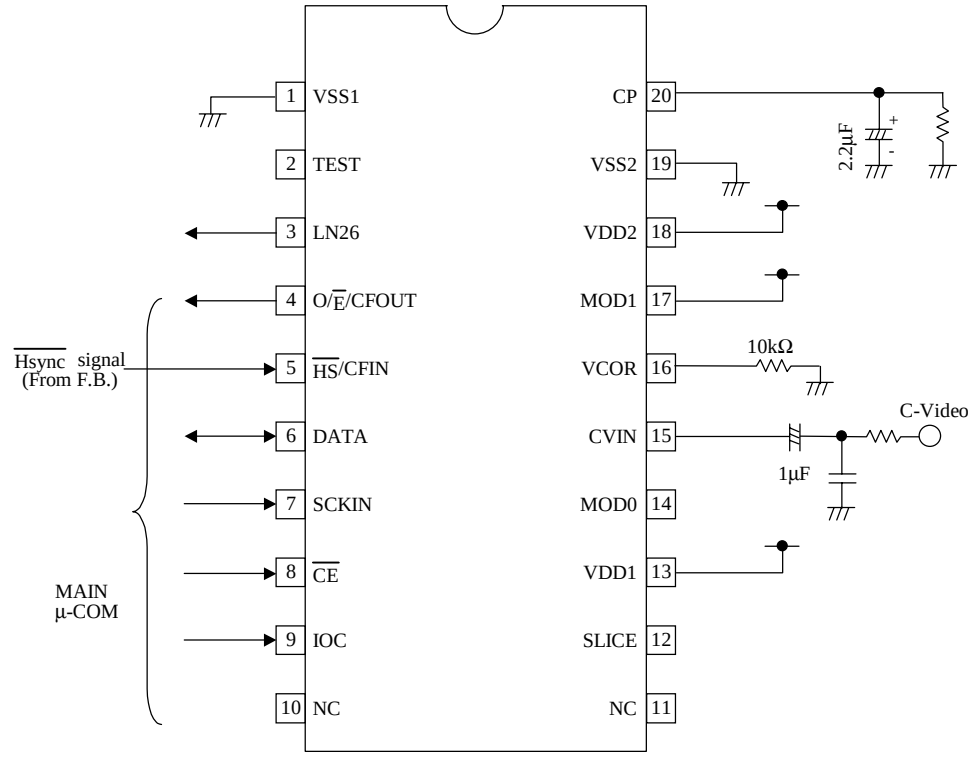

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