DATA SHEET

TDA4657
Generic multi-standard decoder

Preliminary specification
File under Integrated Circuits, IC02

June 1993

Philips
Semiconductors

PHILIPS

Generic multi-standard decoder TDA4657

FEATURES

- Low voltage (8 V)
- Low power dissipation (250 mW)
- Automatic standard recognition
- No adjustments required
- Reduced external components
- Not all time constants integrated (ACC, SECAM de-emphasis).

GENERAL DESCRIPTION

The TDA4657 is a monolithic integrated multi-standard colour decoder for PAL, SECAM and NTSC 4.43 MHz with negative colour difference output signals. It is adapted to the integrated baseband delay line TDA4660/61.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		7.2	8.0	8.8	V
I_P	supply current	V_P = 8.0 V; without load	25	31	37	mA
P_{tot}	total power dissipation	V_P = 8.0 V; without load	–	248	296	mW
Inputs						
V_9	chrominance input voltage (peak-to-peak value)	note 1	20	200	400	mV
V_{20}	sandcastle input voltage		–	–	13.2	V
Outputs						
V_1	colour difference output signals (peak-to-peak value)	independent of supply voltage; note 2				
	–(R–Y) output PAL and NTSC 4.43 MHz		442	525	624	mV
	SECAM		950	1050	1150	mV
V_3	–(B–Y) output PAL and NTSC 4.43 MHz		559	665	791	mV
	SECAM		1200	1330	1460	mV

Notes to the quick reference data

1. Within 2 dB output voltage deviation.
2. Burstkey width 4.3 μs
   Burst width 2.25 μs,
   ratio burst chrominance amplitude 1/2.2.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4657	20	DIL	plastic	SOT146(1)
TDA4657T	20	SO	plastic	SOT163A(2)

Note

1. SOT146-1; 1996 November 26.
2. SOT163-1; 1996 November 26.

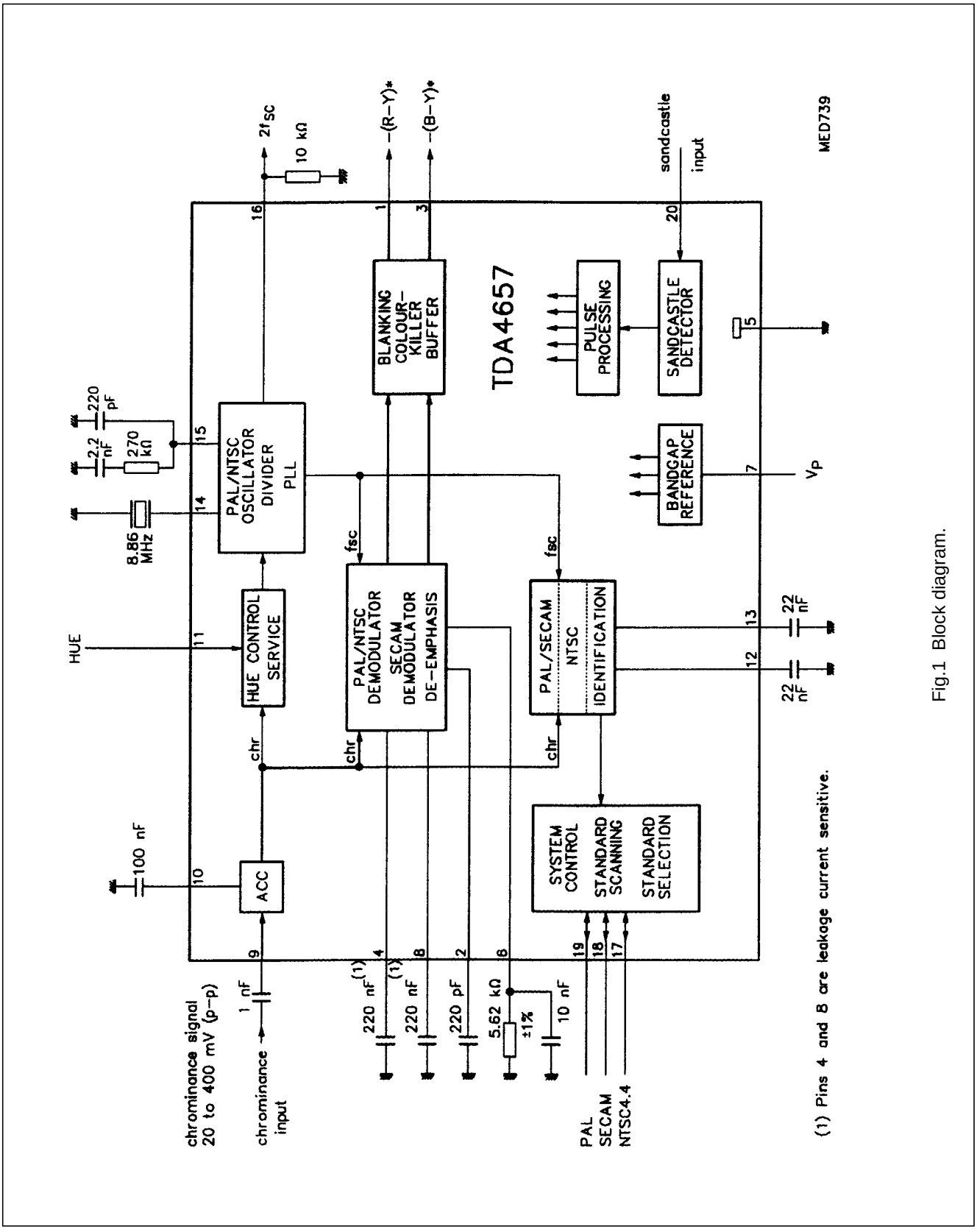


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$-(R-Y)_O$	1	colour difference signal output –(R–Y)* for baseband delay line
DEEM	2	external capacitor for SECAM de-emphasis
$-(B-Y)_O$	3	colour difference signal output –(B–Y)* for baseband delay line
CFOB	4	external capacitor SECAM demodulator control (B–Y) Channel
GND	5	ground
I_{REF}	6	external resistor for SECAM oscillator
V_P	7	supply 8 V
CFOR	8	external capacitor SECAM demodulator control (R–Y) Channel
CHR_I	9	chrominance signal input
C_{ACC}	10	external capacitor for ACC control
HUE	11	input for HUE control and service switch
N_{IDT}	12	external capacitor for identification circuit (NTSC)
P_{IDT}	13	external capacitor for identification circuit (PAL and SECAM)
OSC	14	PAL crystal
PLL	15	external loop filter
2FSC	16	$2 \times f_{sc}$ output
N_o	17	standard setting input/output for NTSC 4.43
SEC_o	18	standard setting input/output for SECAM
PAL_o	19	standard setting input/output for PAL
SC	20	sandcastle input

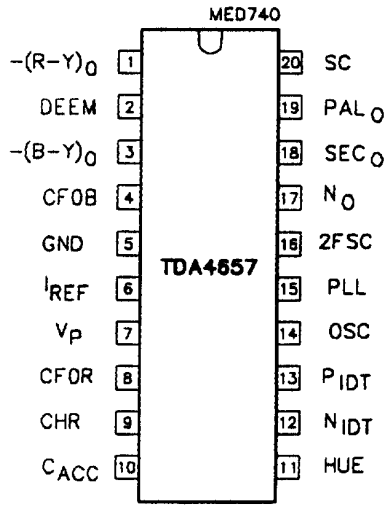


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The IC contains all functions required for the identification and demodulation of signals with the standards PAL, SECAM and NTSC 4.3 with 4.43 MHz colour-carrier frequency. When an unknown signal is fed into the input, the circuit has to detect the standard of the signal, and has to switch on successively the appropriate input filter and demodulator and finally, after having identified the signal, it has to switch on the colour and, in event of NTSC reception, the hue control. At the outputs the two colour difference signals –(R–Y)* and –(B–Y)* are available.

ACC stage

The chrominance signal is fed into the asymmetrical input (pin 9) of the ACC stage (Automatic Colour Control). The input has to be AC coupled and has an input impedance of 20 kΩ in parallel with 10 pF.
To control the chrominance amplitude the modulation independent burst amplitude is measured during the burstkey pulse which is derived from the sandcastle pulse present at pin 20. The generated error current is fed into an external storage capacitor at pin 10. The integrated error voltage controls the gain of the ACC stage so that its output is independent of input signal variations.
The measurement is disabled during the vertical blanking to avoid failures because of missing burst signals.

Reference signal generation

The reference signal generation is achieved by a PLL system. The reference oscillator operates at twice the colour-carrier frequency and is locked on the burst of the chrominance signal (chr). A divider provides reference signals (f_{sc}) with the correct phase relationship for the PAL/NTSC demodulator and the identification part. In the SECAM mode the two f_0 frequencies are derived from the PAL crystal frequency by special dividers. In this mode the oscillator is not locked to the input signal. In the NTSC mode the hue control circuit is switched between ACC stage and PLL. The phase shift of the signal can be controlled by a DC voltage at pin 11. The hue control circuit is switched off during scanning.
The reference frequency ($2 \times f_{sc}$) is available at pin 16 to drive a PAL comb filter for example.

Demodulation

The demodulation of the colour signal requires two demodulators. One is common for PAL and NTSC signals, the other is for SECAM signals.
The PAL/NTSC demodulator consists of two synchronized demodulators, one for the (B–Y) Channel and the other for the (R–Y) Channel. The required reference signals (f_{sc}) are input from the reference oscillator. In NTSC mode the PAL switch is disabled.
The SECAM demodulator consists of a PLL system. During vertical blanking the PLL oscillator is tuned to the f_0 frequencies to provide a fixed black level at the demodulator output. During demodulation the control voltages are stored in the external capacitors at pins 4 and 8.
The oscillator requires an external resistor at pin 6. Behind the PLL demodulator the signal is fed into the de-emphasis network which consists of two internal resistors (2.8 kΩ and 5.6 kΩ) and an external capacitor connected at pin 2 (220 pF).
After demodulation the signal is filtered and then fed into the next stage.

Blanking, colour killer, buffers

As a result of using only one demodulator in SECAM mode the demodulated signal has to be split up in the (B–Y) Channel and the (R–Y) Channel. The unwanted signals occurring every second line, (R–Y) in the (B–Y) Channel and (B–Y) in the (R–Y) Channel, have to be blanked. This happens in the blanking stage by an artificial black level being inserted alternately every second line.
To avoid disturbances during line and field flyback these parts of the colour differential signals are blanked in all modes.
When no signal has been identified, the colour is switched off (signals are blanked) by the colour killer.
At the end of the colour channels are low-ohmic buffers (emitter followers). The CD output signals –(B–Y)* and –(R–Y)* are available at pins 1 and 3.

Identification and system control

The identification part contains three identification demodulators.
The first demodulates in PAL mode. It is only active during the burstkey pulse. The reference signal (f_{sc}) has the (R–Y) phase.
The second demodulator (PLL system) operates in SECAM mode and is active also during the burstkey pulse, but delayed by 2 μs.
The PLL demodulator discriminates the frequency difference between the unmodulated f_0 frequencies of the incoming signal (chr) and the reference frequency input from the crystal oscillator.
These two demodulators are followed by an H/2 switch ‘rectifying’ the demodulated signal. The result is an identification signal (P_{IDT}, pin 13) that is positive for a PAL signal in PAL mode, for a SECAM signal in SECAM mode

and for a PAL signal in NTSC 4.4 mode. If P_{IDT} is positive in SECAM mode, the scanner switches back to the PAL mode in order to prevent a PAL signal being erroneously identified as a SECAM signal (PAL priority).
If then P_{IDT} is not positive, the scanner returns to SECAM mode and remains there if P_{IDT} is positive again. In the event of a field frequency of 60 Hz the signal can not be identified as a SECAM signal, even if P_{IDT} is positive. In this event the scanner switches forward in the NTSC 4.4 mode. If the H/2 signal has the wrong polarity, the identification signal is negative and the H/2 flip-flop is set to the correct phase.
The third demodulator operates in NTSC mode and is active during the burstkey pulse. The resulting identification signal (N_{IDT}, pin 12) is positive for PAL and NTSC 4.4 signals in NTSC 4.4 mode. The reference signal has the (B–Y) phase.
The two identification signals allow an unequivocal identification of the received signal. In the event of a signal being identified, the scanning is stopped and after a delay time the colour is switched on.
The standard outputs (active HIGH) are available at the pins 17, 18 and 19. During scanning the HIGH level is 2.5 V and when a signal has been identified the HIGH level is switched to 6 V. The standard pins can also be used as inputs in order to force the IC into a desired mode (Forced Standard Setting).

Sandcastle detector and pulse processing

In the sandcastle detector the super sandcastle pulse (SC) present at pin 20 is compared with three internal threshold levels by means of three differential amplifiers. The derived signals are the burstkey pulse, the horizontal blanking pulse and the combined horizontal and vertical blanking pulse. These signals are processed into various control pulses required for the timing of the IC.

Bandgap reference

In order to ensure that the CD output signals and the threshold levels of the sandcastle detector are independent of supply voltage variations a bandgap reference voltage has been integrated.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
V_P	supply voltage		–	8.8	V
P_{tot}	power dissipation	without load	–	330	mW
V_{20}	voltage at pin 20	I_{max} = 10 μA	–	15	V
	voltage at all other pins	I_{max} = 100 μA	–	$V_P + v_{be}$	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	thermal resistance on printed-circuit board from junction to ambient in free air (without heat spreader)	
	SO 20	90 K/W
	DIL 20	70 K/W

CHARACTERISTICS

Measured with application circuit (Fig.4) at T_{amb} = +25 °C, 8 V supply, 75% colour bar chrominance input signal of 200 mV (peak-to-peak value) and nominal phase for NTSC unless otherwise specified. All voltages measured referenced to ground.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		7.2	8.0	8.8	V
I	supply current	V_P = 8.0 V without load	25	31	37	mA
P_{tot}	total power dissipation	V_P = 8.0 V without load	–	248	296	mW
CD signals outputs (pins 1 and 3)						
PAL or NTSC						
V_1	colour difference output signals	independent of supply voltage; note 1				
	–(R–Y) output PAL and NTSC 4.43 MHz (peak-to-peak value)		442	525	624	mV
V_3	–(B–Y) output PAL and NTSC 4.43 MHz (peak-to-peak value)		559	665	791	mV
V_1/V_3	ratio of CD signal amplitudes V(R–Y)/V(B–Y)	note 2	0.75	0.79	0.83	–
m	signal linearity –(R–Y) output	V_1 = 0.8 V (p-p)	0.8	–	–	–
	signal linearity –(B–Y) output	V_3 = 1.0 V (p-p)	0.8	–	–	–
f_g	cut-off frequency (both outputs)	–3 dB	–	1	–	MHz
t_d	chrominance delay time		220	270	320	ns
S/N	signal to noise ratio for nominal output voltages	note 3	40	–	–	dB
V_1, V_3	residual carrier at CD outputs 1 × subcarrier frequency (peak-to-peak value)		–	–	10	mV
	2 × subcarrier frequency (peak-to-peak value)		–	–	30	mV
	H/2 content at R–Y output at nominal input signal (peak-to-peak value)		–	–	10	mV
A	crosstalk between CD Channels		–40	–	–	dB
R_1, R_3	output resistance (npn emitter follower)		–	–	200	Ω
I_1, I_3	output current		–	–	–3	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SECAM						
V_1	colour difference output signals	independent of supply voltage; note 4				
	−(R−Y) output (peak-to-peak value)		0.95	1.05	1.15	V
V_3	−(B−Y) output (peak-to-peak value)		1.20	1.33	1.46	V
V_1/V_3	ratio of CD signal amplitudes V(R−Y)/V(B−Y)		0.75	0.79	0.83	–
m	signal linearity at nominal output voltage		0.8	–	–	–
f_g	cut-off frequency	−3 dB	–	730	–	kHz
t_d	chrominance delay time		400	500	600	ns
S/N	signal to noise ratio for 100 mV (p-p) input signal and nominal output voltages	note 3	40	–	–	dB
V_1, V_3	residual carrier at CD outputs: 1 × subcarrier frequency (peak-to-peak value)		–	–	10	mV
	2 × subcarrier frequency (peak-to-peak value)		–	–	20	mV
ΔV_3	shift of demodulated f_0 level relative to blanking level −(B−Y) output	note 8	–	0	±13	mV
ΔV_1	−(R−Y) output		–	0	±10	mV
Impedance and currents see PAL or NTSC specification						
Capacitor for SECAM de-emphasis (pin 2)						
C_2	value of external capacitor		–	220	–	pF
R_A	value of internal de-emphasis resistors	T_{amb} = 35 °C	2.4	2.8	3.2	kΩ
R_B			4.8	5.6	6.4	kΩ
$\Delta(R_A/R_B)$	relative tolerance of de-emphasis resistors		–	–	±5	%
Capacitors for SECAM demodulator control (pins 4 and 8; note 5)						
$\Delta V_{1,3}$	shift of demodulated f_0 level due to external leakage current	C_{ext} = 220 nF	–	–	0.3	mV/nA
Resistor for SECAM oscillator (pin 6)						
V_6	DC voltage		2.4	2.81	3.2	V
R_6	value of external resistor (±1%)		–	5.62	–	kΩ
C_6	value of external capacitor (±20%)		–	10	–	nF
Chrominance input (pin 9)						
V_9	input signal (peak-to-peak value)	note 6	20	200	400	mV
R_9	input resistance		16	20	24	kΩ
C_9	input capacitance		–	–	10	pF
Capacitor for ACC (pin 10; note 7)						
$\Delta V_{1,3}$	change of CD output signals during field blanking due to external leakage current	C_{ext} = 100 nF	–	0.2	–	%/nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Hue control (NTSC) and service switch (pin 11)						
ϕ	phase shift of reference carrier relative to phase at open-circuit pin 11	V_{11} = 3 V	–30	–	–	degree
		V_{11} = open-circuit	–5	0	+5	degree
		V_{11} = 5 V	+30	–	–	degree
V_{11}	internal bias voltage (proportional to supply voltage)	pin 11 open-circuit	3.8	4.0	4.2	V
R_{11}	input resistance		25	30	35	kΩ
Capacitor for identification (pins 12 and 13)						
V_{12}, V_{13}	DC voltage for an identified signal		2.8	3.2	3.5	V
	DC voltage for an unidentified signal		1.5	2.0	2.3	V
PLL oscillator measured with nominal crystal (pin 14; see Table 1)						
R_{14}	initial oscillator amplifier input resistance		–500	–	–	Ω
C_{14}	oscillator amplifier input capacitance		–	–	10	pF
Δf_L	lock-in-range referenced to 4.43361875 MHz	note 9	±400	–	±1300	Hz
ϕ	phase difference for ±400 Hz deviation of colour carrier frequency		–	–	1	degree
2 x f_{sc} output (pin 16; if the output is not used, the pin should be connected to supply)						
V_{16}	DC output level	I_{16} = 0 A	6.1	6.3	6.5	V
R_{16}	output resistance	I_{16} = 0 A	–	–	350	Ω
I_{16}	output current		–	–	–1.0	mA
V_{16}	output signal (peak-to-peak value)		–	250	–	mV
Standard setting inputs/outputs (pins 17 to 19; note 10)						
used as output: npn emitter follower output with 0.1 mA source to ground						
V_O	on-state, during scanning, colour OFF		2.3	2.5	2.7	V
	on-state, colour ON		5.8	6.0	6.2	V
R_O	output resistance	I_O = 0	–	–	300	Ω
I_O	output current		–	–	–3	mA
used as input: forced system switching						
V_O	threshold for system ON		6.8	7.0	7.2	V
I_O	input current		100	150	180	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sandcastle pulse detector (pin 20; note 11)						
C_{20}	input capacitance		–	–	10	pF
V_{20}	thresholds for field and line pulse separation	pulse ON	1.3	1.6	1.9	V
		pulse OFF	1.1	1.4	1.7	V
	line pulse separation	pulse ON	3.3	3.6	3.9	V
		pulse OFF	3.1	3.4	3.7	V
	burst pulse separation	pulse ON	5.3	5.6	5.9	V
		pulse OFF	5.1	5.4	5.7	V
System control processing (note 12)						
t_d	system hold delay	in event of a signal disappearing for a short time	2	–	3	field periods
	colour killer; colour ON delay	switching occurs during field blanking	2	–	3	field periods
	colour OFF delay		0	–	1	field periods
t_s	scanning time for each system		–	4	–	field periods

QUALITY SPECIFICATION: URV-4-2-59/601

Notes to the characteristics

1. Burstkey width 4.3 μs.
   Burst width 2.25 μs, ratio burst chrominance amplitude 1/2.2.
2. At nominal phase of hue control.
3. V (p-p) of signal divided by 6 times effective noise voltage.
4. H/2 blanking alternately every second line.
5. These pins are leakage current sensitive. Pin 4 for (B–Y) Channel, pin 8 for (R–Y) Channel.
6. Within 2 dB output voltage deviation.
7. This pin is leakage current sensitive.
8. IC only.
9. Depends also on network on pin 15.
10. Pin 19 for PAL, pin 18 for SECAM, pin 17 for NTSC 4.43 MHz.
    Threshold levels are dependent of supply.
11. The field interval of the sandcastle has to be adapted to the ICs TDA2579B and TDA4690.
    The thresholds are independent of supply voltage.
12. System scanning sequence: PAL, SECAM, NTSC 4.4.

Table 1 Specification of quartz crystals in HC-49/U13 holder; standard application.

SYMBOL	PARAMETER	VALUE	UNIT
		9922 520 00385	
f_n	nominal frequency	8.867570	MHz
C_L	load capacitance	series resonance	
Δf_n	adjustment tolerance of f_n at +25 °C	±20	ppm
R_r	resonance resistance over temperature range	≤ 60	Ω
$R_{dld\ max}$	in the drive level range between 10^{-12} W and 1.0×10^{-3} W, the resonance resistance may not exceed (at +25 °C) the value of $R_{dld\ max}$	tbn	Ω
R_n	resonance resistance of unwanted response	$2R_{r\ (+25\ °C)}$	Ω
C_1	motional capacitance (±20%)	14.0	fF
C_0	parallel capacitance (±20%)	3.6	pF
T_{amb}	operating ambient temperature	–10 to +60	°C
Δf_n	frequency tolerance over temperature	±20	ppm

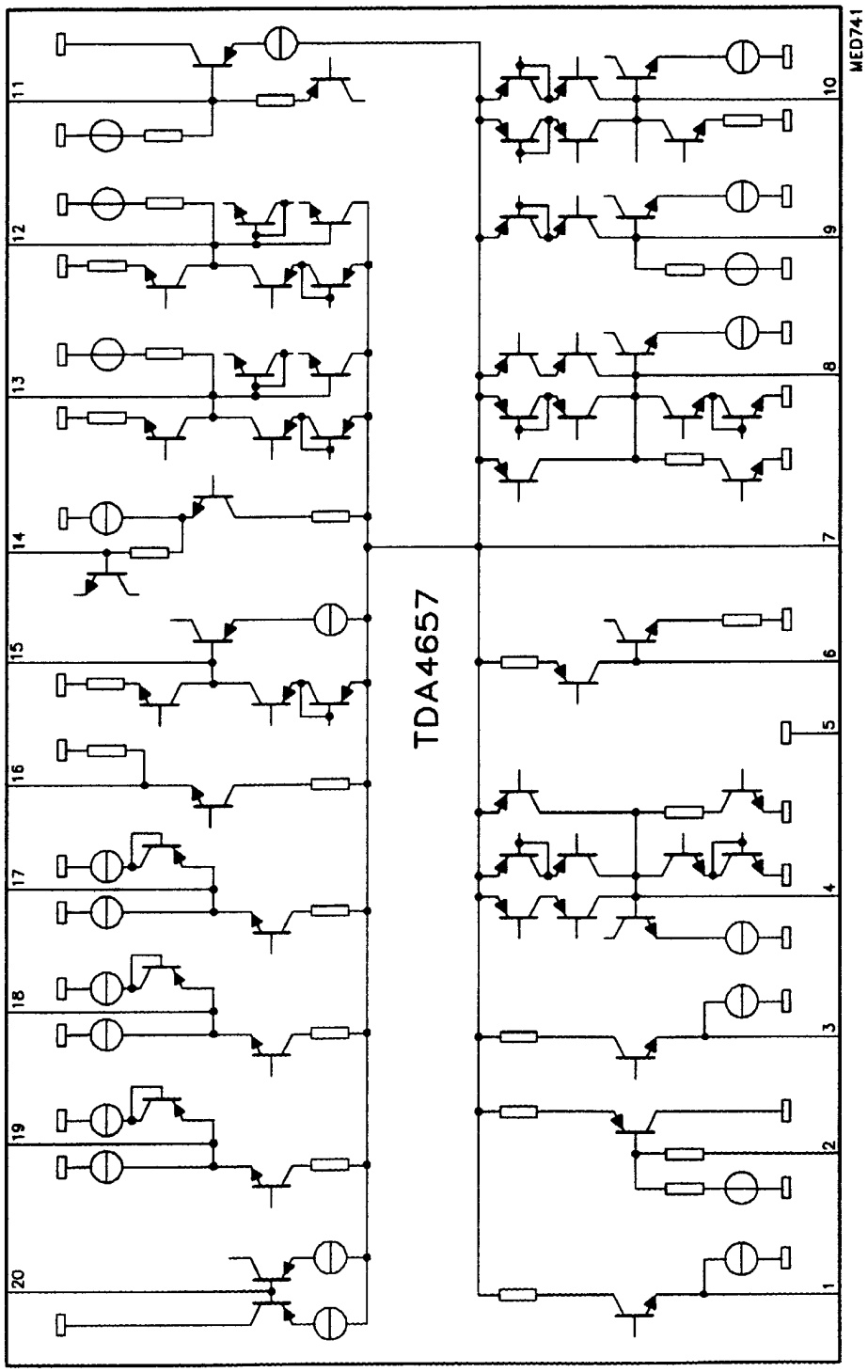


Fig.3 Internal circuits.

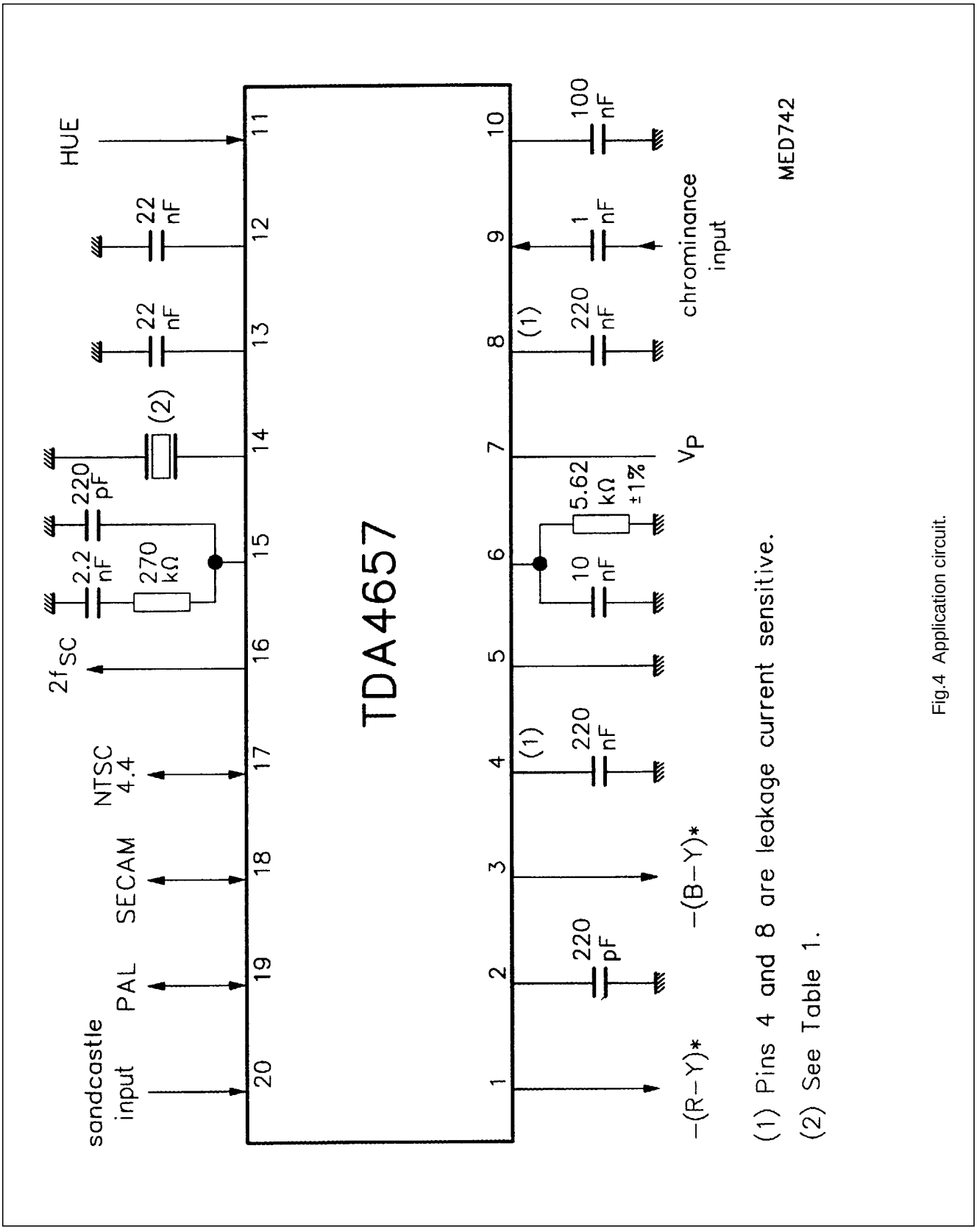
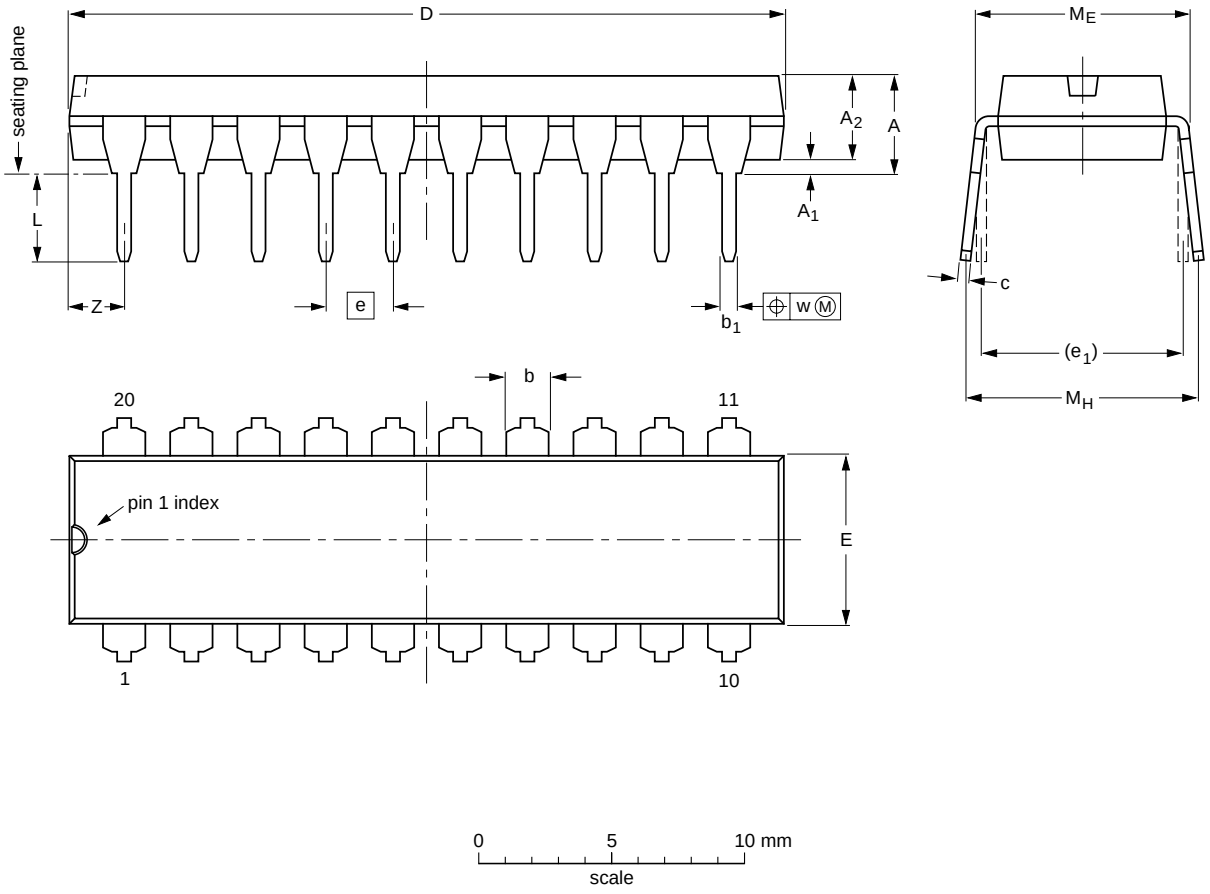


Fig.4 Application circuit.

PACKAGE OUTLINES

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

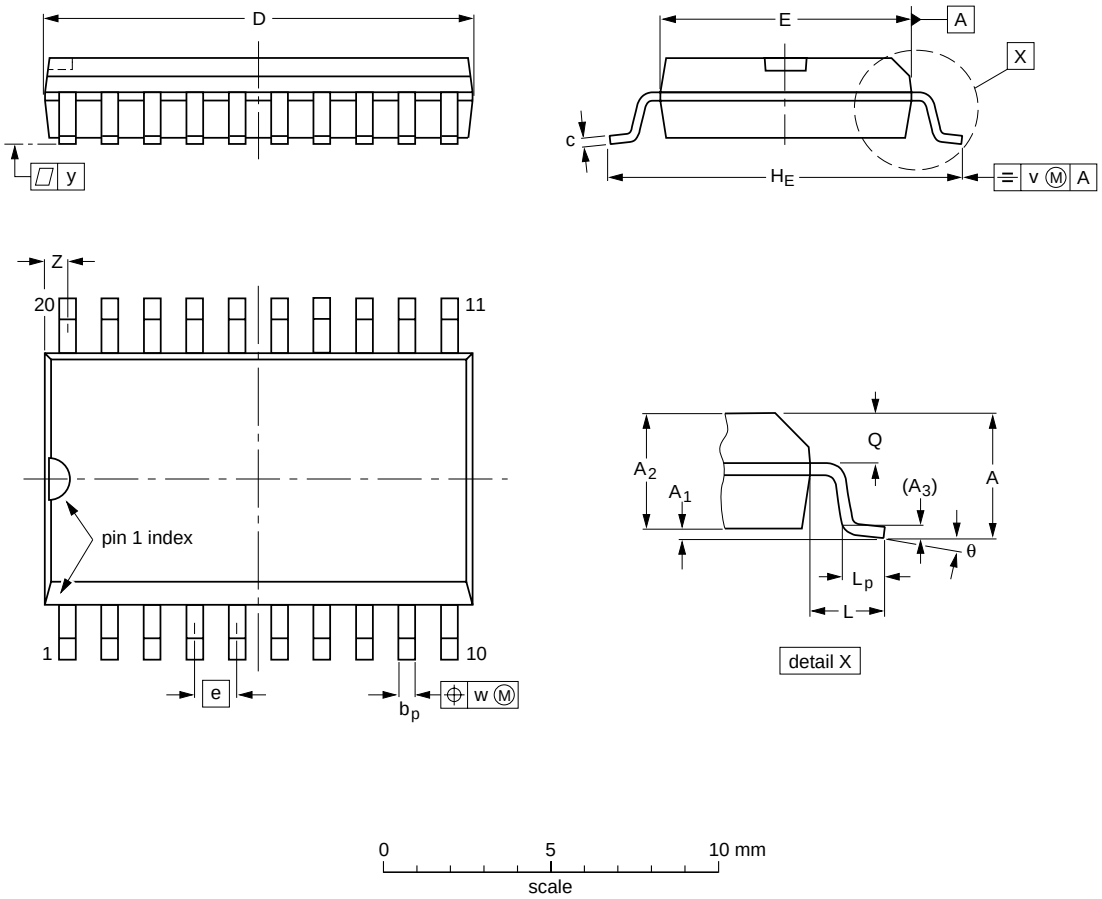
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.