



OPTi Viper Chip Set Level II Cache Module Family

Features

- Pin-compatible secondary cache module family
- Asynchronous (CYM74B550), synchronous pipelined (CYM74P550A), or synchronous burst (CYM74S550, CYM74S551) modules
- Ideal for Intel P54C/P55C systems with the OPTi Viper chipset
- Operates at 50, 60, and 66 MHz
- Uses cost-effective CMOS asynchronous SRAMs or high-performance synchronous SRAMs
- 160-position Burndy DIMM CELP2X80SC3Z48 connector
- 3.3V inputs/ data outputs

Functional Description

This family of secondary cache modules is designed for Intel P54C/P55C systems with the OPTi Viper chip set.

CYM74B550 is a low cost asynchronous cache module that provides 256-Kbytes of cache with industry standard 32Kx8 5

volt SRAMs and 3.3 volt level translators. These modules offer 3-2-2-2 performance at CPU bus speeds up to 66 MHz.

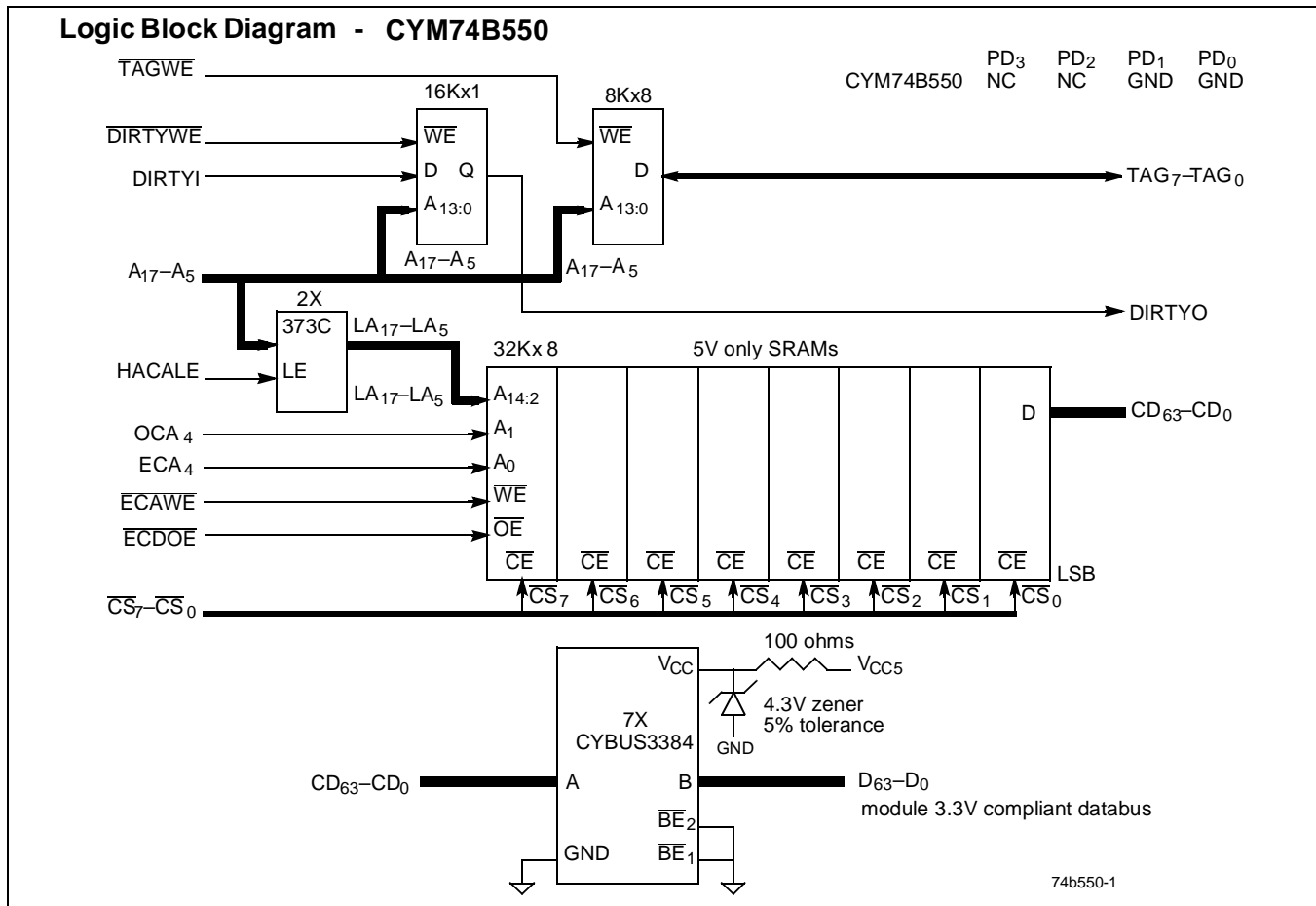
The synchronous modules are available with low cost synchronous pipelined RAMs or high performance synchronous burst RAMs.

The CYM74P550A is a high performance synchronous pipelined burst 256 KB module and is based on industry standard 32Kx32 pipelined BSRAM. The CYM74P550A has series damping resistors on the data lines.

The CYM74S550 and CYM74S551 are high performance synchronous burst cache modules that provide 256-Kbytes and 512-Kbytes of cache respectively. These modules support 3-1-1-1 performance at 66 MHz.

All of these modules include storage for 8-bits of tag and one dirty bit. Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

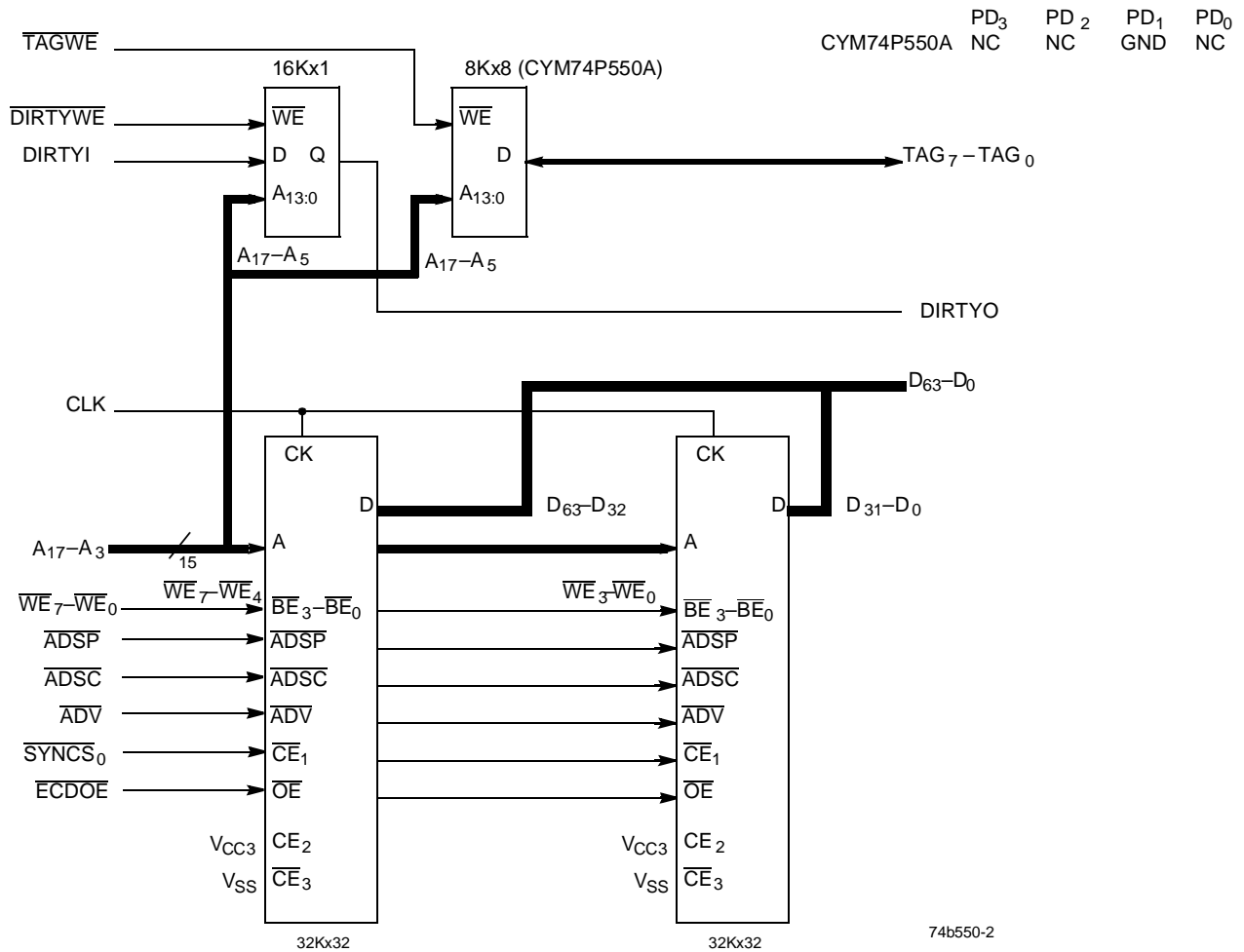
All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The contact pins are plated with 100 micro-inches of nickel covered by 10 micro-inches of gold flash.



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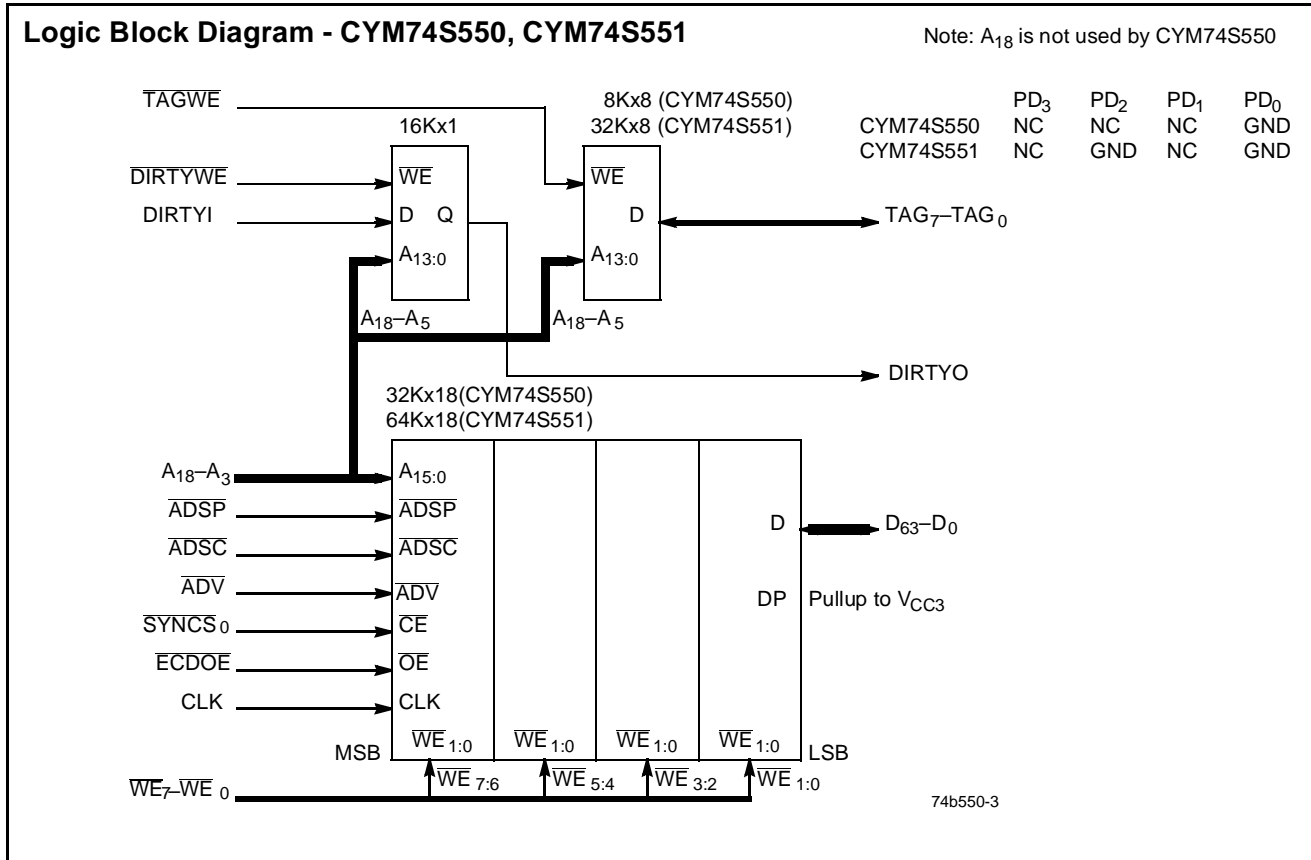
Logic Block Diagram – CYM74P550A





PRELIMINARY

**CYM74B550
CYM74P550A
CYM74S550, CYM74S551**



Selection Guide

Asynchronous Cache Modules			
Part Number	74B550-50	74B550-60	74B550-66
Cache Size	256 KB		
System Clock	50 MHz	60 MHz	66 MHz
Data SRAM t _{AA}	25 ns	15 ns	15 ns
Tag SRAM t _{AA}	20 ns	15 ns	12 ns

Synchronous Pipelined Cache Modules			
Part Number	74P550A-50	74P550A-60	74P550A-66
Cache Size	256 KB		
System Clock	50 MHz	60 MHz	66 MHz
Data SRAM t _{CO}	12 ns	9 ns	9 ns
Tag SRAM t _{AA}	20 ns	15 ns	12 ns

Synchronous Burst Cache Modules						
Part Number	74S550-50	74S550-60	74S550-66	74S551-50	74S551-60	74S551-66
Cache Size	256 KB			512 KB		
System Clock	50 MHz	60 MHz	66 MHz	50 MHz	60 MHz	66 MHz
Data SRAM t _{CO}	12 ns	9 ns	9 ns	12 ns	9 ns	9 ns
Tag SRAM t _{AA}	20 ns	15 ns	12 ns	20 ns	15 ns	12 ns



PRELIMINARY

**CYM74B550
CYM74P550A
CYM74S550, CYM74S551**

Pin Configuration

**Dual Read-Out SIMM (DIMM)
Top View**

GND	81	1	GND
D ₆₃	82	2	D ₆₂
D ₆₁	83	3	D ₆₀
V _{CC5}	84	4	NC (74B550) / V _{CC3} (74P550A, 74S55X)
D ₅₉	85	5	D ₅₈
D ₅₇	86	6	D ₅₆
D ₅₅	87	7	D ₅₄
GND	88	8	GND
D ₅₃	89	9	D ₅₂
D ₅₁	90	10	D ₅₀
D ₄₉	91	11	D ₄₈
V _{CC5}	92	12	NC (74B550) / V _{CC3} (74P550A, 74S55X)
D ₄₇	93	13	D ₄₆
D ₄₅	94	14	D ₄₄
GND	95	15	GND
D ₄₃	96	16	D ₄₂
D ₄₁	97	17	D ₄₀
D ₃₉	98	18	D ₃₈
D ₃₇	99	19	D ₃₆
GND	100	20	GND
D ₃₅	101	21	D ₃₄
D ₃₃	102	22	D ₃₂
D ₃₁	103	23	D ₃₀
D ₂₉	104	24	D ₂₈
GND	105	25	GND
D ₂₇	106	26	D ₂₆
D ₂₅	107	27	D ₂₄
V _{CC5}	108	28	NC (74B550) / V _{CC3} (74P550A, 74S55X)
D ₂₃	109	29	D ₂₂
D ₂₁	110	30	D ₂₀
D ₁₉	111	31	D ₁₈
GND	112	32	GND
D ₁₇	113	33	D ₁₆
D ₁₅	114	34	D ₁₄
D ₁₃	115	35	D ₁₂
GND	116	36	GND
D ₁₁	117	37	D ₁₀
V _{CC5}	118	38	NC (74B550) / V _{CC3} (74P550A, 74S55X)
D ₉	119	39	D ₈
D ₇	120	40	D ₆
GND	121	41	GND
D ₅	122	42	D ₄
V _{CC5}	123	43	NC (74B550) / V _{CC3} (74P550A, 74S55X)
D ₃	124	44	D ₂
D ₁	125	45	D ₀
V _{CC5}	126	46	NC (74B550) / V _{CC3} (74P550A, 74S55X)
(74P550A, 74S55X) \overline{ADSC} / (74B550) \overline{ECA}_4	127	47	\overline{OCA}_4 (74B550) / \overline{ADV} (74P550A, 74S55X)
(74P550A, 74S55X) \overline{SYNC}_{S_0} / (74B550) \overline{ECAWE}	128	48	\overline{OCAWE} (74B550) / \overline{SYNC}_{S_1} (74P550A, 74S55X)
\overline{ECDOE}	129	49	\overline{OCDOE}
(74P550A, 74S55X) \overline{WE}_0 / (74B550) \overline{CS}_0	130	50	\overline{CS}_1 (74B550) / \overline{WE}_1 (74P550A, 74S55X)
GND	131	51	GND
(74P550A, 74S55X) \overline{WE}_2 / (74B550) \overline{CS}_2	132	52	\overline{CS}_3 (74B550) / \overline{WE}_3 (74P550A, 74S55X)
(74P550A, 74S55X) \overline{WE}_4 / (74B550) \overline{CS}_4	133	53	\overline{CS}_5 (74B550) / \overline{WE}_5 (74P550A, 74S55X)
V _{CC5}	134	54	NC (74B550) / V _{CC3} (74P550A, 74S55X)
(74P550A, 74S55X) \overline{WE}_6 / (74B550) \overline{CS}_6	135	55	\overline{CS}_7 (74B550) / \overline{WE}_7 (74P550A, 74S55X)
(74P550A, 74S55X) CLK / (74B550) NC	136	56	HACALE (74B550) / \overline{ADSP} (74P550A, 74S55X)
GND	137	57	GND
$\overline{DIRTYWE}$	138	58	\overline{TAGWE}
(74P550A, 74S55X) A_3 / (74B550) NC	139	59	NC (74B550) / A_4 (74P550A, 74S55X)
A_5	140	60	A_6
A_7	141	61	A_8
GND	142	62	GND
A_9	143	63	A_{10}
A_{11}	144	64	A_{12}
A_{13}	145	65	A_{14}
V _{CC5}	146	66	NC (74B550) / V _{CC3} (74P550A, 74S55X)
A_{15}	147	67	A_{16}
A_{17}	148	68	A_{18}
(Reserved A_{19}) NC	149	69	NC (Reserved A_{20})
GND	150	70	GND
\overline{DIRTYI}	151	71	\overline{DIRTYO}
TAG ₀	152	72	TAG ₁
V _{CC5}	153	73	NC (74B550) / V _{CC3} (74P550A, 74S55X)
TAG ₂	154	74	TAG ₃
TAG ₄	155	75	TAG ₅
GND	156	76	GND
TAG ₆	157	77	TAG ₇
PD ₀	158	78	PD ₁
PD ₂	159	79	PD ₃
V _{CC5}	160	80	NC (74B550) / V _{CC3} (74P550A, 74S55X)

74b550-4



Pin Definitions

Common Signals	Description
V _{CC5}	5V Supply
V _{CC3}	3.3V Supply are CYM74P550A and CYM74S55X only
GND	Ground
A ₁₈ –A ₅	Addresses from processor
D ₆₃ –D ₀	64-bit Data bus from processor
$\overline{E}CDO\overline{E}$	Even bank output enable input
TAG ₇ –TAG ₀	8-bit Tag RAM bidirectional bus
$\overline{T}AGWE$	Tag RAM write enable input
DIRTYI	1-bit Dirty RAM input
DIRTYO	1-bit Dirty RAM output
$\overline{D}IRTYWE$	Dirty RAM write enable input
PD ₃ –PD ₀	Presence Detect pins
NC	Signal not connected on module.
CYM74B550 Only Signals	Description
HACALE	Address Latch Enable input to transparent address latches
OCA ₄	Address bit A ₃ in async cache module (CYM74B550)
ECA ₄	Address bit A ₄ in async cache module (CYM74B550)
$\overline{C}S_7$ – $\overline{C}S_0$	Data RAM Chip Select inputs
$\overline{E}CAWE$	Even bank write enable input
CYM74P550A, CYM74S55X Signals	Description
CLK	Clock input
A ₄ –A ₃	Lower order address bits from processor
$\overline{A}DSC$	Cache Controller Address Strobe input
$\overline{A}DSP$	Processor Address Strobe input
$\overline{A}DV$	Burst Address Advance input
$\overline{S}YNCS_0$	Even bank synchronous burst RAM chip select input
$\overline{S}YNCS_1$	Odd bank synchronous burst RAM chip select input (not used)
$\overline{W}E_7$ – $\overline{W}E_0$	Write enable inputs to Data RAMs

Presence Detect Pins

	PD ₃	PD ₂	PD ₁	PD ₀
Asynchronous - CYM74B550	NC	NC	GND	GND
Sync Pipelined - CYM74P550A	NC	NC	GND	NC
Synch Burst - CYM74S550	NC	NC	NC	GND
Synch Burst - CYM74S551	NC	GND	NC	GND



PRELIMINARY

**CYM74B550
CYM74P550A
CYM74S550, CYM74S551**

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -55°C to +125°C
 Ambient Temperature
 with Power Applied -0°C to +70°C
 3.3V Supply Voltage to Ground Potential..... -0.5V to +4.6V
 5V Supply Voltage to Ground Potential..... -0.5V to +7.0V
 DC Voltage Applied to Outputs
 in High Z State -0.5V to +4.6V

DC Input Voltage -0.5V to +4.6V
 Output Current into Outputs (LOW)..... 20 mA

Operating Range

Range	Ambient Temperature	V _{CC5}	V _{CC3}
Commercial (CYM74B550)	0°C to +70°C	5V ± 5%	N/A
Commercial (CYM74P550A, CYM74S55X)	0°C to +70°C	5V ± 5%	3.3V +10%– 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V _{IH}	Input HIGH Voltage		2.2		V
V _{IL}	Input LOW Voltage	CYM74B550	-0.5	0.8	V
V _{IL}	Input LOW Voltage	CYM74P550A, CYM74S55X	-0.3	0.8	V
V _{OH}	Output HIGH Voltage	V _{CC3} =Min. I _{OH} = -4 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC3} =Min. I _{OL} = 8 mA		0.4	V
I _{CC} (74B550)	Operating Supply Current	V _{CC5} =Max., I _{OUT} =0 mA, f=f _{MAX}		1650	mA
I _{CC} (74P550A)	Operating Supply Current	V _{CC5} =Max., V _{CC3} =Max., I _{OUT} =0 mA, f=f _{MAX}		900	mA
I _{CC} (74S550)	Operating Supply Current	V _{CC5} =Max., V _{CC3} =Max., I _{OUT} =0 mA, f=f _{MAX}		1500	mA
I _{CC} (74S551)	Operating Supply Current	V _{CC5} =Max., V _{CC3} =Max., I _{OUT} =0 mA, f=f _{MAX}		1500	mA

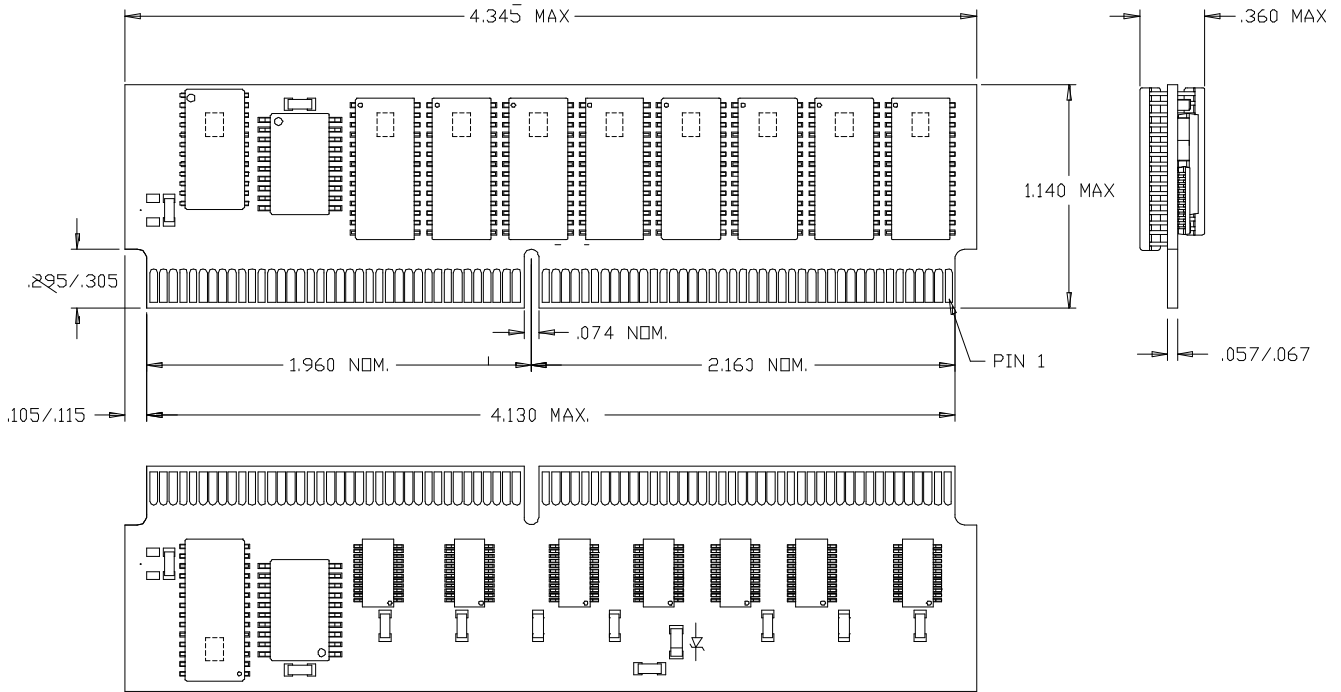
Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
50	CYM74B550PM-50C	PM35	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74P550APM-50C	PM42		Sync Pipelined 256 KB	
	CYM74S550PM-50C	PM33		Sync Burst 256 KB	
	CYM74S551PM-50C			Sync Burst 512 KB	
60	CYM74B550PM-60C	PM35	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74P550APM-60C	PM42		Sync Pipelined 256 KB	
	CYM74S550PM-60C	PM33		Sync Burst 256 KB	
	CYM74S551PM-60C			Sync Burst 512 KB	
66	CYM74B550PM-66C	PM35	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74P550APM-66C	PM42		Sync Pipelined 256 KB	
	CYM74S550PM-66C	PM33		Sync Burst 256 KB	
	CYM74S551PM-66C	PM33		Sync Burst 512 KB	

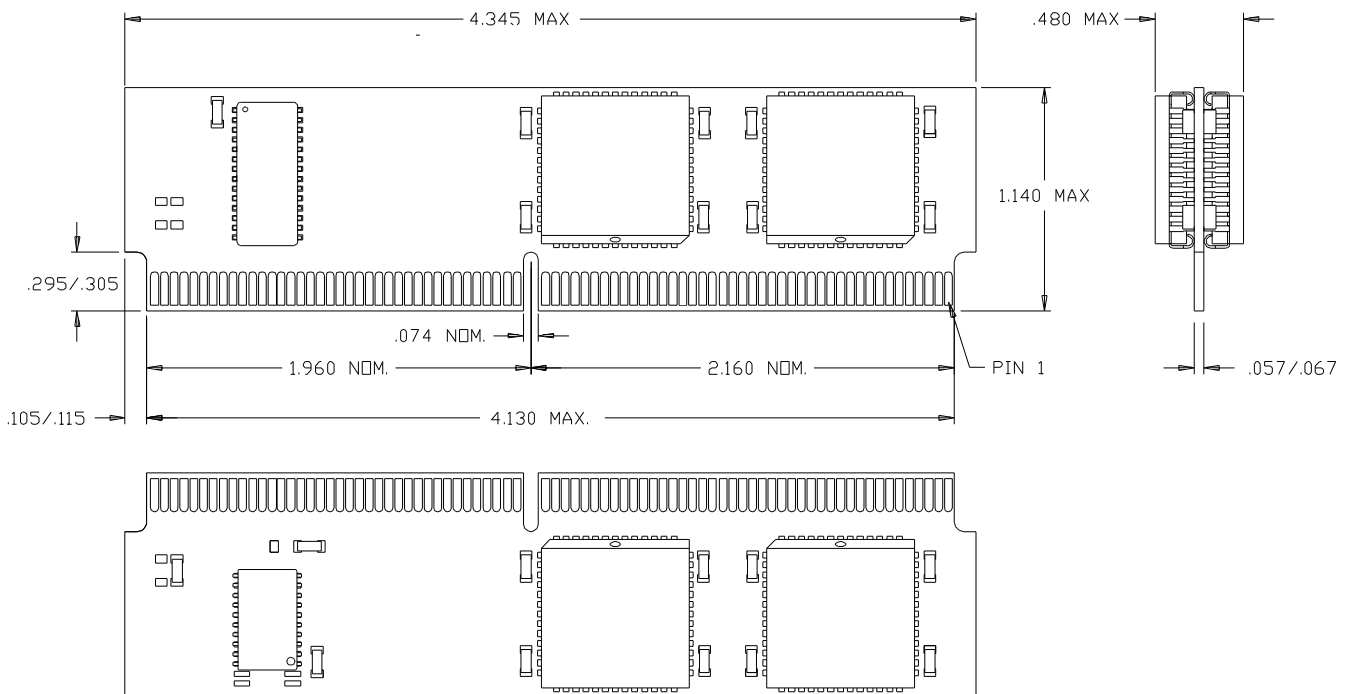
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Package Diagrams

160-Pin Dual Readout SIMM (PM35)



160-Pin Dual Readout SIMM (PM33)



Package Diagrams (continued)

160-Pin Dual Readout SIMM (PM42)

