

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4724B

MSI

8-bit addressable latch

Product specification
File under Integrated Circuits, IC04

January 1995

8-bit addressable latch

HEF4724B

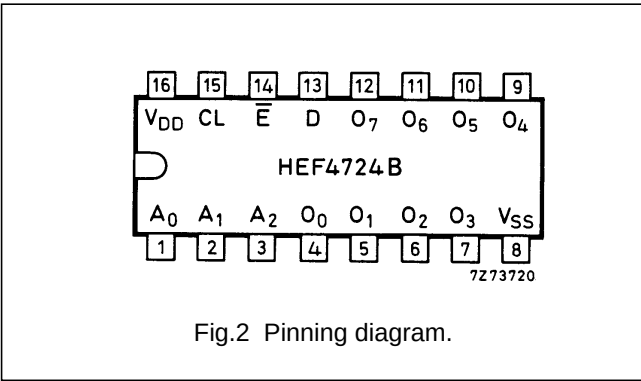
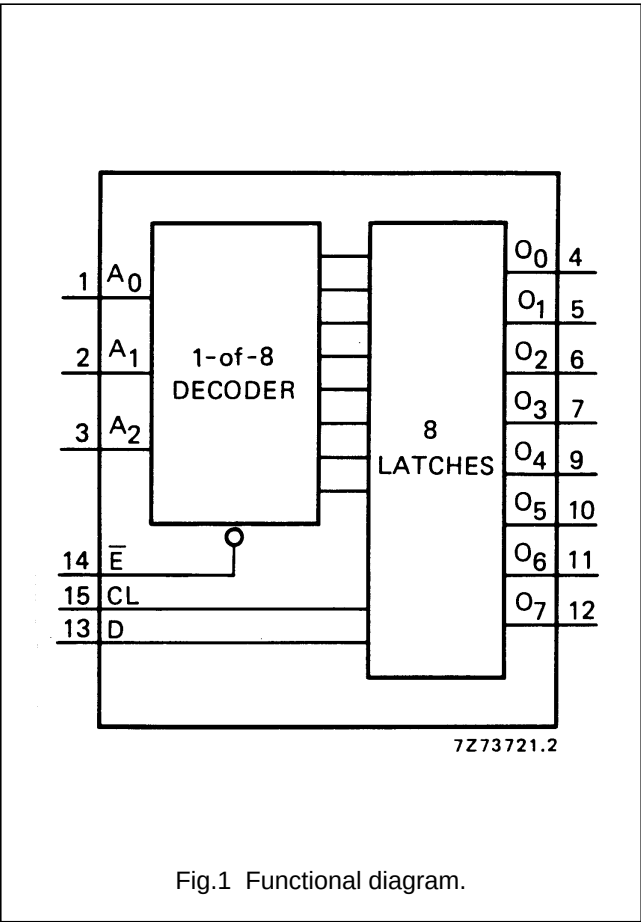
MSI

DESCRIPTION

The HEF4724B is an 8-bit addressable latch with three address inputs (A_0 to A_2), a data input (D), an active LOW enable input ($\overline{E}$), an active HIGH clear input (CL), and eight parallel latch outputs (O_0 to O_7).

When $\overline{E}$ and CL are HIGH, all outputs (O_0 to O_7) are LOW. Eight-channel demultiplexing or active HIGH 1-of-8 decoding with output enable operation occurs when CL is HIGH and $\overline{E}$ is LOW. When CL and $\overline{E}$ are LOW, the

selected output (O_0 to O_7 ; determined by A_0 to A_2) follows D . When $\overline{E}$ goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\overline{E} = CL = \text{LOW}$), changing more than one bit of A_0 to A_2 could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\overline{E} = \text{HIGH}$, $CL = \text{LOW}$).



- HEF4724BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4724BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4724BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

PINNING

- A_0 to A_2 address inputs
- A data input
- $\overline{E}$ enable input (active LOW)
- CL clear input (active HIGH)
- O_0 to O_7 parallel latch outputs

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

8-bit addressable latch

HEF4724B
MSI

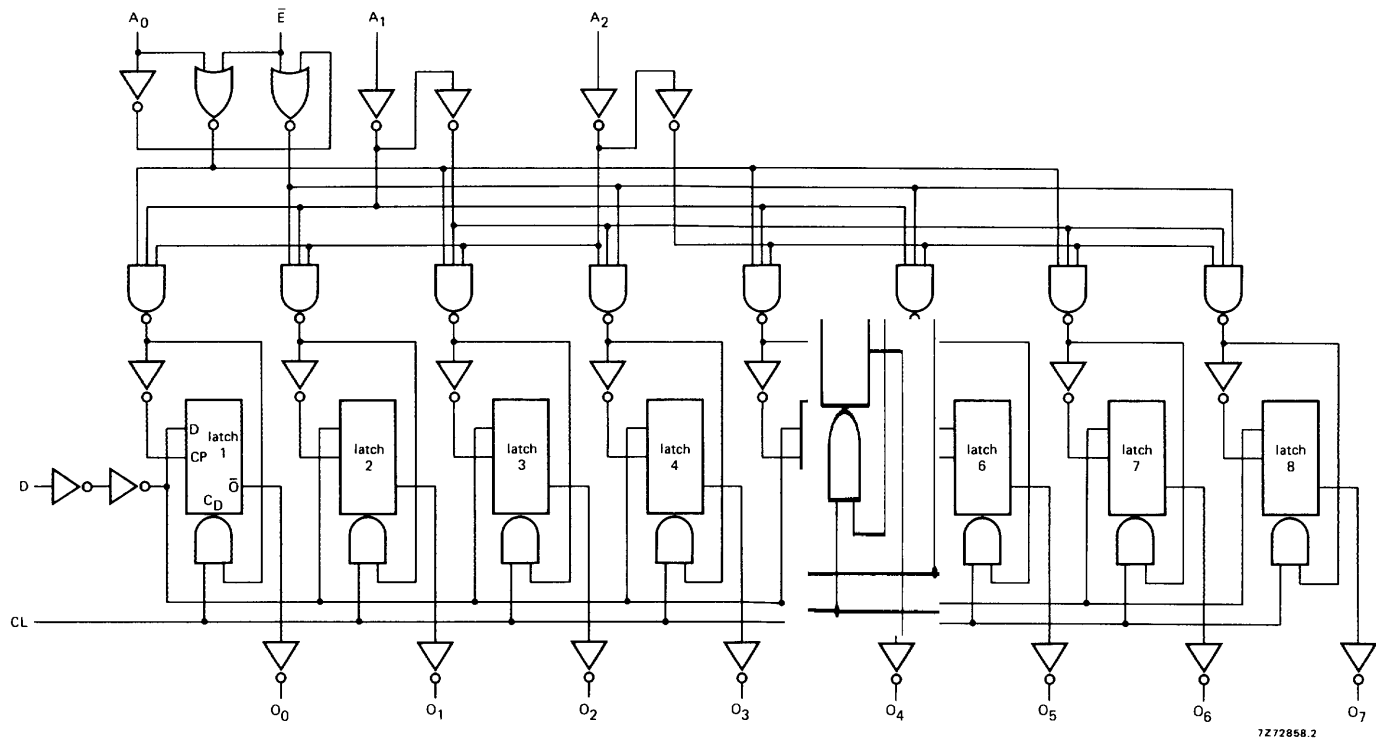


Fig.3 Logic diagram.

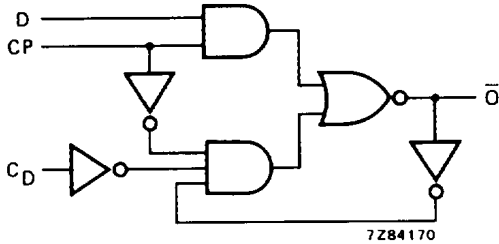


Fig.4 Logic diagram (one latch).

8-bit addressable latch

HEF4724B
MSI

MODE SELECTION

$\bar{E}$	CL	MODE
L	L	addressable latch
H	L	memory
L	H	active HIGH 8-channel demultiplexer
H	H	clear

FUNCTION TABLE

CL	$\bar{E}$	D	A ₀	A ₁	A ₂	O ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇	MODE
H	H	X	X	X	X	L	L	L	L	L	L	L	L	clear
H	L	D ₁	L	L	L	D ₁	L	L	L	L	L	L	L	demultiplexer; unaddressed latch is cleared
H	L	D ₁	H	L	L	L	D ₁	L	L	L	L	L	L	
H	L	D ₁	L	H	L	L	L	D ₁	L	L	L	L	L	
H	L	D ₁	H	H	L	L	L	L	D ₁	L	L	L	L	
H	L	D ₁	L	L	H	L	L	L	L	D ₁	L	L	L	
H	L	D ₁	H	L	H	L	L	L	L	L	D ₁	L	L	
H	L	D ₁	L	H	H	L	L	L	L	L	L	D ₁	L	
H	L	D ₁	H	H	H	L	L	L	L	L	L	L	D ₁	
L	H	X	X	X	X	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	memory
L	L	D ₁	L	L	L	D ₁	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	addressable latch; unaddressed latch holds previous state
L	L	D ₁	H	L	L	O _{n-1}	D ₁	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	
L	L	D ₁	L	H	L	O _{n-1}	O _{n-1}	D ₁	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	
L	L	D ₁	H	H	L	O _{n-1}	O _{n-1}	O _{n-1}	D ₁	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	
L	L	D ₁	L	L	H	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	D ₁	O _{n-1}	O _{n-1}	O _{n-1}	
L	L	D ₁	H	L	H	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	D ₁	O _{n-1}	O _{n-1}	
L	L	D ₁	L	H	H	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	D ₁	O _{n-1}	
L	L	D ₁	H	H	H	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	D ₁	

Notes

1. H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
O_{n-1} = state before the positive transition of $\bar{E}$
D₁ = either HIGH or LOW

8-bit addressable latch

HEF4724B
MSI

AC CHARACTERISTICS

 $V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ≤ 20 ns

	V_{DD} V	TYPICAL FORMULA FOR P (μ W)	
Dynamic power dissipation per package (P)	5 10 15	$700 f_i + \sum (f_o C_L) \times V_{DD}^2$ $3700 f_i + \sum (f_o C_L) \times V_{DD}^2$ $10\,800 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)

AC CHARACTERISTICS

 $V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays							
$\bar{E} \rightarrow O_n$	5			115	230	ns	88 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		50	95	ns	39 ns + (0,23 ns/pF) C _L
	15			35	70	ns	27 ns + (0,16 ns/pF) C _L
LOW to HIGH	5			95	195	ns	68 ns + (0,55 ns/pF) C _L
	10	t _{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C _L
	15			30	55	ns	22 ns + (0,16 ns/pF) C _L
D → O _n	5			95	190	ns	68 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		35	75	ns	24 ns + (0,23 ns/pF) C _L
	15			25	55	ns	17 ns + (0,16 ns/pF) C _L
LOW to HIGH	5			85	170	ns	58 ns + (0,55 ns/pF) C _L
	10	t _{PLH}		35	75	ns	24 ns + (0,23 ns/pF) C _L
	15			25	55	ns	17 ns + (0,16 ns/pF) C _L
A _n → O _n	5			110	225	ns	83 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		45	95	ns	34 ns + (0,23 ns/pF) C _L
	15			35	70	ns	27 ns + (0,16 ns/pF) C _L
LOW to HIGH	5			95	190	ns	68 ns + (0,55 ns/pF) C _L
	10	t _{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C _L
	15			30	55	ns	22 ns + (0,16 ns/pF) C _L
CL → O _n	5			85	165	ns	58 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		35	70	ns	24 ns + (0,23 ns/pF) C _L
	15			25	50	ns	17 ns + (0,16 ns/pF) C _L

8-bit addressable latch

HEF4724B
MSI

	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Set-up times D → $\bar{E}$	5	t _{su}	40	20	ns	see also waveforms Fig.5
	10		15	5	ns	
	15		10	0	ns	
	5	t _{su}	40	20	ns	
	10		20	10	ns	
	15		15	5	ns	
Hold times D → $\bar{E}$	5	t _{hold}	20	0	ns	
	10		15	5	ns	
	15		15	5	ns	
	5	t _{hold}	50	25	ns	
	10		20	10	ns	
	15		15	5	ns	
Minimum $\bar{E}$ pulse width; LOW	5	t _{WEL}	75	35	ns	
	10		30	15	ns	
	15		20	10	ns	
Minimum CL pulse width; HIGH	5	t _{WCLH}	70	35	ns	
	10		30	15	ns	
	15		20	10	ns	

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Output transition times	5	t _{THL}		60	120 ns	10 ns + (1,0 ns/pF) C _L
HIGH to LOW	10			30	60 ns	9 ns + (0,42 ns/pF) C _L
	15			20	40 ns	6 ns + (0,28 ns/pF) C _L
LOW to HIGH	5	t _{TLH}		60	120 ns	10 ns + (1,0 ns/pF) C _L
	10			30	60 ns	9 ns + (0,42 ns/pF) C _L
	15			20	40 ns	6 ns + (0,28 ns/pF) C _L