HM674100H Series

1,048,576-word × 4-bit High Speed Static Random Access Memory

HITACHI

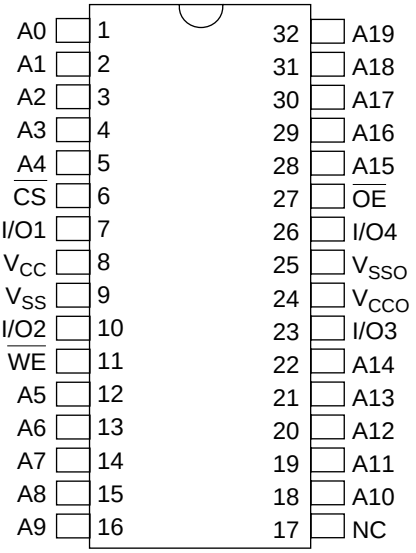
Features

- 1,048,576-word × 4-bit organization.
- Directly TTL compatible input and output.
- +5 V Single supply.
- Completely static memory.
- No clock or timing strobe required.
- Super fast access time: 15/20/25 ns (max).
- Revolutional pin arrangement.

Ordering Information

Type No.	Access Time	Package
HM674100HJP-15	15 ns	400 mil 32 pin plastic SOJ (CP-32DB)
HM674100HJP-20	20 ns	
HM674100HJP-25	25 ns	

Pin Arrangement

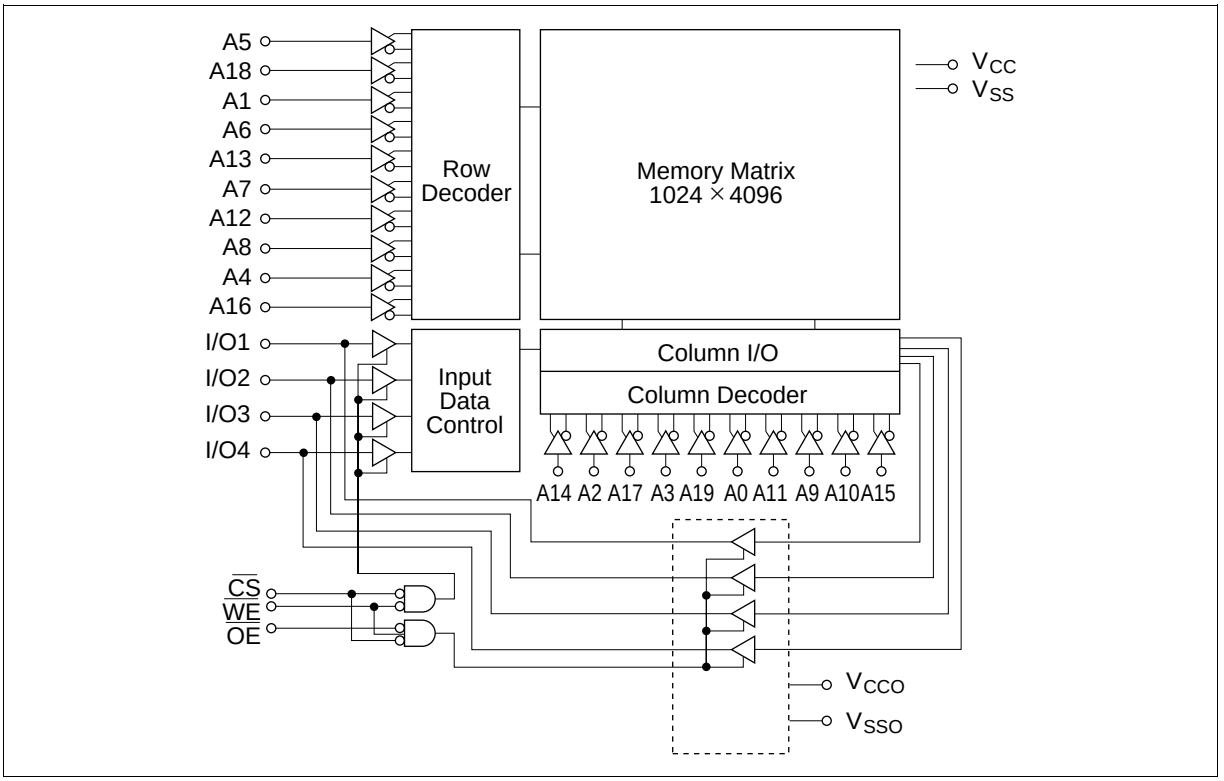


(Top View)

Pin Description

Pin Name	Function
A0 to A19	Address input
I/O1 to I/O4	input/output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
V_{cc}	+5 V Power supply
V_{cco}	Output buffer power supply
V_{sso}	Output buffer ground
V_{ss}	Ground
NC	Not connect

Block Diagram



Function Table

Input

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Ref. Cycle
H	X	X	Not selected	High-Z	I_{SB}, I_{SB1}	—
L	H	H	Output disabled	High-Z	I_{CC}, I_{CC1}	—
L	H	L	Read	Data Out	I_{CC}, I_{CC1}	Read Cycle (1), (2), (3)
L	L	H	Write	Data In	I_{CC}, I_{CC1}	Write Cycle (1), (2), (3), (4)
L	L	L	Write	Data In	I_{CC}, I_{CC1}	Write Cycle (5), (6)

Note: X: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage[*1]	V_{CC}	–0.5 to +7.0	V
Voltage on any pin relative to V_{SS}[*1]	V_T	–0.5 to V_{CC} + 0.5	V
Power dissipation	P_T	1.0/1.5[*2]	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg (Bias)	–10 to +85	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1 With respect to $V_{SS} = V_{SSO}$

2 P_T = 1.5 W is guaranteed under the minimum air flow exceeding 500 linear feet per minute. Under the DC and AC specifications shown in the Tables, this device is tested under the minimum transverse air flow exceeding 500 linear feet per minute.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}, V_{CCO}	4.5	5.0	5.5	V
	V_{SS}, V_{SSO}	0.0	0.0	0.0	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input low voltage	V_{IL}	–0.5	—	0.8	V

DC Characteristics (V_{CC} = V_{CCO} = 5.0 V ±10%, V_{SS} = V_{SSO} = 0 V, Ta = 0 to +70°C)

		HM674100H							
		-15		-20		-25			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Input leakage current	$\|I_{LI}\|$	—	2	—	2	—	2	µA	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	10	—	10	—	10	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $\overline{WE}$ = V_{IL} $V_{I/O}$ = 0 V to V_{CC}
Operating power supply current	I_{CC}	—	120	—	120	—	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
Average operating current	I_{CC1}	—	220	—	200	—	160	mA	min cycle, $I_{I/O}$ = 0 mA
Standby power supply current	I_{SB}	—	100	—	80	—	60	mA	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}
	I_{SB1}	—	10	—	10	—	10	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = –4 mA

Capacitance (Ta = 25°C, f = 1 MHz)

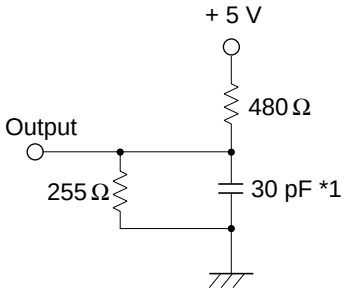
Parameter	**Symbol**	**Max**	**Unit**	**Test Conditions**
Input capacitance	C_{IN} *1	6	pF	V_{IN} = 0 V
Input/Output capacitance	$C_{I/O}$ *1	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

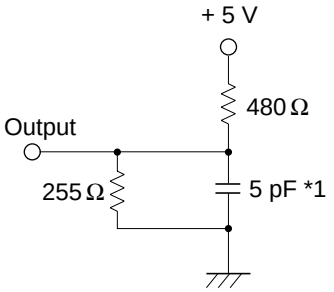
AC Characteristics (V_{CC} = V_{CCO} = 5 V ± 10%, V_{SS} = V_{SSO} = 0 V, Ta = 0 to +70°C, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5V
- Input rise and fall time: 4 ns
- Output reference levels: 1.5 V
- Output Load: See figure



Output Load A



Output Load B

(for t_{HZ}, t_{LZ}, t_{OHZ}, t_{OLZ}, t_{WZ}, & t_{OW})

Note: including scope and jig capacitance

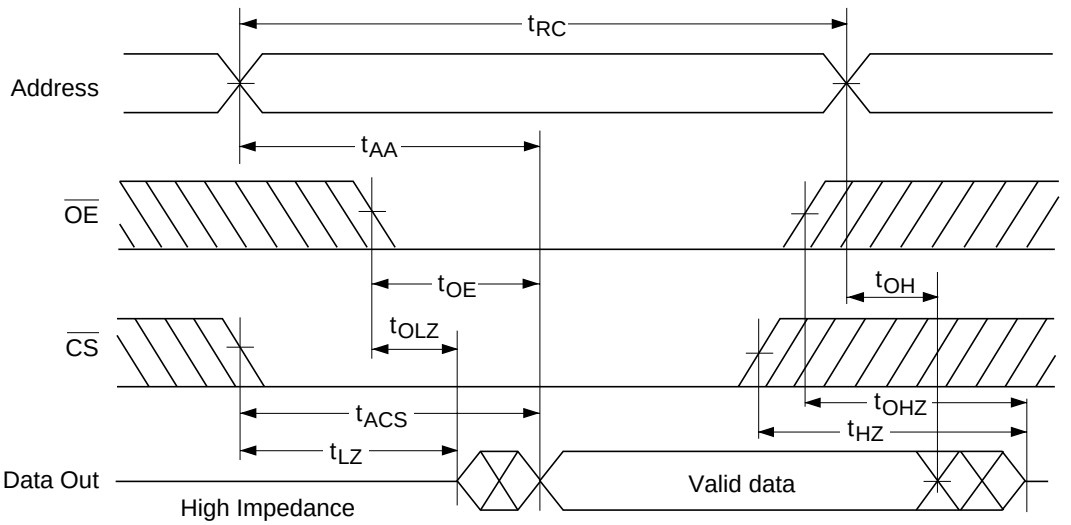
Read Cycle

		HM674100H						
		-15		-20		-25		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read cycle time	t_{RC}	15	—	20	—	25	—	ns
Address access time	t_{AA}	—	15	—	20	—	25	ns
Chip select access time	t_{ACS}	—	15	—	20	—	25	ns
Chip selection to output in low-Z	t_{LZ} *1,*2	5	—	5	—	5	—	ns
Output enable to output Valid	t_{OE}	—	8	—	10	—	15	ns
Output enable to output in low-Z	t_{OLZ} *1,*2	2	—	2	—	2	—	ns
Chip deselection to output in high-Z	t_{HZ} *1,*2	0	7	0	8	0	15	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns

Notes: 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

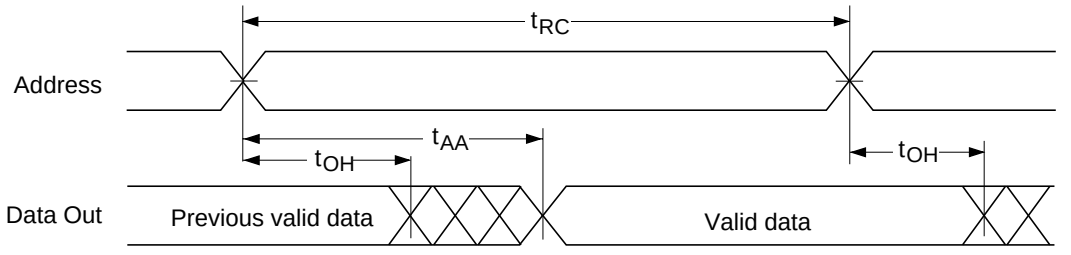
Timing Waveforms

Read Cycle-1



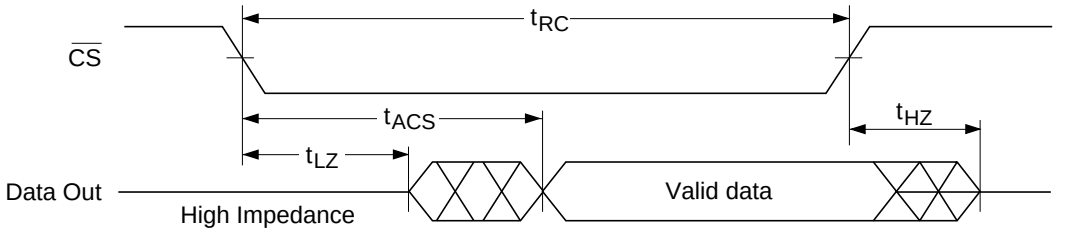
Note: 1. $\overline{WE}$ = V_{IH}

Read Cycle-2



Note: 1. $\overline{WE}$ = V_{IH}
2. $\overline{CS}$ = V_{IL}
3. $\overline{OE}$ = V_{IL}

Read Cycle-3



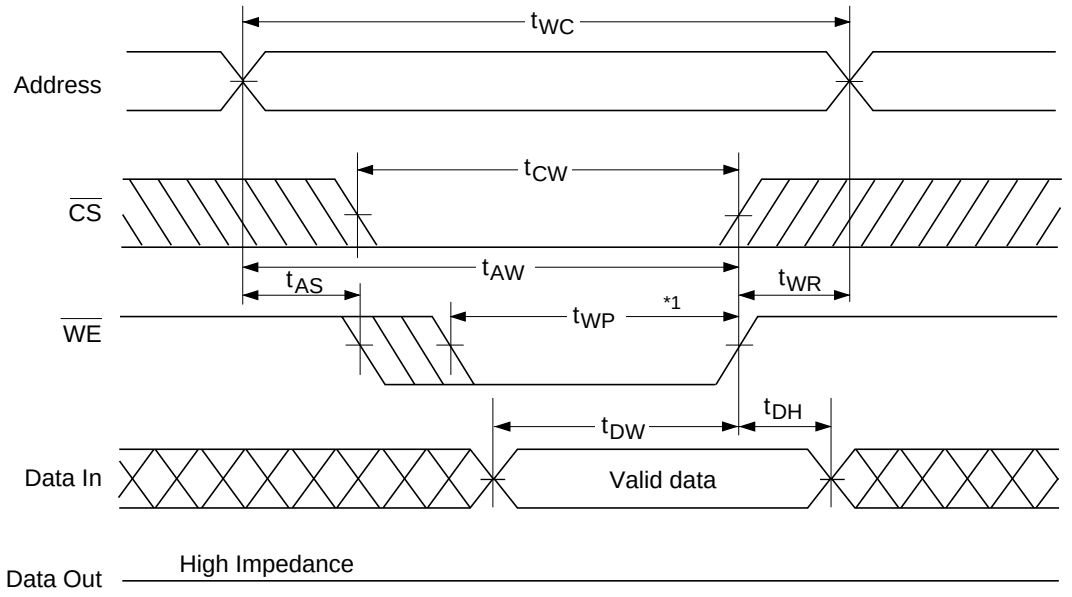
Note: 1. $\overline{WE} = V_{IH}$
2. $\overline{OE} = V_{IL}$
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

		HM674100H						
		-15		-20		-25		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC} *1	15	—	20	—	25	—	ns
Chip selection to end of write	t_{CW}	12	—	15	—	17	—	ns
Address valid to end of write	t_{AW}	12	—	15	—	17	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	12	—	15	—	17	—	ns
Write recovery time	t_{WR}	3	—	3	—	3	—	ns
Data valid to end of write	t_{DW}	8	—	10	—	15	—	ns
Data hold time	t_{DH}	0	—	0	—	0	—	ns
Write enable to output in high Z	t_{WZ} *2, *3	0	7	0	8	0	12	ns
Output disable to output in high Z	t_{OHZ} *2, *3	0	7	0	8	0	10	ns
Output active from end of write	t_{OW} *2, *3	2	—	2	—	2	—	ns

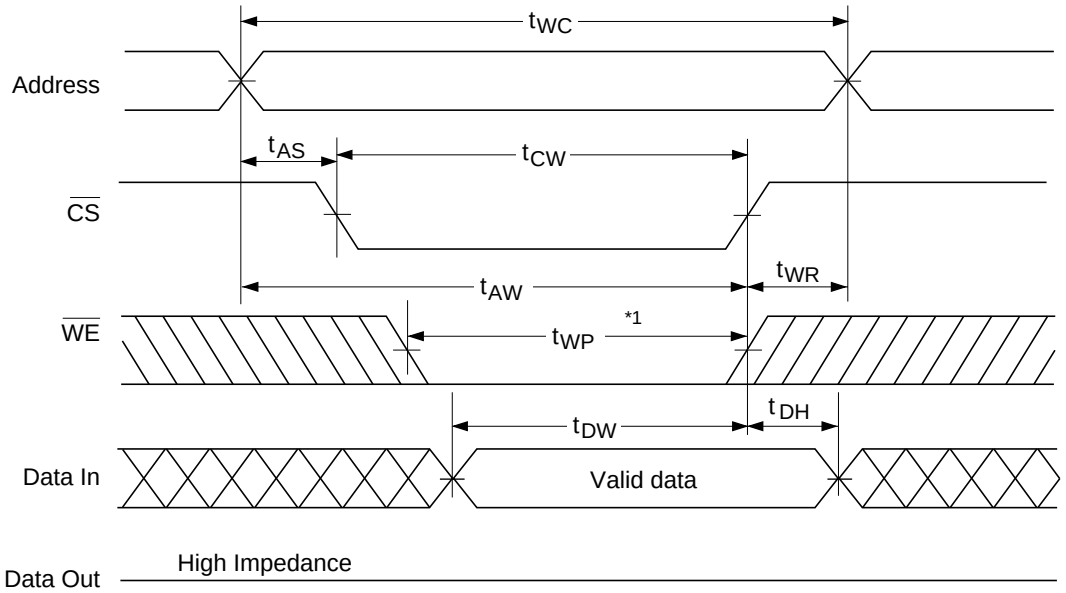
Notes: 1. All write cycle timings are referred from the last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

Write Cycle-1 ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



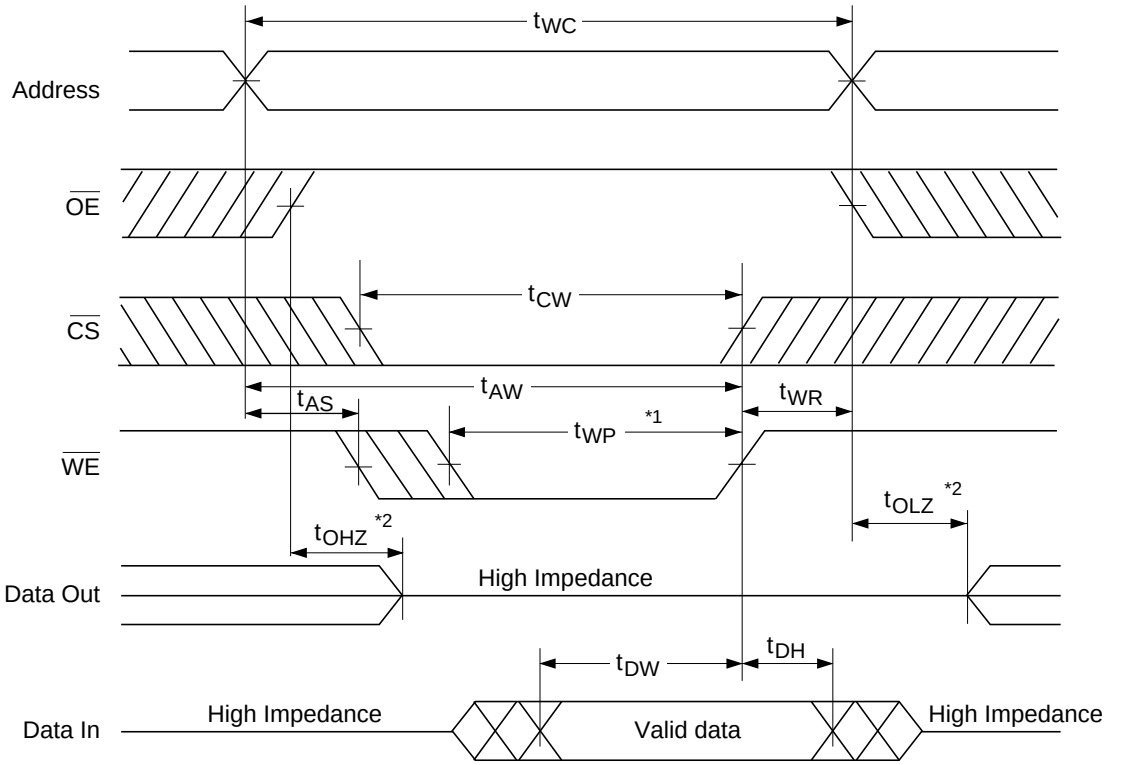
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle-2 ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



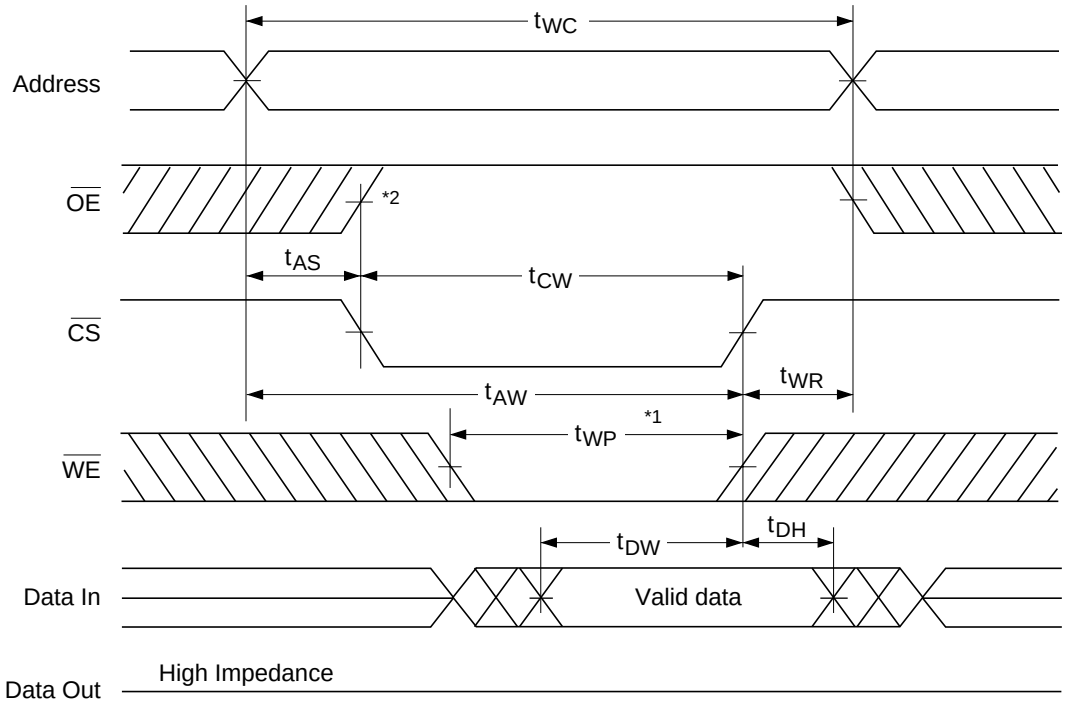
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle-3 ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



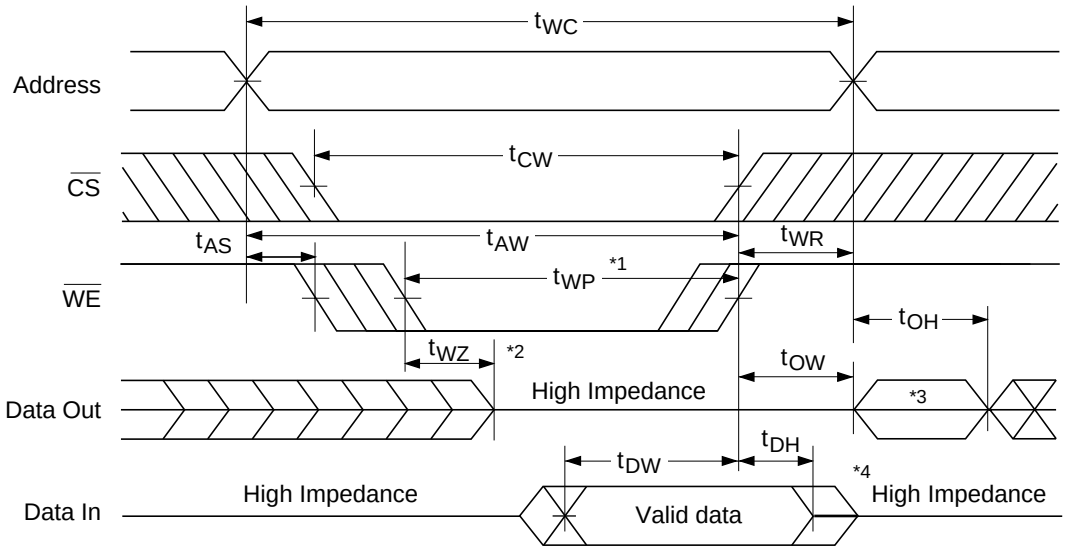
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

Write Cycle-4 ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



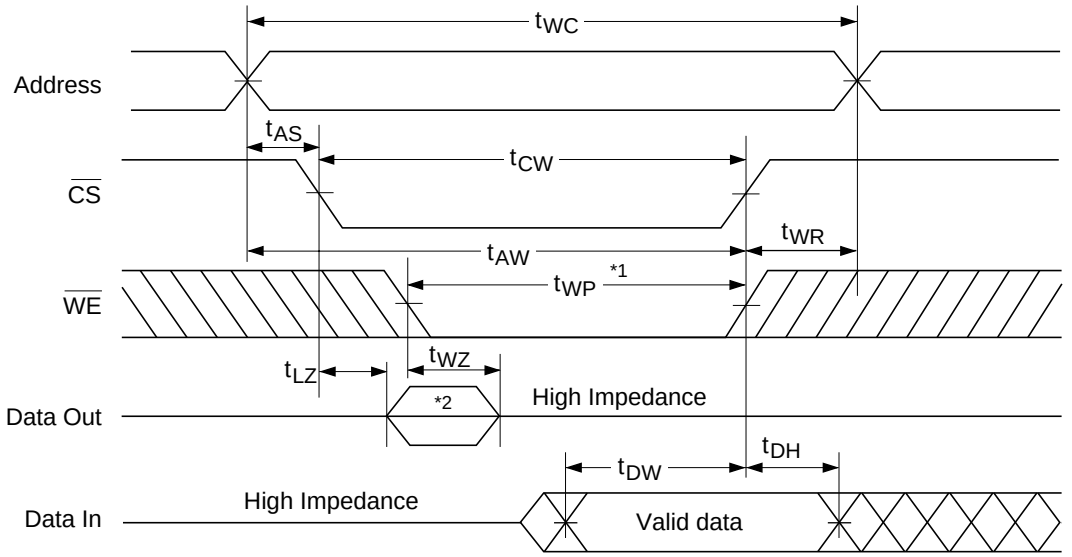
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in a high impedance state.

Write Cycle-5 ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied them.

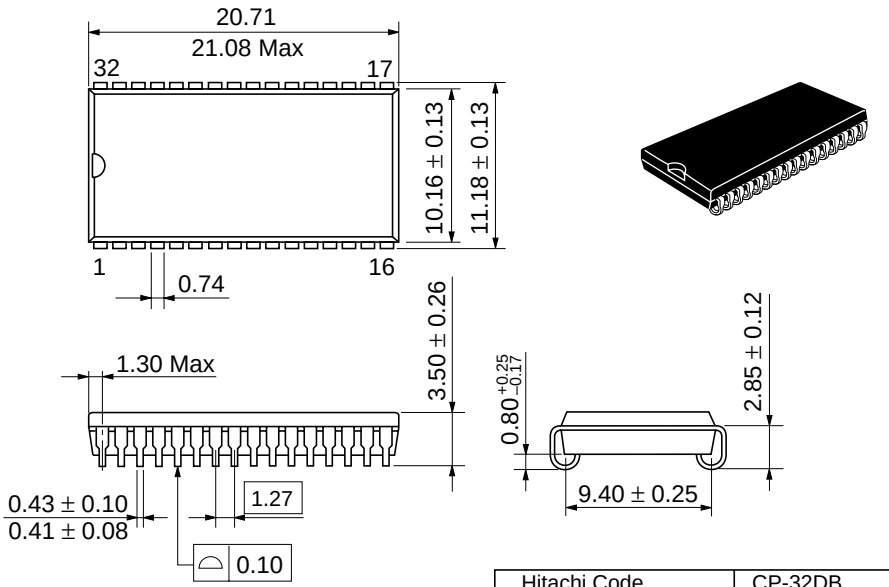
Write Cycle-6 ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

Package Dimension

HM674100HJP Series (CP-32DB) Unit: mm



Hitachi Code	CP-32DB
JEDEC Code	MO-061-AB
EIAJ Code	SC-638
Weight	1.2 g

HM674100HJP -15, -20, -25 400 mil 32 pin plastic SOJ (CP-32DB) — Mechanical