MOTOROLA
Semiconductor Products Sector
Technical Data

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Addendum to MC68HC908LD64 Technical Data

This addendum provides corrections to:

MC68HC908LD64 Technical Data
(Motorola document number MC68HC908LD64/D Rev. 2.0)

Page 278: Correct WRDY description under **18.7.2 OSD Status Register**.

From: WRDY — OSD Buffer Write Ready

This bit is set when the OSD data registers $0062 and $0063, are ready to be loaded with new data. The WRDY is cleared after the CPU writes to the high byte register, $0063. It becomes set again when the OSD circuitry has transferred the content of data registers to the OSD RAM. Reset sets this bit.

1 = OSD data buffers ready for new data
0 = OSD data buffers busy

To: WRDY — OSD Buffer Write Ready

This bit is set when the OSD data registers $0062 and $0063, are ready to be loaded with new data. The WRDY is cleared after the CPU writes to the low byte register, $0062. It becomes set again when the OSD circuitry has transferred the content of data registers to the display RAM. Reset sets this bit.

1 = OSD data buffers ready for new data
0 = OSD data buffers busy

Page 279: Correct OSDD[15:0] description under **18.7.3 OSD Data Registers**.

From: OSDD[15:0] — OSD RAM 16-Bit Data Buffer

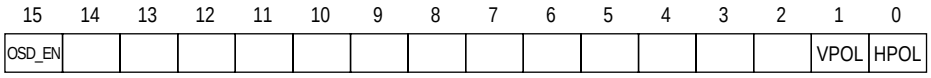
These bits store the data which is going to be written into the OSD RAM when OSDMEN is set. While OSD circuitry is displaying data from the display RAM, updates to the display RAM is made by writing to the OSD row and column address registers and this 8-bit pair data registers. The OSD buffer write ready bit, WRDY, will be cleared after the write to the high byte register, $0063.

To: OSDD[15:0] — OSD RAM 16-Bit Data Buffer

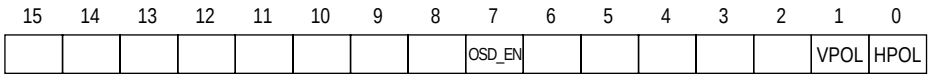
While OSD circuitry is displaying data from the display RAM, update the display RAM (location specified by the row and column address registers, OSDRAR and OSDCAR) by writing data to the high byte register (OSDDRH) followed by the low byte register (OSDDRL). After writing to the OSDDRL, the OSD buffer write ready bit (WRDY) will be cleared. WRDY becomes set again when the OSD circuitry has transferred the content of the OSD data registers to the display RAM.

Page 288: Correct OSD_EN bit location under **18.8.3.5 Frame Control Registers**

From: **Row 15, Column 15:**



To: **Row 15, Column 15:**



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