PEEL™ 16CV8 -25
CMOS Programmable Electrically Erasable Logic Device

Features

- **Compatible with Popular 16V8 Devices**
  - 16V8 socket and function compatible
  - Programs with standard 16V8 JEDEC file
  - 20-pin DIP, SOIC, TSSOP, and PLCC
- **CMOS Electrically Erasable Technology**
  - Superior factory testing
  - Reprogrammable in plastic package
  - Reduces retrofit and development costs
- **Application Versatility**
  - Replaces random logic
  - Super sets standard 20-pin PLDs (PALs)
- **Multiple Speed, Power Options**
  - Speeds range 25ns
  - Power as low as 37mA @ 25mHZ
- **Development / Programmer Support**
  - Third party software and programmers
  - Anachip WinPLACE Development Software
  - Automatic programmer translation and JEDEC file translation software available for the most popular PAL devices

General Description

The PEEL™ 16CV8 is a Programmable Electrically Erasable Logic (PEEL) device providing an attractive alternative to ordinary PLDs. The PEEL™ 16CV8 offers the performance, flexibility, ease of design and production practicality needed by logic designers today.

The PEEL™ 16CV8 is available in 20-pin DIP, PLCC, SOIC and TSSOP packages (see Figure 1) with 25ns speed and power consumption as low as 37mA. EE-Reprogrammability provides the convenience of instant reprogramming for development and reusable production inven- tory minimizing the impact of programming changes or errors. EE-Reprogrammability also improves factory testability, thus assuring the highest quality possible.

The PEEL™ 16CV8 architecture allows it to replace over standard 20-pin PLDs (PAL, GAL, EPLD etc.). See Figure 2. Anachip's PEEL™ 16CV8 can be programmed with existing 16CV8 JEDEC file. Some programmers also allow the PEEL™ 16CV8 to be programmed directly from PLD 16L8, 16R4, 16R6 and 16R8 JEDEC files. Additional development and programming support for the PEEL™16CV8 is provided by popular third-party programmers and development software. Anachip also offers free WinPLACE development software.

Figure 1 - Pin Configuration

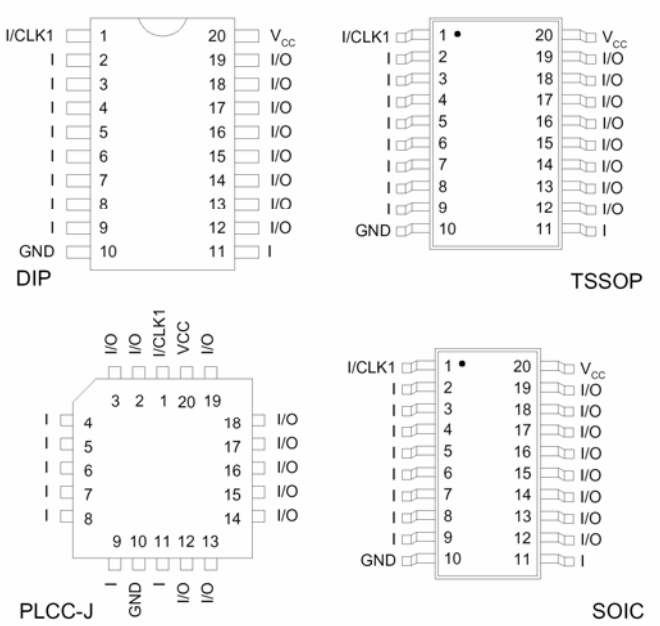
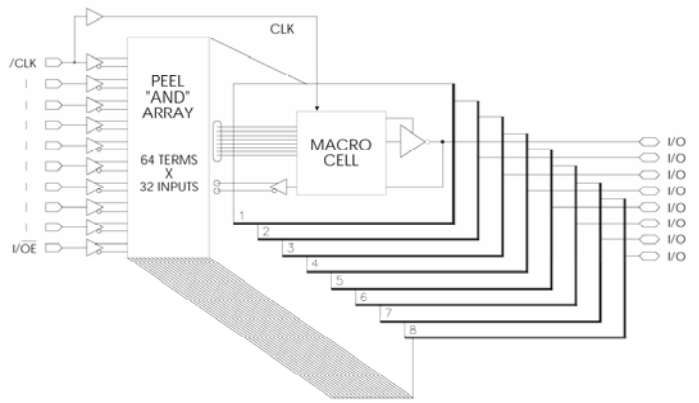


Figure 2 - Block Diagram



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Functional Description

The PEEL™ 16CV8 implements logic functions as sum-of- products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of macrocells further increase logic flexibility.

Architecture Overview

The PEEL™ 16CV8 features ten dedicated input pins and eight I/O pins, which allow a total of up to 16 inputs and 8 outputs for creating logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure the PEEL™ 16CV8 can implement up to 8 sum-of-products logic expressions.

Associated with each of the eight OR functions is a macrocell which can be independently programmed to one of up to four different basic configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing two possible feedback paths into the array.

Three different device modes, Simple, Complex, and Registered, support various user configurations. In Simple mode a macrocell can be configured for combinatorial function with the output buffer permanently enabled, or the output buffer can be disabled and the I/O pin used as a dedicated input. In Complex mode a macrocell is configured for combinatorial function with the output buffer enable controlled by a product term. In Registered mode, a macrocell can be configured for registered operation with the register clock and output buffer enable controlled directly from pins, or can be configured for combinatorial function with the output buffer enable controlled by a product term. In most cases the device mode is set automatically by the development software, based on the features specified in the design.

The three device modes support designs created explicitly for the PEEL™ 16CV8, as well as designs created originally for popular PLD devices such as the 16R4, 16R8, and 16L8. Table 1 shows the device mode used to emulate the various PLDs. Design conversion into the 16CV8 is accommodated by JEDEC-to-JEDEC translators available from Anachip, as well as several programmers which can read the original PLD JEDEC file and automatically program the 16CV8 to perform the same function.

AND/OR Logic Array

The programmable AND array of the PEEL™ 16CV8 is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

- **32 input lines:**
  - -16 input lines carry the true and complement of the signals applied to the 8 dedicated input pins
  - -16 additional lines carry the true and complement of 8 macrocell feedback signals or inputs from I/O pins or the clock/ OE pins

- **64 product terms:**
  - -56 product terms (arranged in 8 groups of 7) form sum-of-product functions for macrocell combinatorial or registered logic
  - -8 product terms (arranged 1 per macrocell) add an additional product term for macrocell sum-of-products functions or I/O pin output enable control

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 32-input AND gate. A product term which is connected to both the true and complement of an input signal will always be FALSE and thus will not affect the OR function that it drives. When all the connections on a product term are opened, that term will always be TRUE.

When programming the PEEL™ 16CV8, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL™ device programmers automatically program all of the connections on unused product terms so that they will have no effect on the output function.

Table 1 : PEEL™ 16CV8 Device Compatibility

PLD Architecture Compatibility	PEEL™ 16CV8 Device Mode
10H8	Simple
10L8	Simple
10P8	Simple
12H6	Simple
12L6	Simple
12P6	Simple
14H4	Simple
14L4	Simple
14P4	Simple
16H2	Simple
16HD8	Simple
16L2	Simple
16LD8	Simple
16P2	Simple
16H8	Complex
16L8	Complex
16P8	Complex
16R4	Registered
16R6	Registered
16R8	Registered
16RP4	Registered

Table 1 : PEEL™ 16CV8 Device Compatibility

PLD Architecture Compatibility	PEEL™ 16CV8 Device Mode
16RP6	Registered
14RP8	Registered

Programmable Macrocell

The macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL™ 16CV8 to the precise requirements of their designs.

Macrocell Architecture

Each macrocell consists of an OR function, a D-type flip-flop, an output polarity selector, and a programmable feedback path. Four EEPROM architecture bits MS0, MS1, OP, and RC control the configuration of each macrocell. Bits MS0 and MS1 are global, and select between Simple, Complex, and Registered mode for the whole device. Bits OP and RC are local for each macrocell; bit OP controls the output polarity and bit RC selects between registered and combinatorial operation and also specifies the feedback path. Table 2 shows the architecture bit settings for each possible configuration.

Equivalent circuits for the possible macrocell configurations are illustrated in Figures 3, 4, and 5. When creating a PEEL™ device design, the desired macrocell configuration generally is specified explicitly in the design file. When the design is assembled or compiled, the macrocell configuration bits are defined in the last lines of the JEDEC programming file.

Simple Mode

In Simple mode, all eight product terms feed the OR array which can generate a purely combinatorial function for the output pin. The programmable output polarity selector allows active-high or active-low logic, eliminating the need for external inverters. For output functions, the buffer can be permanently enabled. Feedback into the array is available on all macrocell I/O pins, except for pins 15 and 16. Figure 6 shows the logic array of the PEEL™ 16CV8 configured in Simple mode.

Simple mode also provides the option of configuring an I/O pin as a dedicated input. In this case, the output buffer is permanently disabled, and the I/O pin feedback is used to bring the input signal from the pin into the logic array. This option is available for all I/O pins except pins 15 and 16. Figure 3 shows the possible Simple mode macrocell configurations.

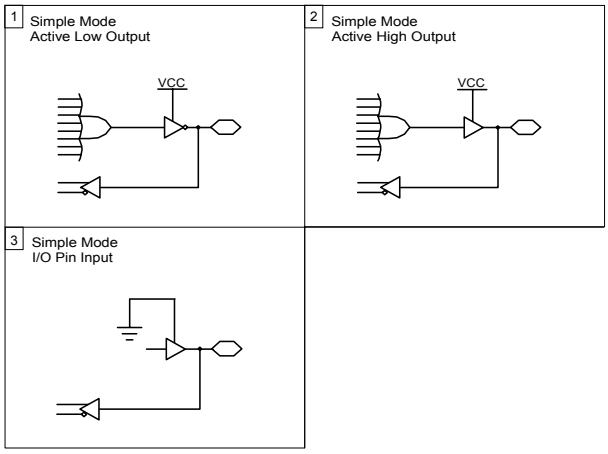


Figure 3 - Macrocell Configurations for Simple mode of the PEEL™ 16CV8 (see Figure 6 for Logic Array)

Table 2 : PEEL™ 16CV8 Device Mode/Macrocell Configuration Bits

Config.	Mode	Architecture Bits				Function	Polarity	Feedback
#		MSO	MS1	OP	RC			
1	Simple	1	0	0	0	Combinatorial	Active Low	I/O Pin
2	Simple	1	0	1	0	Combinatorial	Active High	I/O Pin
3	Simple	1	0	X	1	None	None	I/O Pin
1	Complex	1	1	0	1	Combinatorial	Active Low	I/O Pin
2	Complex	1	1	1	1	Combinatorial	Active High	I/O Pin
1	Registered	0	1	0	0	Registered	Active Low	Registered
2	Registered	0	1	1	0	Registered	Active High	Registered
3	Registered	0	1	0	1	Combinatorial	Active Low	I/O Pin
4	Registered	0	1	1	1	Combinatorial	Active High	I/O Pin

Complex Mode

In Complex mode, seven product terms feed the OR array which can generate a purely combinatorial function for the output pin. The programmable output polarity selector provides active-high or active-low logic, eliminating the need for external inverters. The output buffer is controlled by the eighth product term, allowing the macrocell to be configured for input, output, or bidirectional functions. Feedback into the array for input or bidirectional functions is available on all pins except 12 and 19. Figure 4 shows the possible complex mode macrocell configurations.

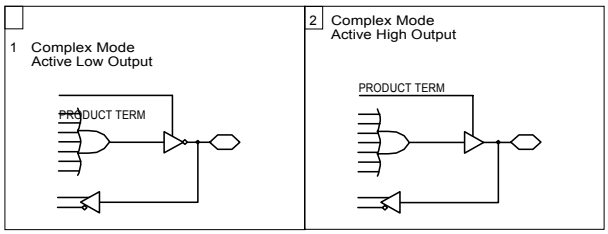


Figure 4 - Macrocell Configurations for the Complex Mode of the PEEL^{TM} 16CV8 (see Figure 7 for Logic Array)

Registered Mode

Registered mode provides eight product terms to the OR array for registered functions. The programmable output polarity selector provides active-high or active-low logic, eliminating the need for external inverters. (Note, however, that if register is selected, the PEEL^{TM} 16CV8 registers power-up reset and so before the first clock arrives the output at the pin will be low if the user has selected active-high logic and high if the user has selected active-low logic. If combinatorial is selected, the output will be a function of the logic.) For registered functions, the output buffer enable is controlled directly from the /OE control pin. Feedback into the array comes from the macrocell register. In Registered mode, input pins 1 and 11 are permanently allocated as CLK and /OE, respec- tively. Figure 8 shows the logic array of the PEEL^{TM} 16CV8 configured in Registered mode.

Registered mode also provides the option of configuring a macrocell for combinatorial operation, with seven product terms feeding the OR function.

Again the programmable output polarity selector provides active-high or active-low logic. The output buffer enable is controlled by the eighth product term, allowing the macrocell to be configured for input, output, or bidirectional functions. Feedback into the array for input or bidirectional functions is available on all I/O pins. Macrocell Configurations for the Registered Mode of the PEEL^{TM} 16CV8

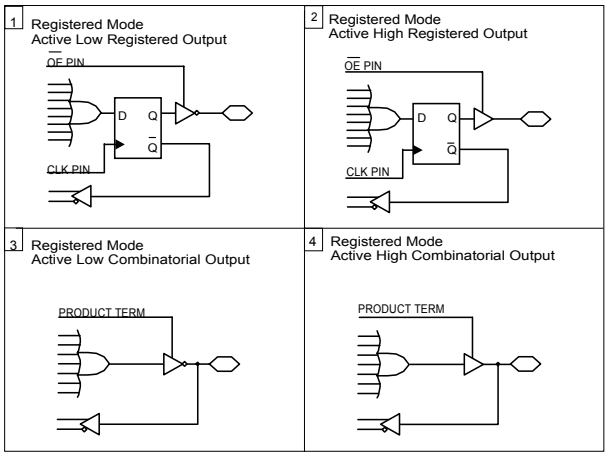


Figure 5 - Macrocell Configurations for the Registered Mode of the PEEL^{TM} 16CV8 (see Figure 8 for logic Array)

Design Security

The PEEL^{TM} 16CV8 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit has been set it is impossible to verify (read) or program the PEEL^{TM} until the entire device has first been erased with the bulk-erase function.

Signature Word

The signature word feature allows a 64-bit code to be programmed into the PEEL^{TM} 16CV8. The code cannot be read back after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

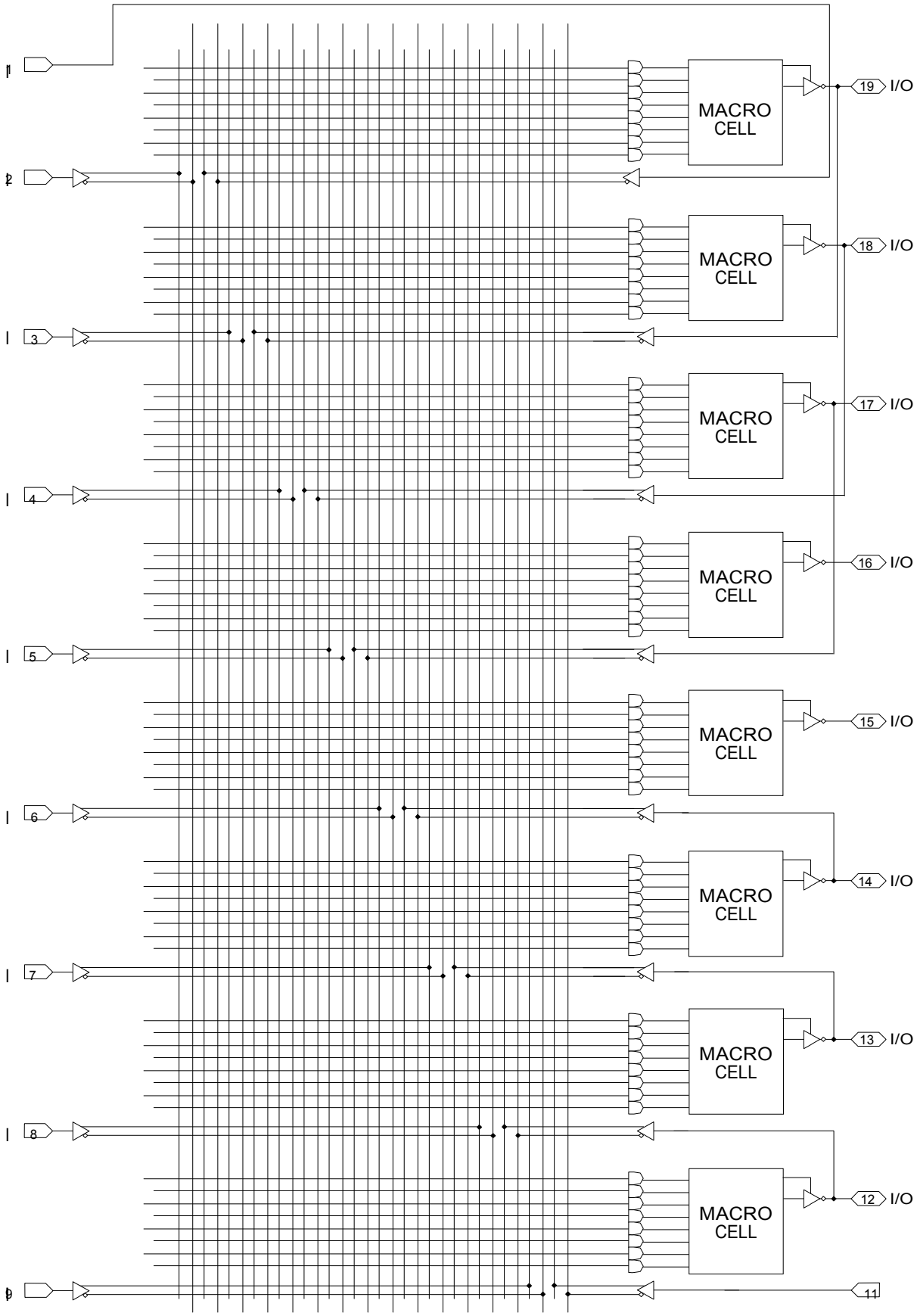


Figure 6 - PEEL™ 16CV8 Logic Array - Simple Mode (see Figure 3 for macrocell details)

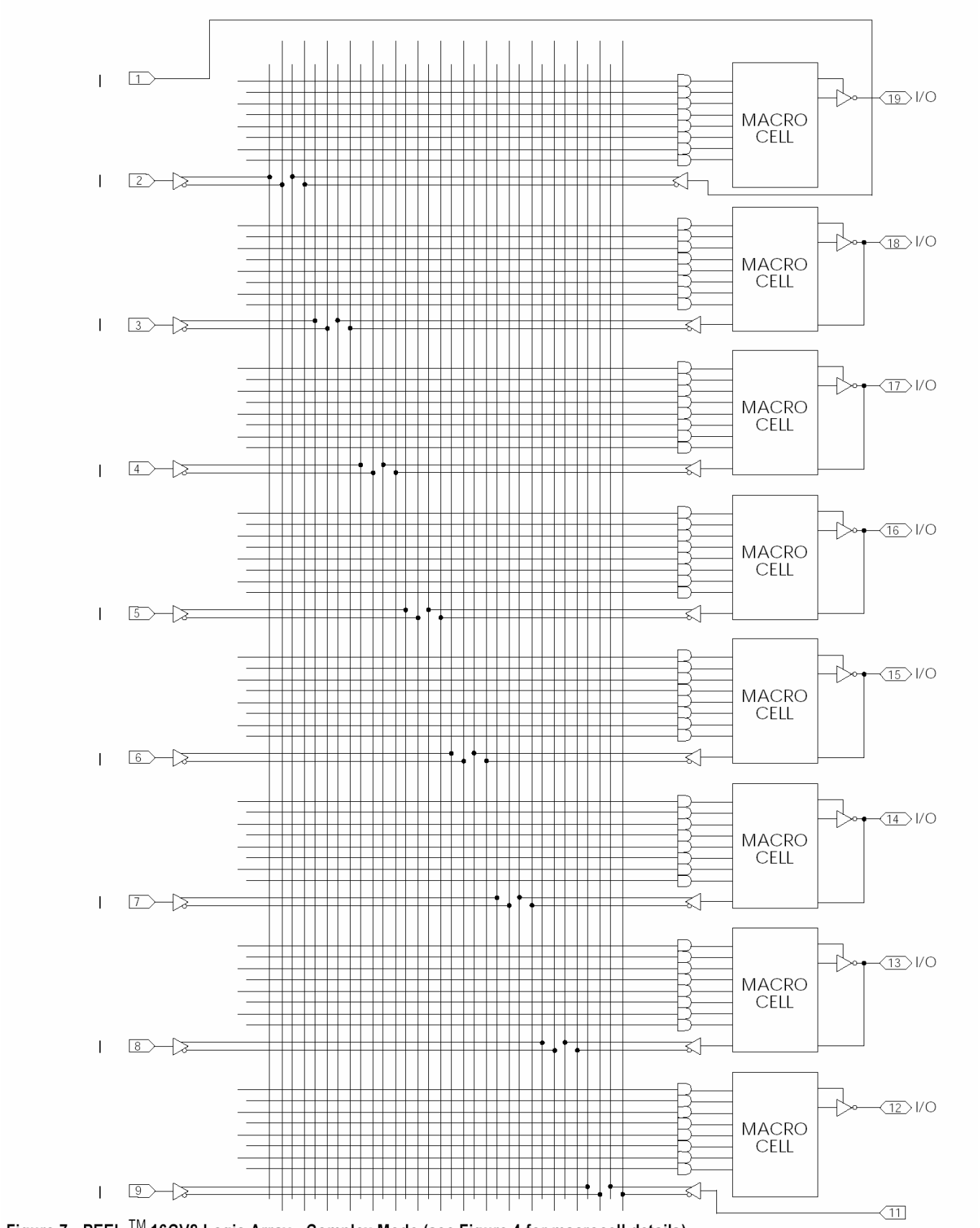


Figure 7 - PEEL ™ 16CV8 Logic Array - Complex Mode (see Figure 4 for macrocell details)

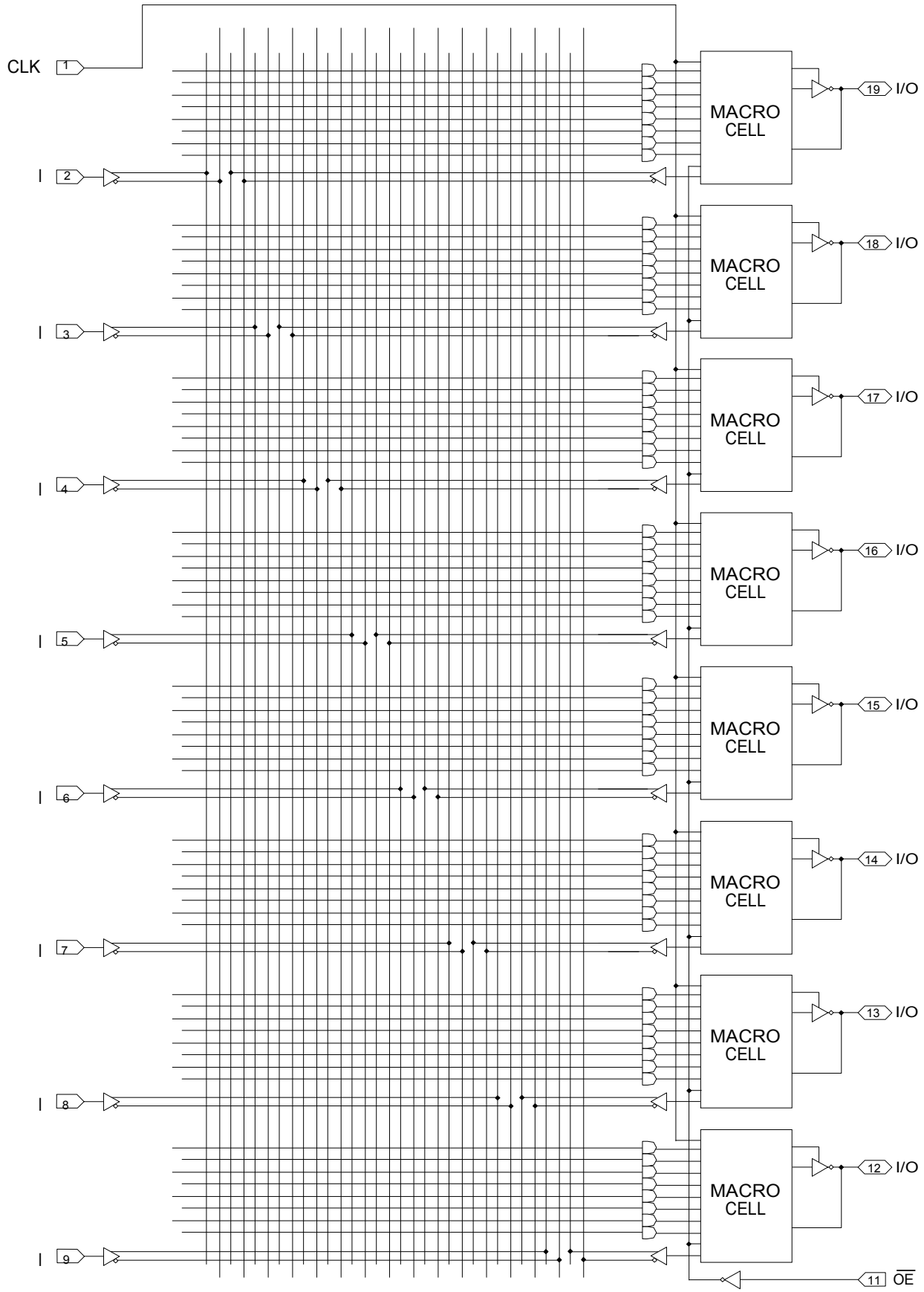


Figure 8 - PEEL ^{TM} 16CV8 Logic Array - Registered Mode (see Figure 5 for macrocell details)

Absolute Maximum Ratings

This device has been designed and tested for the specified operating ranges. Improper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to Ground	-0.5 to +6.0	V
V_O	Voltage Applied to Any Pin[2]	Relative to Ground[1]	-0.5 to V_{CC} +0.6	V
I_O	Output Current	Per Pin (I_{OL}, I_{OH})	+25	mA
T_{ST}	Storage Temperature		-65 to +150	°C
T_{LT}	Lead Temperature	Soldering 10 Seconds	+300	°C

Operating Range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	Ambient Temperature	Commercial	0	+70	°C
T_R	Clock Rise Time	See Note 3.		20	ns
T_F	Clock Fall Time	See Note 3.		20	ns
T_{RVCC}	V_{CC} Rise Time	See Note 3.		250	ms

D.C. Electrical Characteristics Over the operating range (Unless otherwise specified)

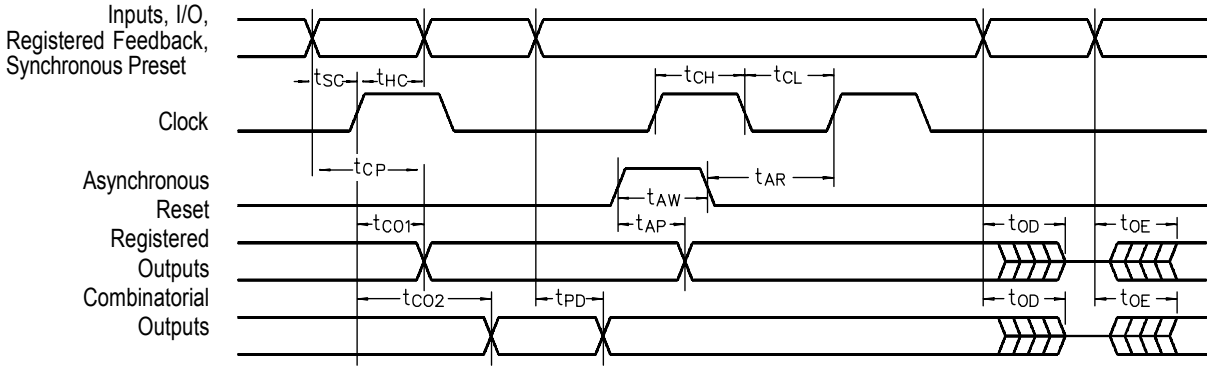
Symbol	Parameter	Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage – TTL	V_{CC}=Min, I_{OH}=-4.0mA		2.4		V
V_{OHC}	Output HIGH Voltage – CMOS	V_{CC}=Min, I_{OH}=-10µA		V_{CC}-0.3		V
V_{OL}	Output LOW Voltage – TTL	V_{CC}=Min, I_{OL}=16mA			0.5	V
V_{OLC}	Output LOW Voltage – CMOS	V_{CC}=Min, I_{OL}=10µA			0.15	V
V_{IH}	Input HIGH level			2.0	V_{CC}+0.3	V
V_{IL}	Input LOW Voltage			-0.3	0.8	V
I_{IL}	Input, I/O Leakage Current LOW	V_{CC}=Max, V_{IN}=GND, I/O=High Z			-10	µA
I_{IH}	Input, I/O Leakage Current HIGH	V_{CC}=Max, V_{IN}=GND, I/O=High Z		0(Typical)	40	µA
I_{CC}[10]	V_{CC} Current, f=1MHz	V_{IN}=0V or V_{CC}, F=25MHz All Outputs disabled[4]	-25		37	mA
C_{IN}[7]	Input Capacitance	T_A=25oC, V_{CC}=5.0V @f=1MHz			6	pF
C_{OUT}[7]	Output Capacitance				12	pF

A. C. Electrical Characteristics

Over the Operating Range 8, 11

Symbol	Parameter	Min	Max	Unit
tPD	Input[5] to non-registered output		25	ns
tOE	Input[5] to output enable[6]		25	ns
tOD	Input[5] to output disable[6]		25	ns
tCO1	Clock to Output		15	ns
tCO2	Clock to comb. Output delay Via internal registered feedback		35	ns
tCF	Clock to Feedback		10	ns
tSC	Input[5] or feedback setup to clock	20		ns
tHC	Input[5] hold after clock	0		ns
tCL, tCH	Clock low time, clock high time[8]	15		ns
tCP	Min clock period Ext (tSC + tCO1)	35		ns
fMAX1	Internal feedback (1/tSC +tCF)[11]	28.5		MHz
fMAX2	External Feedback (1/tCP)[11]	28.5		MHz
fMAX3	No Feedback (1/tCL +tCH)[11]	33.3		MHz
tAW	Asynchronous Reset Pulse Width	25		ns
tAP	Input[5] to Asynchronous Reset		25	ns
tAR	Asynchronous Reset recovery time		25	ns
tRESET	Power-on reset time for registers in clear state		5	µs

Switching Waveforms



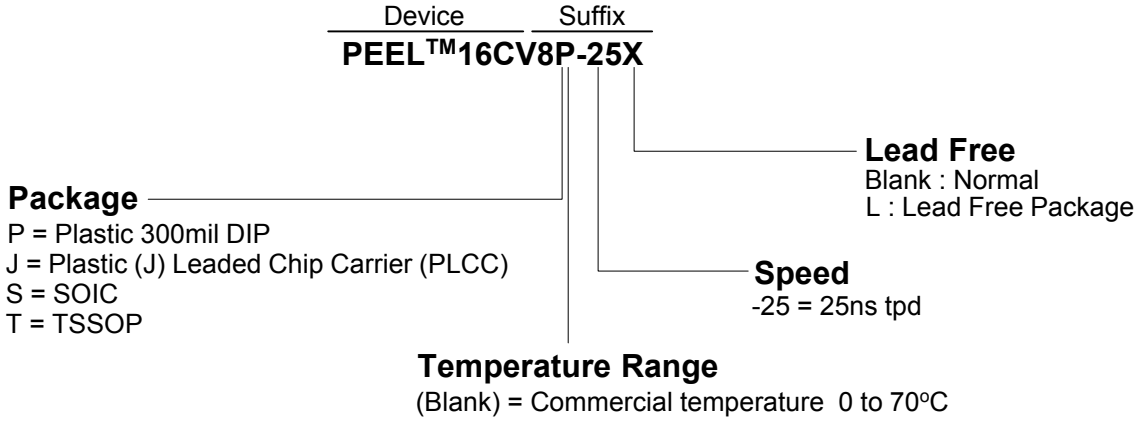
Notes:

1. Minimum DC input is -0.5V, however, inputs may undershoot to -2.0V for periods less than 20 ns.
2. VI and VO are not specified for program/verify operation.
3. Test Points for Clock and VCC in tR and tF are referenced at the 10% and 90% levels.
4. I/O pins are 0V and VCC.
5. "Input" refers to an input pin signal.
6. tOE is measured from input transition to VREF±0.1V, TOD is measured from input transi- tion to VOH-0.1V or VOL+0.1V; VREF=VL.
7. Capacitances are tested on a sample basis.
8. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (Unless otherwise specified).
9. Test one output at a time for a duration of less than 1 second.
10. ICC for a typical application: This parameter is tested with the device programmed as an 8-bit Counter.
11. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design process modification that might affect operational fre- quency.

Ordering Information

Part Number	Speed	Temperature	Package
PEEL™ 16CV8P-25 (L)	25ns	C	P20
PEEL™ 16CV8J-25 (L)	25ns	C	J20
PEEL™ 16CV8S-25 (L)	25ns	C	S20
PEEL™ 16CV8T-25 (L)	25ns	C	T20

Part Number



Anachip Corp.
Head Office ,
2F, No. 24-2, Industry E. Rd. IV, Science-Based
Industrial Park, Hsinchu, 300, Taiwan
Tel: +886-3-5678234
Fax: +886-3-5678368

Anachip USA
780 Montague Expressway, #201
San Jose, CA 95131
Tel: (408) 321-9600
Fax: (408) 321-9696

Email: sales_usa@anachip.com
Website: http://www.anachip.com