RJ21P3AA0PT

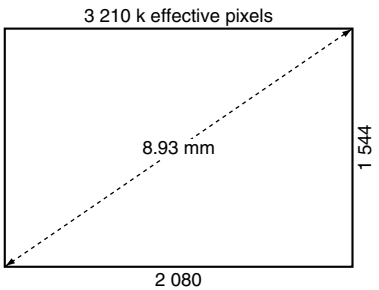
1/1.8-type Interline Color CCD Area Sensor with 3 370 k Pixels

DESCRIPTION

The RJ21P3AA0PT is a 1/1.8-type (8.93 mm) solid-state image sensor that consists of PN photodiodes and CCDs (charge-coupled devices). With approximately 3 370 000 pixels (2 152 horizontal x 1 567 vertical), the sensor provides a stable high-resolution color image.

FEATURES

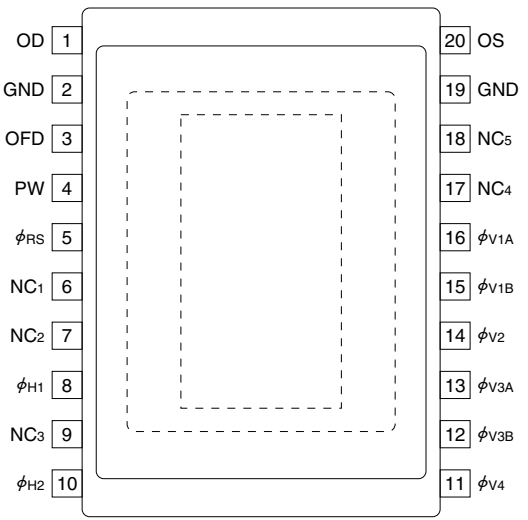
- Optical size : 8.93 mm (aspect ratio 4 : 3)



- Interline scan format
- Square pixel
- Number of image pixels : 2 096 (H) x 1 560 (V)
- Number of effective pixels : 2 080 (H) x 1 544 (V)
- Number of optical black pixels
  - Horizontal : 2 front and 54 rear
  - Vertical : 5 front and 2 rear
- Number of dummy bits
  - Horizontal : 24
  - Vertical : 2
- Pixel pitch : 3.45 µm (H) x 3.45 µm (V)
- R, G, and B primary color mosaic filters
- Supports monitoring mode
- Low fixed-pattern noise and lag
- No burn-in and no image distortion
- Blooming suppression structure
- Built-in output amplifier
- Built-in overflow drain voltage circuit and reset gate voltage circuit
- Variable electronic shutter
- Package :
  20-pin half-pitch DIP [Plastic]
  (P-DIP020-0500)
  Row space : 12.20 mm

PIN CONNECTIONS

20-PIN HALF-PITCH WDIP TOP VIEW



(P-DIP020-0500)

PRECAUTIONS

- The exit pupil position of lens should be 30 to 55 mm from the top surface of the CCD.
- Refer to **"PRECAUTIONS FOR CCD AREA SENSORS"** for details.

PIN DESCRIPTION

SYMBOL	PIN NAME
OD	Output transistor drain
OS	Output signals
ϕ_{RS}	Reset transistor clock
ϕ_{V1A}, ϕ_{V1B}, ϕ_{V2}, ϕ_{V3A}, ϕ_{V3B}, ϕ_{V4}	Vertical shift register clock
ϕ_{H1}, ϕ_{H2}	Horizontal shift register clock
OFD	Overflow drain
PW	P-well
GND	Ground
NC_1, NC_2, NC_3, NC_4, NC_5	No connection

ABSOLUTE MAXIMUM RATINGS

(T_A = +25˚C)

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Output transistor drain voltage	V_{OD}	0 to +18	V	
Overflow drain voltage	V_{OFD}	Internal output	V	1
Reset gate clock voltage	$V_{\phi RS}$	Internal output	V	2
Vertical shift register clock voltage	$V_{\phi V}$	V_{PW} to +18	V	
Horizontal shift register clock voltage	$V_{\phi H}$	−0.3 to +12	V	
Voltage difference between P-well and vertical clock	V_{PW}-$V_{\phi V}$	−27 to 0	V	
Voltage difference between vertical clocks	$V_{\phi V}$-$V_{\phi V}$	0 to +18	V	3
Storage temperature	T_{STG}	−40 to +85	˚C	
Ambient operating temperature	T_{OPR}	−20 to +70	˚C	

NOTES :

1. Do not connect to DC voltage directly. When OFD is connected to GND, connect V_{OD} to GND. Overflow drain clock is applied below 24 Vp-p.
2. Do not connect to DC voltage directly. When ϕ_{RS} is connected to GND, connect V_{OD} to GND. Reset gate clock is applied below 8 Vp-p.
3. When clock width is below 10 µs, and clock duty factor is below 0.1%, voltage difference between vertical clocks will be below 26 V.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Ambient operating temperature		T_{OPR}		25.0		˚C	
Output transistor drain voltage		V_{OD}	14.55	15.0	15.45	V	
Overflow drain clock	p-p level	$V_{\phi OFD}$	20.7	21.5	22.8	V	1
Ground		GND		0.0		V	
P-well voltage		V_{PW}	−8.0		$V_{\phi VL}$	V	2
Vertical shift register clock	LOW level	$V_{\phi V1AL}$, $V_{\phi V1BL}$, $V_{\phi V2L}$ $V_{\phi V3AL}$, $V_{\phi V3BL}$, $V_{\phi V4L}$	−7.35	−7.0	−6.65	V	
	INTERMEDIATE level	$V_{\phi V1AI}$, $V_{\phi V1BI}$, $V_{\phi V2I}$ $V_{\phi V3AI}$, $V_{\phi V3BI}$, $V_{\phi V4I}$		0.0		V	
	HIGH level	$V_{\phi V1AH}$, $V_{\phi V1BH}$ $V_{\phi V3AH}$, $V_{\phi V3BH}$	14.55	15.0	15.45	V	
Horizontal shift register clock	LOW level	$V_{\phi H1L}$, $V_{\phi H2L}$	−0.05	0.0	+0.05	V	
	HIGH level	$V_{\phi H1H}$, $V_{\phi H2H}$	4.5	4.8	5.5	V	
Reset gate clock	p-p level	$V_{\phi RS}$	4.5	4.8	5.5	V	1
Vertical shift register clock frequency		$f_{\phi V1A}$, $f_{\phi V1B}$, $f_{\phi V2}$ $f_{\phi V3A}$, $f_{\phi V3B}$, $f_{\phi V4}$		7.50		kHz	
Horizontal shift register clock frequency		$f_{\phi H1}$, $f_{\phi H2}$		18.00		MHz	
Reset gate clock frequency		$f_{\phi RS}$		18.00		MHz	

NOTES :

1. Use the circuit parameter indicated in **"SYSTEM CONFIGURATION EXAMPLE"**, and do not connect to DC voltage directly.
2. V_{PW} is set below $V_{\phi VL}$ that is low level of vertical shift register clock, or is used with the same power supply that is connected to V_L of V driver IC.

∗ To apply power, first connect GND and then turn on V_{OD}. After turning on V_{OD}, turn on V_{PW} first and then turn on other powers and pulses. Do not connect the device to or disconnect it from the plug socket while power is being applied.

CHARACTERISTICS (Drive method : 1/30 s frame accumulation)

(T_A = +25˚C, Operating conditions : The typical values specified in "**RECOMMENDED OPERATING CONDITIONS**". Color temperature of light source : 3 200 K, IR cut-off filter (CM-500, 1 mmt) is used.)

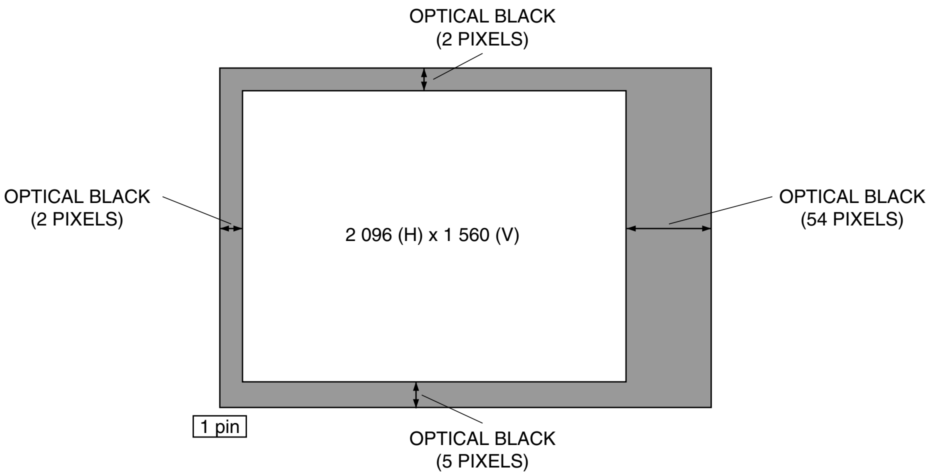
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Standard output voltage	V_O		150		mV	2
Photo response non-uniformity	PRNU			10	%	3
Saturation output voltage	V_{SAT}	450	530		mV	4
		320	400		mV	5
Dark output voltage	V_{DARK}		0.5	3.0	mV	1, 6
Dark signal non-uniformity	DSNU		0.5	2.0	mV	1, 7
Sensitivity (green channel)	R (G)	130	160		mV	8
Smear ratio	SMR		–90	–82	dB	9
Image lag	AI			1.0	%	10
Blooming suppression ratio	ABL	1 000				11
Output transistor drain current	I_{OD}		4.0	8.0	mA	

NOTES :

- Within the recommended operating conditions of V_{OD}, V_{OFD} of the internal output satisfies with ABL larger than 1 000 times exposure of the standard exposure conditions, and V_{SAT} larger than 320 mV.

1. T_A = +60˚C
2. The average output voltage of G signal under uniform illumination. The standard exposure conditions are defined as when Vo is 150 mV.
3. The image area is divided into 10 x 10 segments under the standard exposure conditions. Each segment's voltage is the average output voltage of all pixels within the segment. PRNU is defined by (Vmax – Vmin)/Vo, where Vmax and Vmin are the maximum and minimum values of each segment's voltage respectively.
4. The image area is divided into 10 x 10 segments. Each segment's voltage is the average output voltage of all pixels within the segment. V_{SAT} is the minimum segment's voltage under 10 times exposure of the standard exposure conditions. The operation of OFDC is high. (for still image capturing)
5. The image area is divided into 10 x 10 segments. Each segment's voltage is the average output voltage of all pixels within the segment. V_{SAT} is the minimum segment's voltage under 10 times exposure of the standard exposure conditions. The operation of OFDC is low.
6. The average output voltage under non-exposure conditions.
7. The image area is divided into 10 x 10 segments under non-exposure conditions. DSNU is defined by (Vdmax – Vdmin), where Vdmax and Vdmin are the maximum and minimum values of each segment's voltage respectively.
8. The average output voltage of G signal when a 1 000 lux light source with a 90% reflector is imaged by a lens of F4, f50 mm.
9. The sensor is exposed only in the central area of V/10 square with a lens at F4, where V is the vertical image size. SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum output voltage in the V/10 square.
10. The sensor is exposed at the exposure level corresponding to the standard conditions. AI is defined by the ratio of the output voltage measured at the 1st field during the non-exposure period to the standard output voltage.
11. The sensor is exposed only in the central area of V/10 square, where V is the vertical image size. ABL is defined by the ratio of the exposure at the standard conditions to the exposure at a point where blooming is observed.

PIXEL STRUCTURE



COLOR FILTER ARRAY

Pin arrangement of the vertical readout clock

(1, 1 560) (2 096, 1 560)

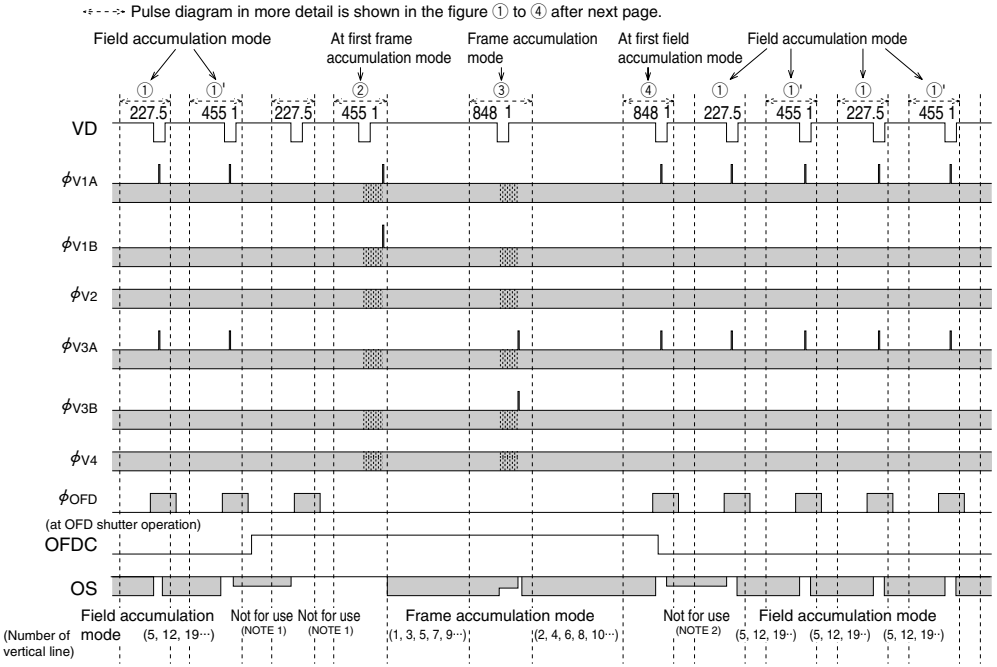
$\phi V3B$	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
$\phi V1A$	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
$\phi V3B$	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
$\phi V1B$	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
$\phi V3B$	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
$\phi V1B$	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
$\phi V3B$	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
$\phi V1B$	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
$\phi V3A$	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
$\phi V1B$	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
$\phi V3B$	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
$\phi V1B$	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
$\phi V3B$	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
$\phi V1B$	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
$\phi V3B$	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
$\phi V1A$	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
$\phi V3B$	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
$\phi V1B$	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G

$\phi V3B$	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
$\phi V1B$	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
$\phi V3B$	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
$\phi V1B$	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
$\phi V3B$	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
$\phi V1B$	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
$\phi V3A$	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
$\phi V1B$	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
$\phi V3B$	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
$\phi V1B$	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
$\phi V3B$	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
$\phi V1B$	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
$\phi V3B$	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
$\phi V1A$	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
$\phi V3B$	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
$\phi V1B$	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
$\phi V3B$	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
$\phi V1B$	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G

(1, 1) (2 096, 1)

TIMING CHART

TIMING CHART EXAMPLE

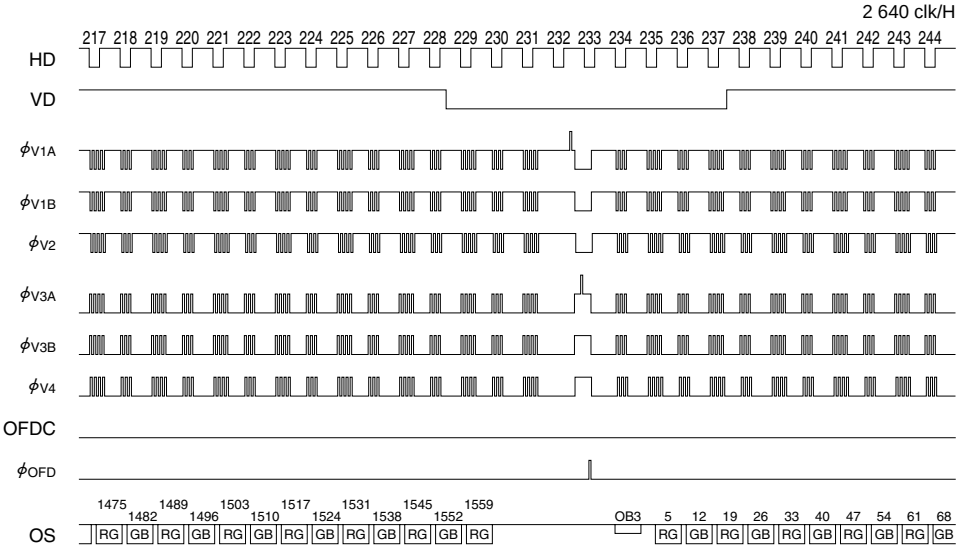


NOTES :

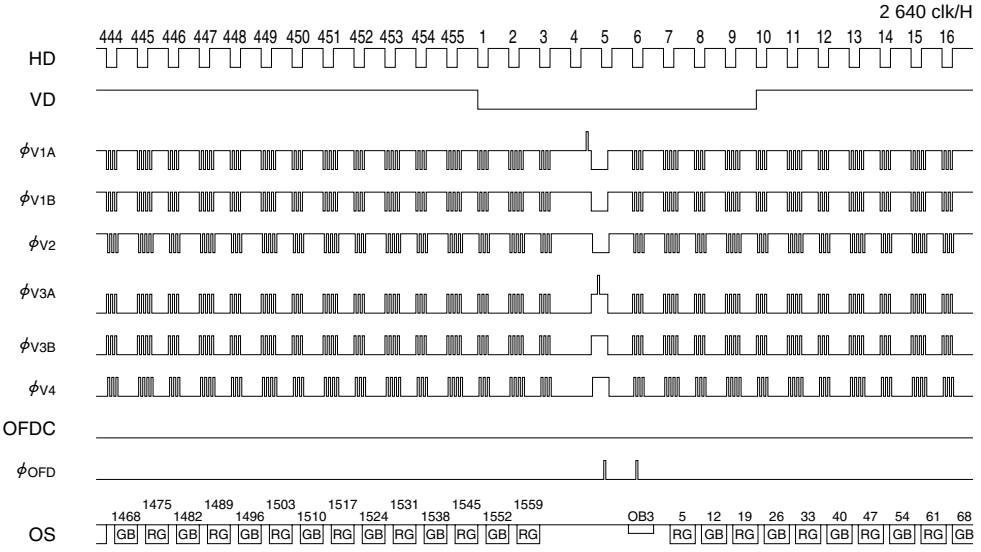
1. Do not use these signals immediately after field accumulation mode is transferred to frame accumulation mode for still image capturing.
2. Do not use these signals immediately after frame accumulation mode is transferred to field accumulation mode for monitoring image.

* Start the exposure period after 10 ms later that OFDC is high, and finish before change swept transfer.
* Apply at least an OFD shutter pulse to OFD in each field accumulation mode.

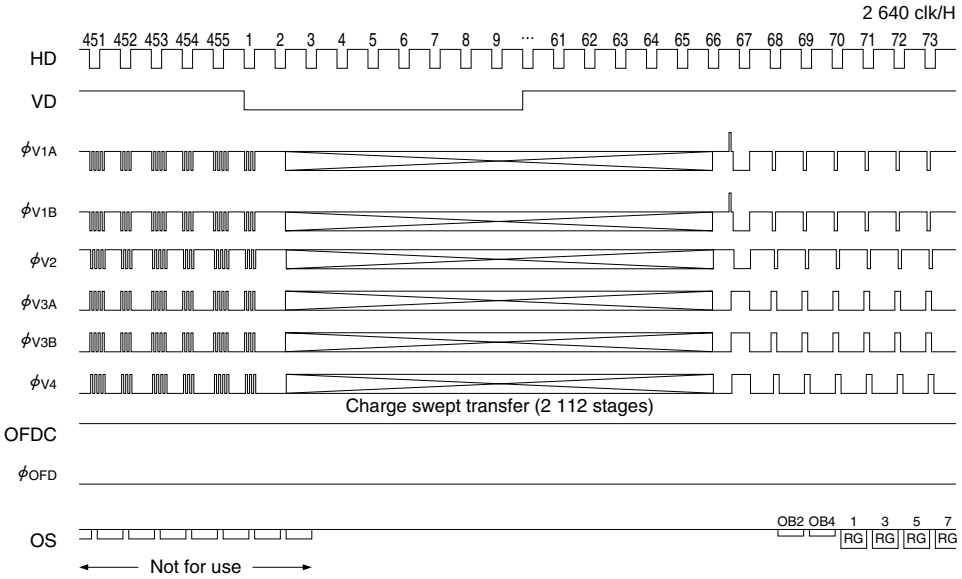
① VERTICAL TRANSFER TIMING【FIELD ACCUMULATION MODE】



①' VERTICAL TRANSFER TIMING【FIELD ACCUMULATION MODE】

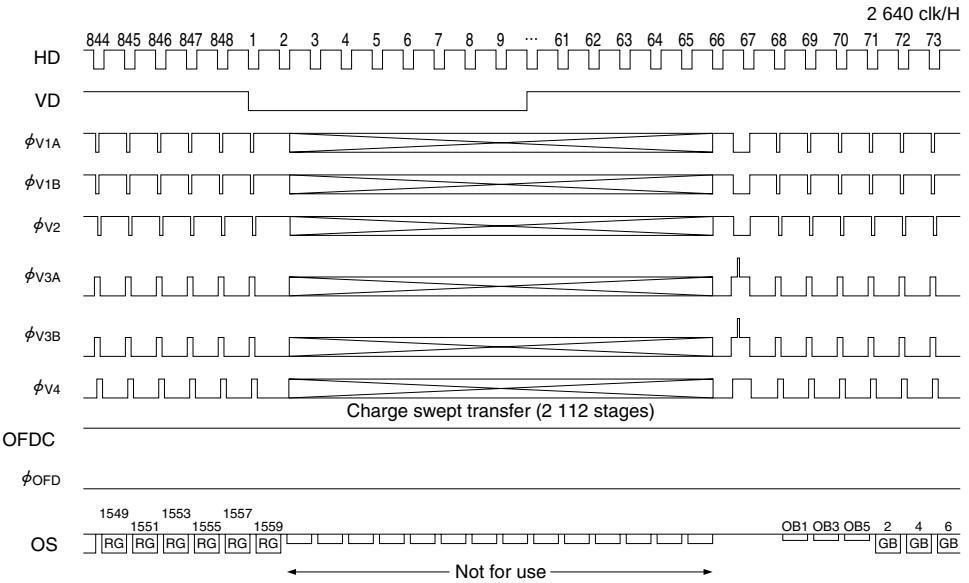


② VERTICAL TRANSFER TIMING【AT FIRST FRAME ACCUMULATION MODE】

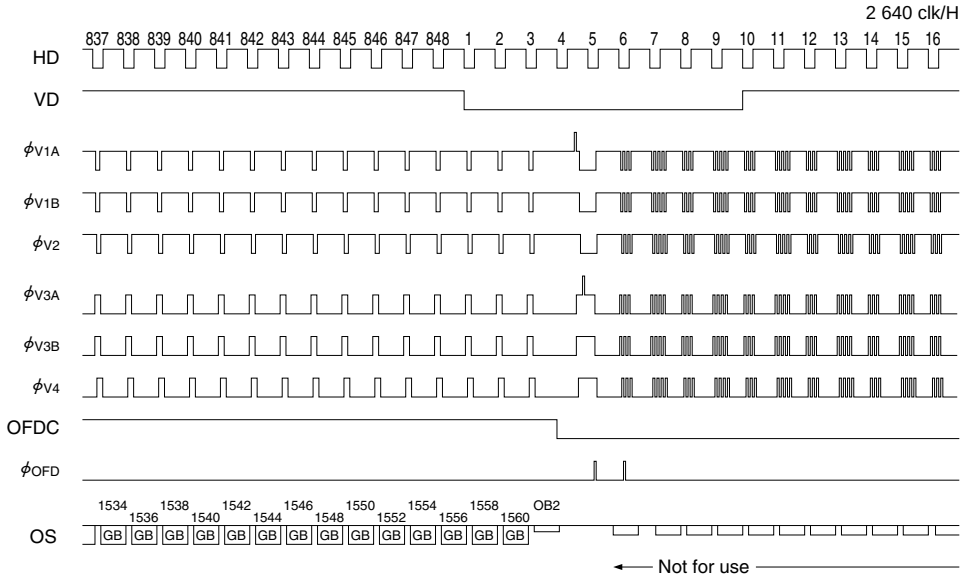


* Do not use the frame signals immediately after field accumulation mode is transferred to frame accumulation mode.

③ VERTICAL TRANSFER TIMING【FRAME ACCUMULATION MODE】

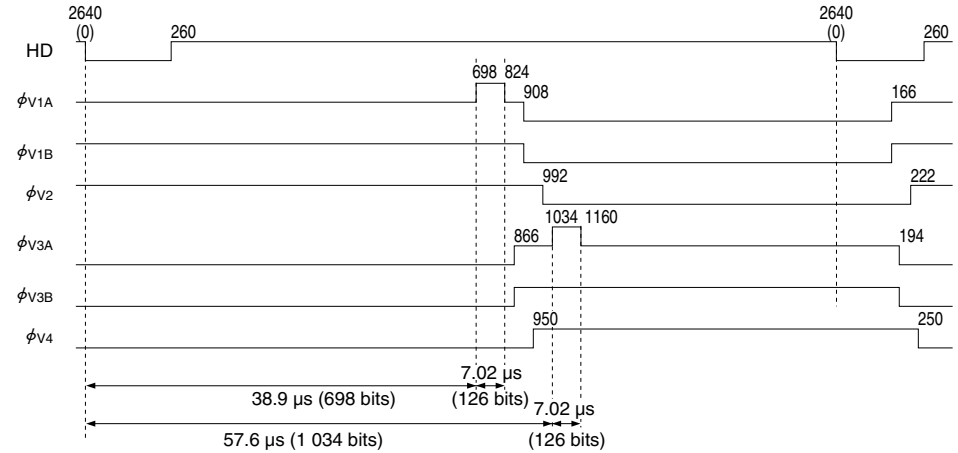


④ VERTICAL TRANSFER TIMING【AT FIRST FIELD ACCUMULATION MODE】

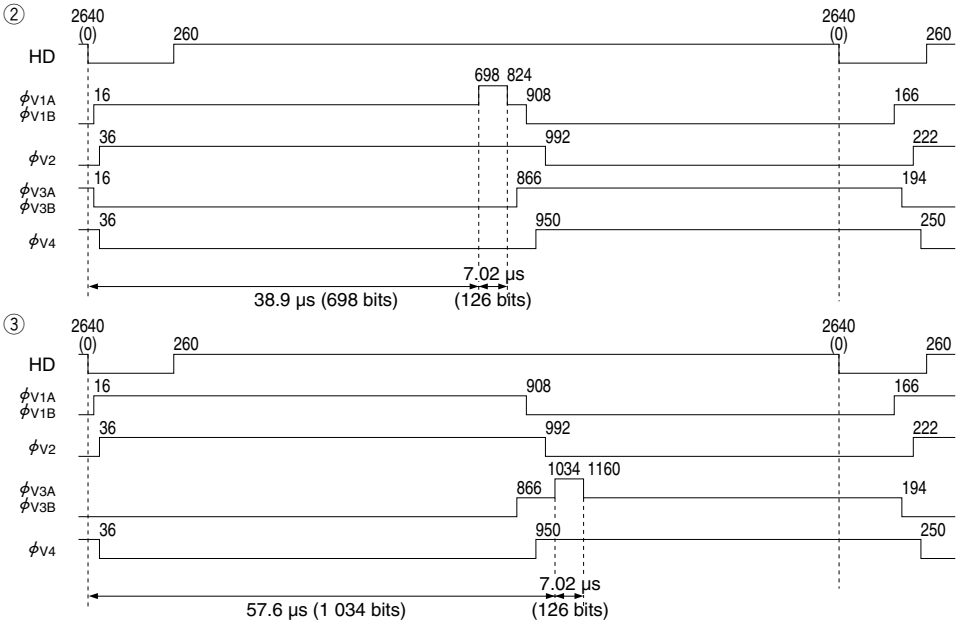


* Do not use the field signals immediately after frame accumulation mode is transferred to field accumulation mode for monitoring image.

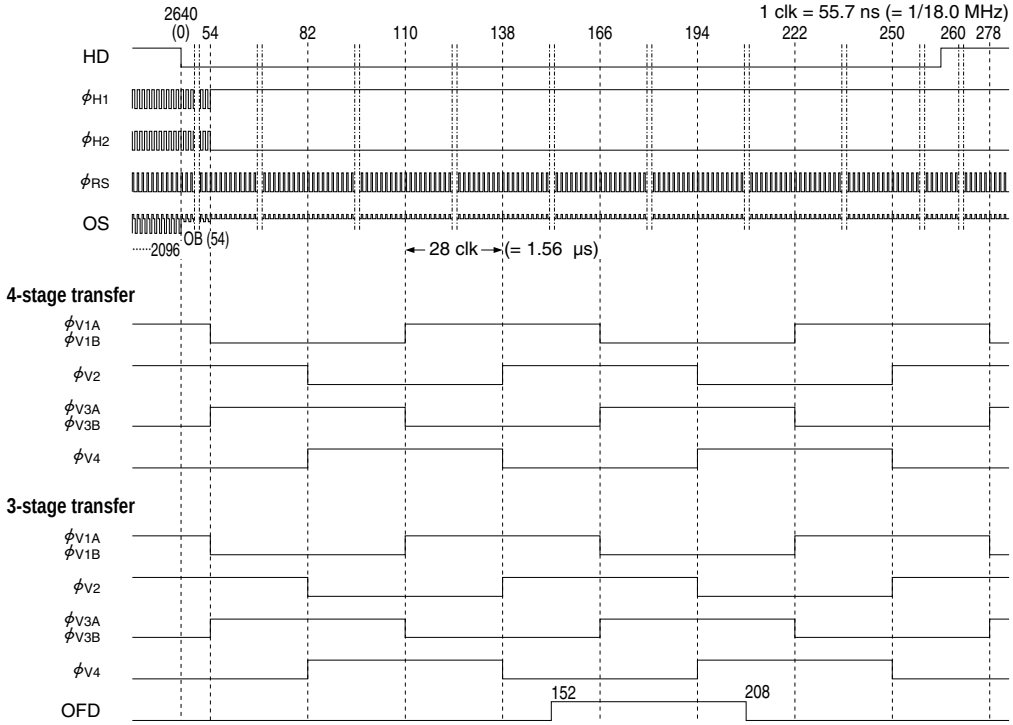
READOUT TIMING【FIELD ACCUMULATION MODE】



READOUT TIMING【FRAME ACCUMULATION MODE】

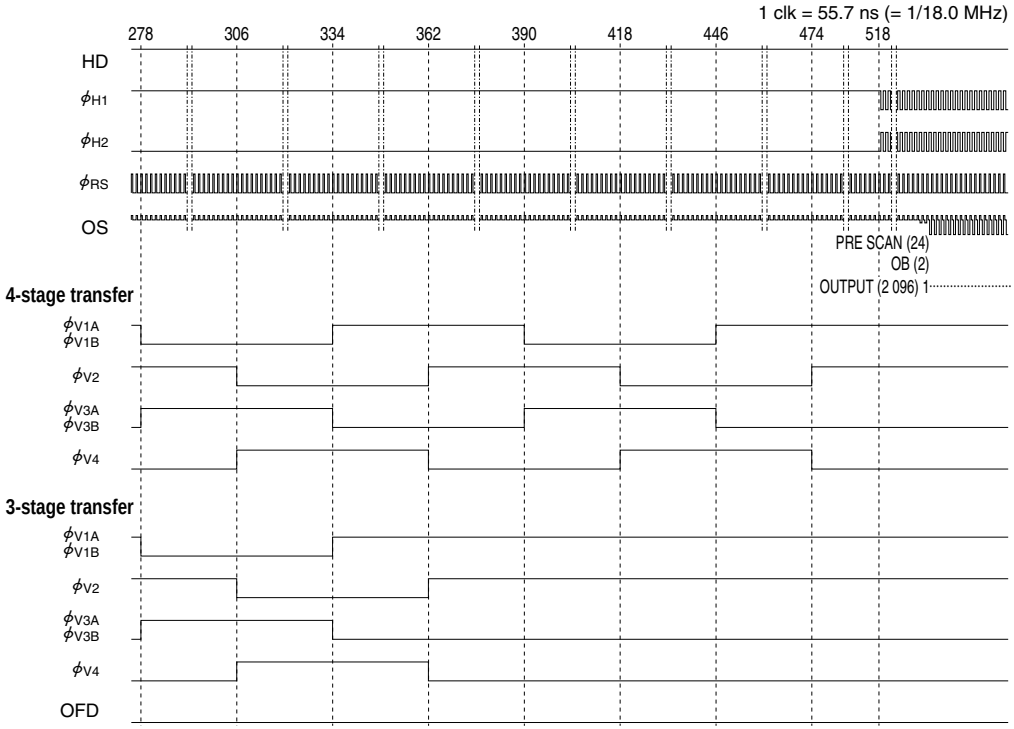


HORIZONTAL TRANSFER TIMING【FIELD ACCUMULATION MODE】-1



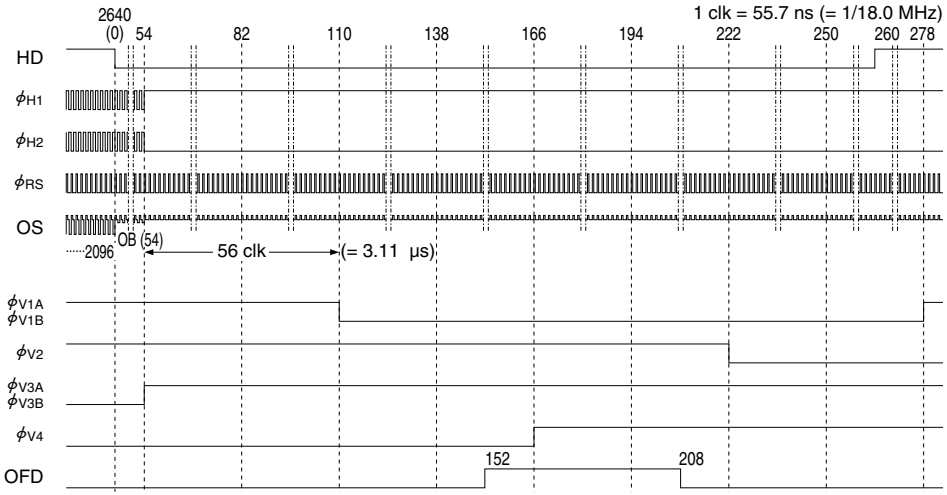
* Keep over 1.56 µs when vertical transfer clock pulse is overlapping.

HORIZONTAL TRANSFER TIMING【FIELD ACCUMULATION MODE】-2



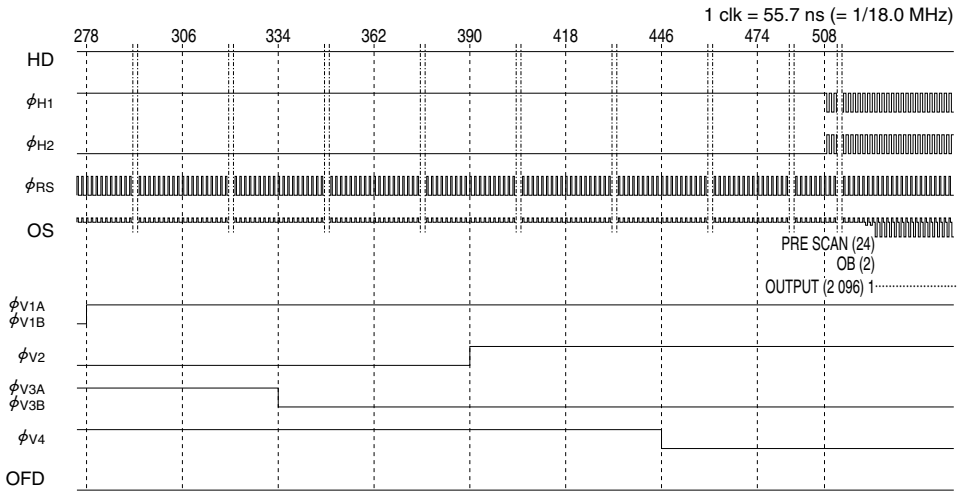
∗ Keep over 1.56 µs when vertical transfer clock pulse is overlapping.

HORIZONTAL TRANSFER TIMING【FRAME ACCUMULATION MODE】-1



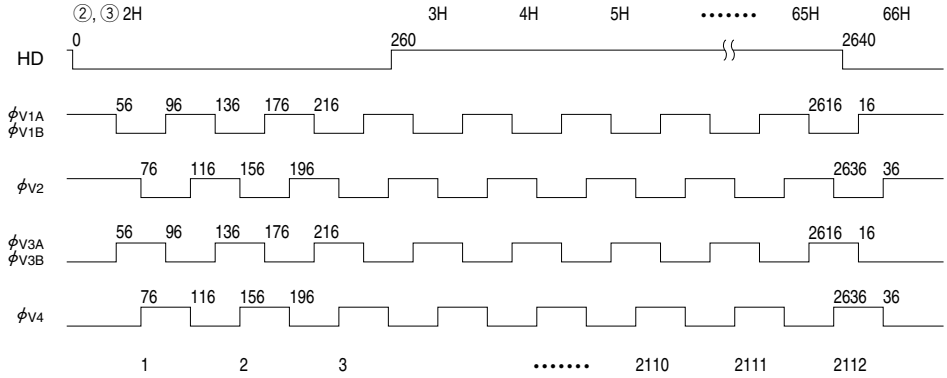
∗ Keep over 3.11 µs when vertical clock pulse is overlapping.

HORIZONTAL TRANSFER TIMING【FRAME ACCUMULATION MODE】-2



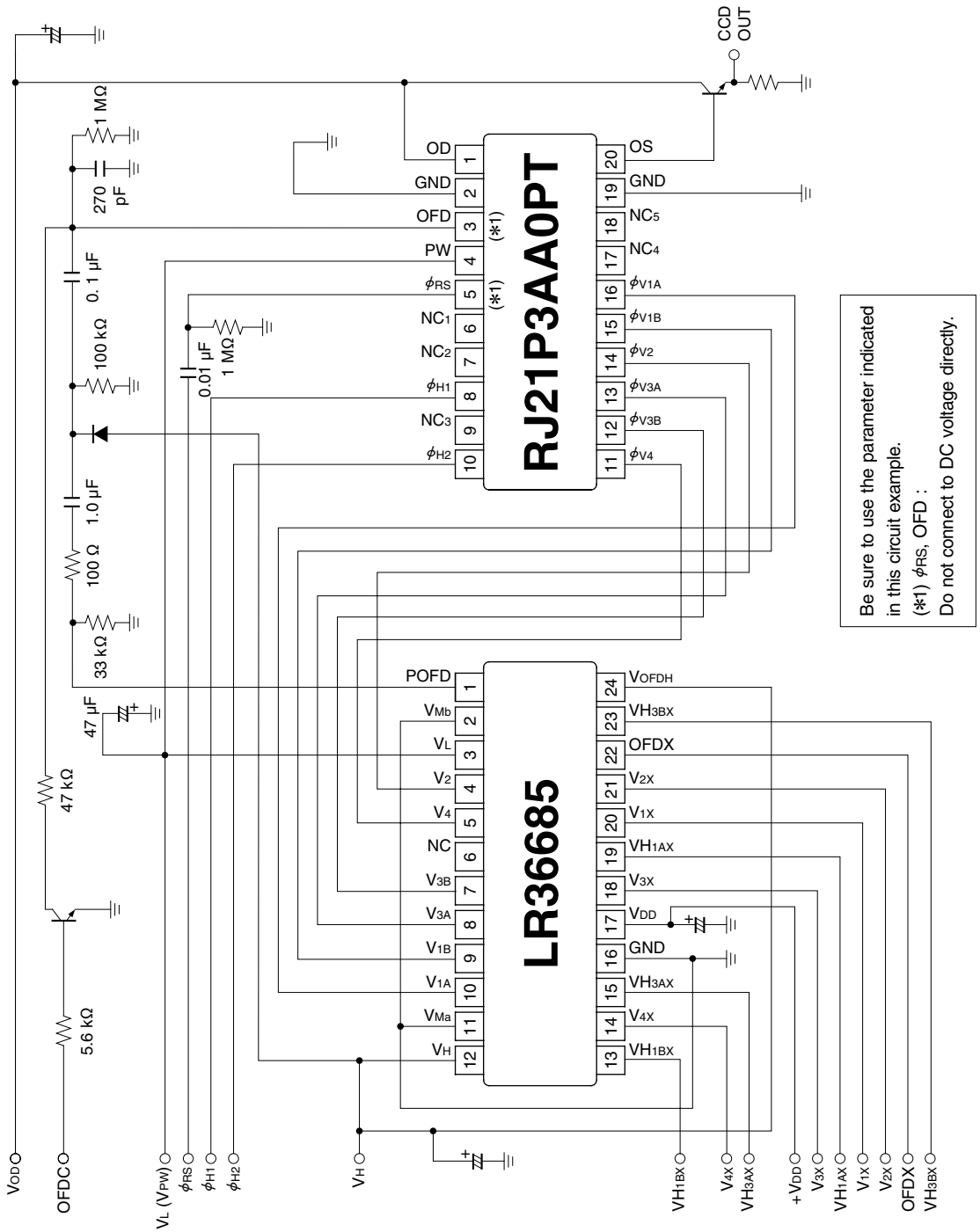
∗ Keep over 3.11 µs when vertical transfer clock pulse is overlapping.

CHARGE SWEPT TRANSFER TIMING【FRAME ACCUMULATION MODE】



∗ Keep over 1.56 µs when vertical transfer clock pulse of charge swept transfer is overlapping.

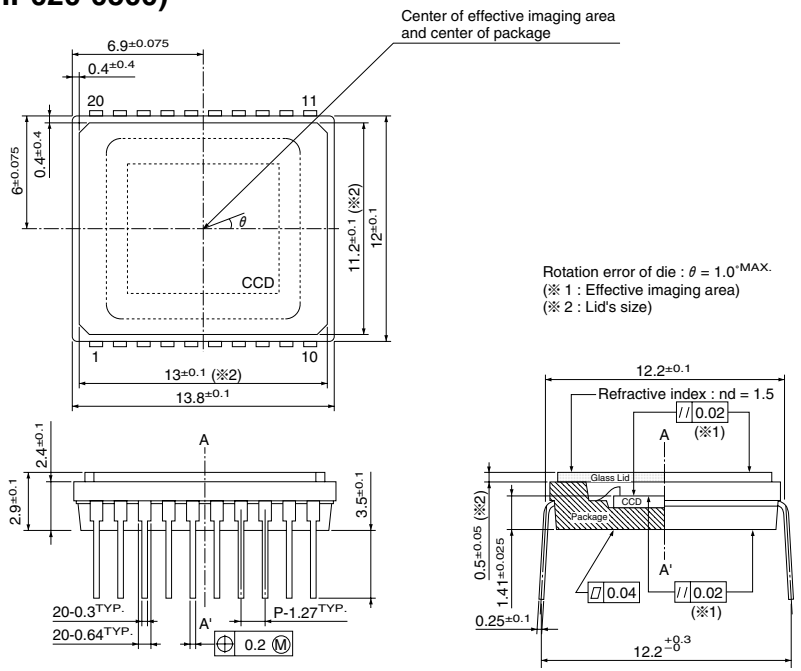
SYSTEM CONFIGURATION EXAMPLE



PACKAGE OUTLINES

20 DIP (P-DIP020-0500)

(Unit : mm)



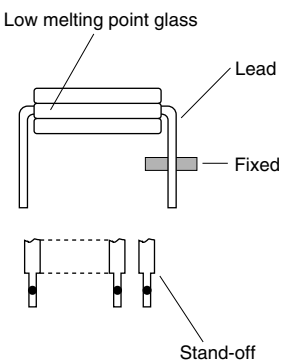
PRECAUTIONS FOR CCD AREA SENSORS

1. Package Breakage

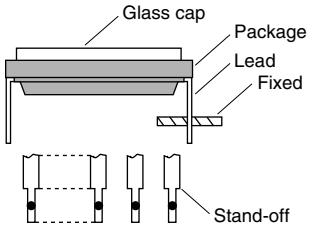
In order to prevent the package from being broken, observe the following instructions :

1) The CCD is a precise optical component and the package material is ceramic or plastic.
   Therefore,
   - Take care not to drop the device when mounting, handling, or transporting.
   - Avoid giving a shock to the package.
     Especially when leads are fixed to the socket or the circuit board, small shock could break the package more easily than when the package isn't fixed.
2) When applying force for mounting the device or any other purposes, fix the leads between a joint and a stand-off, so that no stress will be given to the jointed part of the lead. In addition, when applying force, do it at a point below the stand-off part.

   (In the case of ceramic packages)
   – The leads of the package are fixed with low melting point glass, so stress added to a lead could cause a crack in the low melting point glass in the jointed part of the lead.



   (In the case of plastic packages)
   – The leads of the package are fixed with package body (plastic), so stress added to a lead could cause a crack in the package body (plastic) in the jointed part of the lead.



3) When mounting the package on the housing, be sure that the package is not bent.
   – If a bent package is forced into place between a hard plate or the like, the package may be broken.
4) If any damage or breakage occurs on the surface of the glass cap, its characteristics could deteriorate.
   Therefore,
   - Do not hit the glass cap.
   - Do not give a shock large enough to cause distortion.
   - Do not scrub or scratch the glass surface.
   – Even a soft cloth or applicator, if dry, could cause flaws to scratch the glass.

2. Electrostatic Damage

As compared with general MOS-LSI, CCD has lower ESD. Therefore, take the following antistatic measures when handling the CCD :

1) Always discharge static electricity by grounding the human body and the instrument to be used. To ground the human body, provide resistance of about 1 MΩ between the human body and the ground to be on the safe side.
2) When directly handling the device with the fingers, hold the part without leads and do not touch any lead.