DATA SHEET

SAA8116HL
Digital PC-camera signal processor, microcontroller and USB interface

Objective specification
File under Integrated Circuits, IC22

2000 Apr 13

Digital PC-camera signal processor, microcontroller and USB interface

SAA8116HL

FEATURES

- High precision digital processing with 10-bit input
- Embedded microcontroller (80C51 core based) for control loops Auto Optical Black (AOB), Auto White Balance (AWB), Auto Exposure (AE) and USB interface control
- Compliant for VGA CCD and VGA CMOS sensors (RGB Bayer)
- USB 1.1 compliant core
- RGB processing
- Optical black processing
- Defect pixel concealment
- Programmable colour matrix
- RGB to YUV transform
- Programmable gamma correction (including knee)
- Programmable edge enhancement
- Video formatter with SIF/QSIF downscaler
- Compression engine
- Flexible Measurement Engine (ME) with up to eight measurements per frame
- Internal Pulse Pattern Generator (PPG) for wide range of VGA CCDs (Sony, Sharp and Panasonic) and frame rate selection
- Programmable H and V timings for the support of CMOS sensors
- Programmable output pulse for switched mode power supply of the sensor
- 3-wire interface to control the TDA8787A: Correlated Double Sampling (CDS) circuit, Automatic Gain Control (AGC) circuit and 10-bit ADC
- Analog microphone/audio input to USB: Low DropOut (LDO) supply filter, microphone supply, low noise amplifier, programmable amplifier, PLL and ADC
- Integrated analog USB driver (ATX)
- Integrated main oscillator including a clock PLL to increase the crystal frequency (from 12 to 48 MHz)
- USB 1.1 compliant bus-powered USB device with integrated power management and POR circuit.

APPLICATIONS

- USB PC-camera (video and audio).

GENERAL DESCRIPTION

The SAA8116HL is a highly integrated third generation of USB PC-camera ICs. It is the successor of the SAA8112HL and SAA8115HL. It processes the digitized sensor data and converts it to a high quality, compressed YUV signal. Together with the audio signal, this video signal is then properly formatted in USB packets.

In addition, an 80C51 microcontroller derivative with five I/O ports, I^{2}C-bus, 512 bytes of RAM and 32 kbytes of program memory is embedded in the SAA8116HL. The microcontroller is used in combination with the programmable statistical measurement capabilities to provide advanced AE, AWB and AOB. The microcontroller is also used to control the USB interface.

QUICK REFERENCE DATA

Measured over full voltage and temperature range: V_{DD} = 3.3 V ±10% and T_{amb} = 0 to 70 °C; unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	3.3	3.6	V
$I_{DD(tot)}$	total supply current	V_{DD} = 3.6 V; T_{amb} = 70 °C	–	–	tbf	mA
V_i	input voltage	3.0 V < V_{DD} < 3.6 V	low voltage TTL compatible			V
V_o	output voltage	3.0 V < V_{DD} < 3.6 V	low voltage TTL compatible			V
$f_{(i)xtal}$	crystal input frequency		–	12	–	MHz
δ	crystal frequency duty factor		–	50	–	%
P_{tot}	total power dissipation	V_{DD} = 3.3 V; T_{amb} = 25 °C	–	–	300	mW
T_{stg}	storage temperature		–55	–	+150	°C
T_{amb}	ambient temperature		0	25	70	°C
T_j	junction temperature	T_{amb} = 70 °C	–	–	125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA8116HL	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

BLOCK DIAGRAM

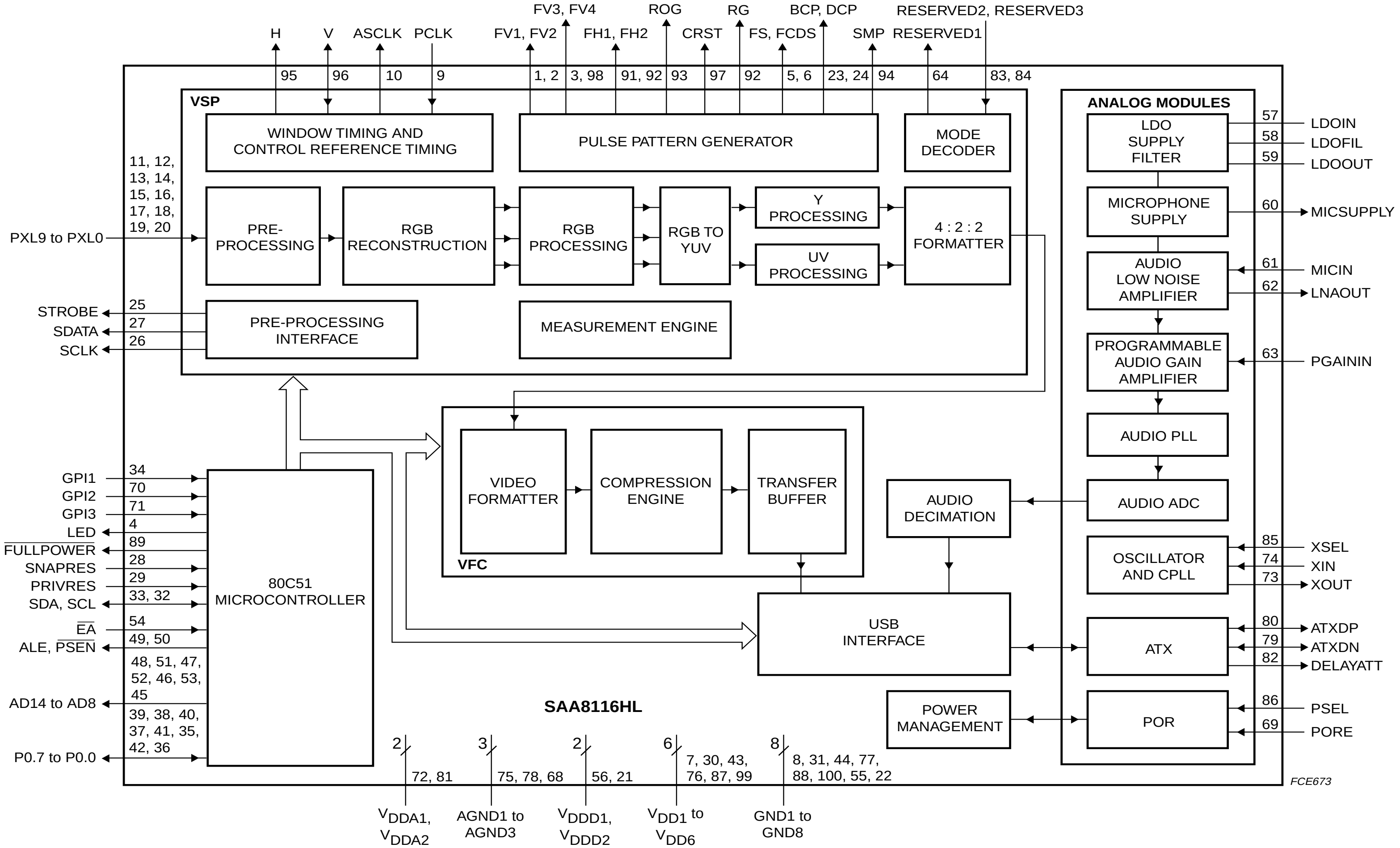


Fig.1 Block diagram.

PINNING

PIN	SYMBOL	TYPE[1]	DESCRIPTION
1	FV1	O	vertical CCD transfer pulse output
2	FV2	O	vertical CCD transfer pulse output
3	FV3	O	vertical CCD transfer pulse output
4	LED	O	output to drive LED
5	FS	O	data sample-and-hold pulse output to TDA8787A (SHD)
6	FCDS	O	preset sample-and-hold pulse output to TDA8787A (SHP)
7	V_{DD1}	P	supply voltage 1 for output buffers
8	GND1	P	ground 1 for output buffers
9	PCLK	I	pixel input clock
10	ASCLK	O	clock1 (pixel clock) or clock2 (2 × pixel clock) output for ADC or CMOS sensor
11	PXL9	I	pixel data input; bit 9
12	PXL8	I	pixel data input; bit 8
13	PXL7	I	pixel data input; bit 7
14	PXL6	I	pixel data input; bit 6
15	PXL5	I	pixel data input; bit 5
16	PXL4	I	pixel data input; bit 4
17	PXL3	I	pixel data input; bit 3
18	PXL2	I	pixel data input; bit 2
19	PXL1	I	pixel data input; bit 1
20	PXL0	I	pixel data input; bit 0
21	V_{DDD2}	P	supply voltage 2 for the digital core
22	GND8	P	ground 8 for input buffers and predrivers
23	BCP	O	optical black clamp pulse output to TDA8787A
24	DCP	O	dummy clamp pulse output to TDA8787A
25	STROBE	O	strobe signal output to TDA8787A or general purpose output of the microcontroller
26	SCLK	O	serial clock output to TDA8787A or general purpose output of the microcontroller
27	SDATA	O	serial data output to TDA8787A or general purpose output of the microcontroller
28	SNAPRES	I	snapshot input or remote wake-up trigger input (programmable)
29	PRIVRES	I	privacy shutter input or remote wake-up trigger input (programmable)
30	V_{DD2}	P	supply voltage 2 for input buffers and predrivers
31	GND2	P	ground 2 for input buffers and predrivers
32	SCL	I/O	I^2C-bus clock input/output (master/slave)
33	SDA	I/O	I^2C-bus data input/output (master/slave)
34	GPI1	I	general purpose input 1 (Port 4; bit 6)
35	P0.2	I/O	microcontroller Port 0 bidirectional (data - address); bit 2
36	P0.0	I/O	microcontroller Port 0 bidirectional (data - address); bit 0
37	P0.4	I/O	microcontroller Port 0 bidirectional (data - address); bit 4
38	P0.6	I/O	microcontroller Port 0 bidirectional (data - address); bit 6
39	P0.7	I/O	microcontroller Port 0 bidirectional (data - address); bit 7

PIN	SYMBOL	TYPE[1]	DESCRIPTION
40	P0.5	I/O	microcontroller Port 0 bidirectional (data - address); bit 5
41	P0.3	I/O	microcontroller Port 0 bidirectional (data - address); bit 3
42	P0.1	I/O	microcontroller Port 0 bidirectional (data - address); bit 1
43	V_{DD3}	P	supply voltage 3 for output buffers
44	GND3	P	ground 3 for output buffers
45	AD8	O	microcontroller Port 2 output (address); bit 0
46	AD10	O	microcontroller Port 2 output (address); bit 2
47	AD12	O	microcontroller Port 2 output (address); bit 4
48	AD14	O	microcontroller Port 2 output (address); bit 6
49	ALE	O	address latch enable output for external latch
50	$\overline{PSEN}$	O	program store enable output for external memory (active LOW)
51	AD13	O	microcontroller Port 2 output (address); bit 5
52	AD11	O	microcontroller Port 2 output (address); bit 3
53	AD9	O	microcontroller Port 2 output (address); bit 1
54	$\overline{EA}$	I	external access select input - internal or external program memory (active LOW)
55	GND7	P	ground 7 for input buffers and predrivers
56	V_{DDD1}	P	supply voltage 1 for the digital core
57	LDOIN	P	analog supply voltage for LDO supply filter
58	LDOFIL	–	external capacitor connection (filter of LDO)
59	LDOOUT	–	external capacitor connection (internal analog supply voltage for PLL, amplifier and ADC)
60	MICSUPPLY	O	microphone supply output
61	MICIN	I	microphone input
62	LNAOUT	O	low noise amplifier output
63	PGAININ	I	programmable gain amplifier input
64	RESERVED1	O	test pin 1 (should not be used)
65	REF1	I	reference voltage 1 (used in the amplifier and the ADC)
66	REF2	I	reference voltage 2 (used in the ADC)
67	REF3	I	reference voltage 3 (used in the ADC)
68	AGND3	P	analog ground 3 for PLL, amplifier and ADC
69	PORE	I	external Power-on reset (backup)
70	GPI2	I	general purpose input 2 (Port 1; bit 4)
71	GPI3	I	general purpose input 3 (Port 3; bit 5)
72	V_{DDA1}	P	analog supply voltage 1 for crystal oscillator (12 MHz, fundamental)
73	XOUT	O	oscillator output
74	XIN	I	oscillator input
75	AGND1	P	analog ground 1 for crystal oscillator
76	V_{DD4}	P	supply voltage 4 for input buffers and predrivers
77	GND4	P	ground 4 for input buffers and predrivers
78	AGND2	P	analog ground 2 for ATX transceiver
79	ATXDN	I/O	negative driver of the differential data pair input/output (ATX)

PIN	SYMBOL	TYPE[(1)]	DESCRIPTION
80	ATXDP	I/O	positive driver of the differential data pair input/output (ATX)
81	V_{DDA2}	P	analog supply voltage 2 for ATX transceiver
82	DELAYATT	O	delay attached control output; connected with pull-up resistor on ATXDP (USB)
83	RESERVED2	I	test pin 2 (should not be used)
84	RESERVED3	I	test pin 3 (should not be used)
85	XSEL	I	crystal selection input (backup)
86	PSEL	I	POR selection input (backup)
87	V_{DD5}	P	supply voltage 5 for output buffers
88	GND5	P	ground 5 for output buffers
89	$\overline{\text{FULLPOWER}}$	O	full power signal output (active LOW)
90	FH2	O	horizontal CCD transfer pulse output
91	FH1	O	horizontal CCD transfer pulse output
92	RG	O	reset output for CCD output amplifier gate
93	ROG	O	vertical CCD load pulse output
94	SMP	O	switch mode pulse output for CCD supply
95	H	O	horizontal synchronization pulse output
96	V	I/O	vertical synchronization pulse input/output
97	CRST	O	CCD charge reset output for shutter control
98	FV4	O	vertical CCD transfer pulse output
99	V_{DD6}	P	supply voltage 6 for output buffers
100	GND6	P	ground 6 for output buffers

Note

1. I = input, O = output and P = power supply.

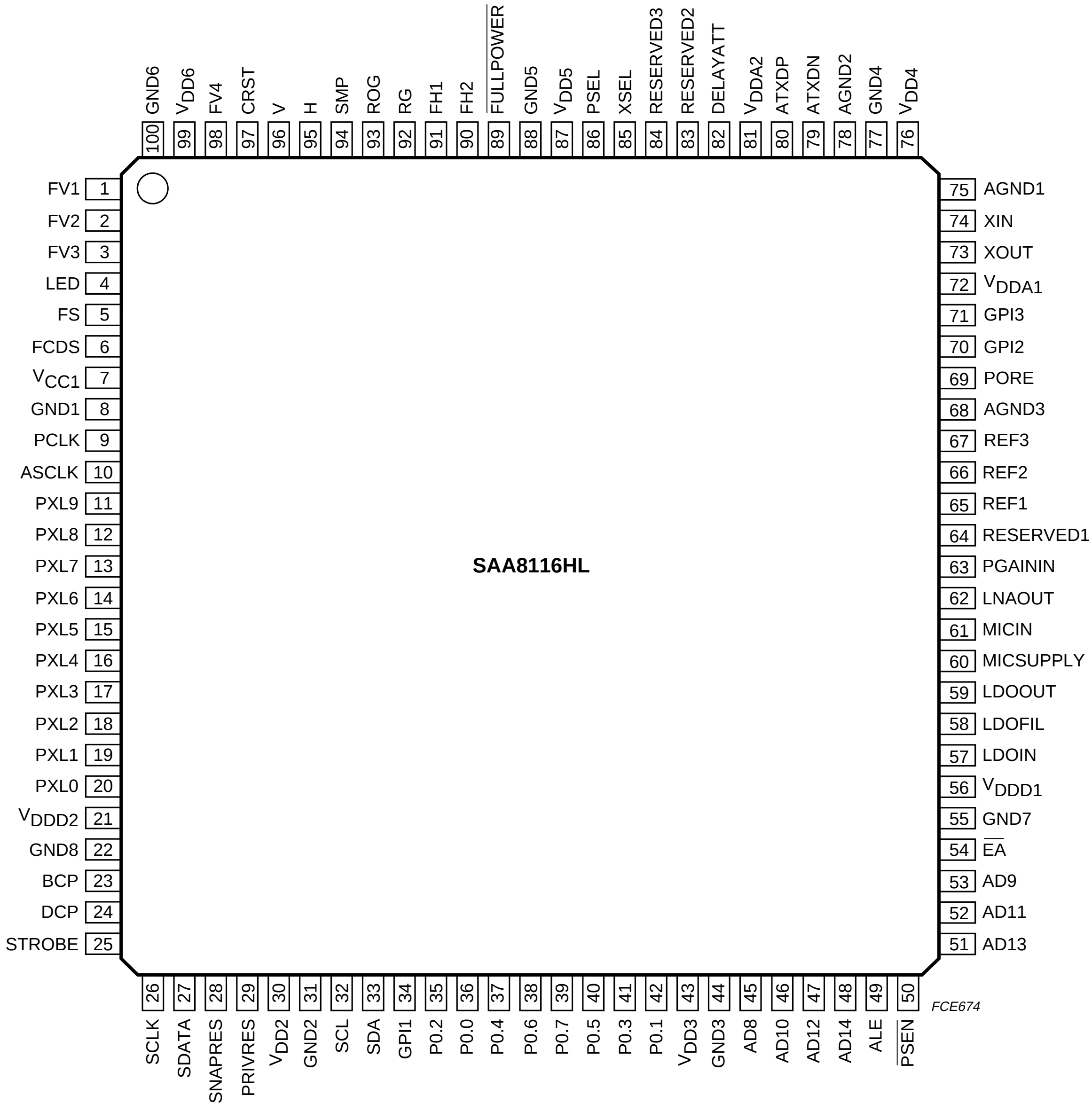


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); note 1.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+4.0	V
V_n	voltage on			
	pins GND and AGND	–0.5	+4.0	V
	all other pins	–0.5	V_{DD} + 0.5	V
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	ambient temperature	0	70	°C
T_j	junction temperature	–40	+125	°C

Note

1. Stress beyond these levels may cause permanent damage to the device.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	53	K/W

CHARACTERISTICS

$V_{DD} = V_{DDD} = V_{DDA}$ = 3.3 V ±10%; T_{amb} = 0 to 70 °C; unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		3.0	3.3	3.6	V
V_{DDD}	supply voltage for digital core		3.0	3.3	3.6	V
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
$I_{DDD(tot)}$	total digital supply current	$V_{DD} = V_{DDD}$ = 3.3 V; T_{amb} = 25 °C	–	–	75	mA
$I_{DDA(tot)}$	total analog supply current	V_{DDA} = 3.3 V; T_{amb} = 25 °C	–	–	16	mA
Digital data and control inputs						
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2	–	–	V
Digital data and control outputs						
V_{OL}	LOW-level output voltage		0	–	$0.1V_{DD}$	V
V_{OH}	HIGH-level output voltage		$0.9V_{DD}$	–	V_{DD}	V
LDO supply filter						
V_{ref}	reference voltage	at $0.5V_{DDA}$	–	1.50	–	V
V_O	output voltage on pin LDOUT	V_{DDA} = 3.0 V	–	3.0	–	V
I_O	output current on pin LDOUT		–	5	10	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Microphone supply						
I_{DDA}	supply current		–	0.85	1.2	mA
V_{ref}	reference voltage	at $0.5V_{DDA}$	–	1.50	–	V
V_O	output voltage on pin MICSUPPLY	V_{DDA} = 3.0 V	–	2.7	–	V
I_O	output current on pin MICSUPPLY		–	–	2.0	mA
Audio low noise amplifier						
TRANSFER FUNCTION						
R_i	input resistance		3.5	5.0	–	kΩ
I_{DDA}	supply current		–	0.85	1.2	mA
A	amplification		28	30	32	dB
THD	total harmonic distortion	note 1	–	–70	–60	dB
$V_{o(rms)}$	output voltage (RMS value)		–	–	800	mV
V_{OO}	output offset voltage		–	0.0	1.0	mV
BIASING						
I_{ref}	reference current		–	10	–	μA
Programmable audio gain amplifier						
TRANSFER FUNCTION						
R_i	input resistance		7.0	10.5	25	kΩ
I_{DDA}	supply current		–	0.45	0.6	mA
V_{OO}	output offset voltage	A = 0 dB	–	1.0	2.0	mV
		A = 30 dB	–	14	30	mV
A	amplification		0.0	–	30	dB
THD	total harmonic distortion	A = 0 dB; note 1	–	–83	–78	dB
		A = 30 dB; note 1	–	–59	–54	dB
BIASING						
I_{ref}	reference current		–	10	–	μA
Audio phase-locked loop						
$f_{i(clk)}$	clock input frequency		–	48	–	MHz
$f_{o(clk)}$	clock output frequency	note 2	–	8.19200	–	MHz
			–	11.2996	–	MHz
			–	12.2880	–	MHz
B	bandwidth		–	2.3	–	kHz
ζ	damping		–	0.98	–	
Audio ADC (ΣΔ converter)						
INPUTS						
f_i	input signal frequency		1	–	20	kHz
$V_{i(rms)}$	input voltage (RMS value)		–	800	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TRANSFER FUNCTION						
N	order of the $\Sigma\Delta$		–	3	–	
N_{bit}	number of output bits		–	1	–	
$N_{bit(eq)}$	equivalent output resolution (bit)		–	16	–	
DR_i	dynamic range at input	note 3	–	96.6	–	dB
f_{clk}	clock frequency		–	–	5.6448	MHz
δ	clock frequency duty factor		–	50	–	%
THD	total harmonic distortion		–	–70	–55	dB
ATX transceiver full speed mode: pins ATXDP and ATXDN						
DRIVER CHARACTERISTICS						
$t_{t(rise)}$	rise transition time	C_L = 50 pF	4	–	20	ns
$t_{t(fall)}$	fall transition time	C_L = 50 pF	4	–	20	ns
$t_{t(match)}$	transition time matching	note 4	90	–	110	%
V_{cr}	output signal crossover voltage		1.3	–	2.0	V
Z_o	driver output impedance	steady state drive	30	–	42	Ω
RECEIVER CHARACTERISTICS						
$f_{i(D)}$	data input frequency rate		–	12.00	–	Mbits/s
t_{frame}	frame interval		–	1.000	–	ms

Notes

1. The distortion is measured at HIGH level, 1 kHz and V_o = 800 mV (RMS).
2. Frequencies depend on PLL settings.
3. Defined here as: $20 \times \log \frac{\text{input voltage}}{\text{equivalent input noise voltage}}$
4. Transition time matching: $t_{t(match)} = \frac{t_{t(rise)}}{t_{f(fall)}} \times 100\%$

APPLICATION INFORMATION

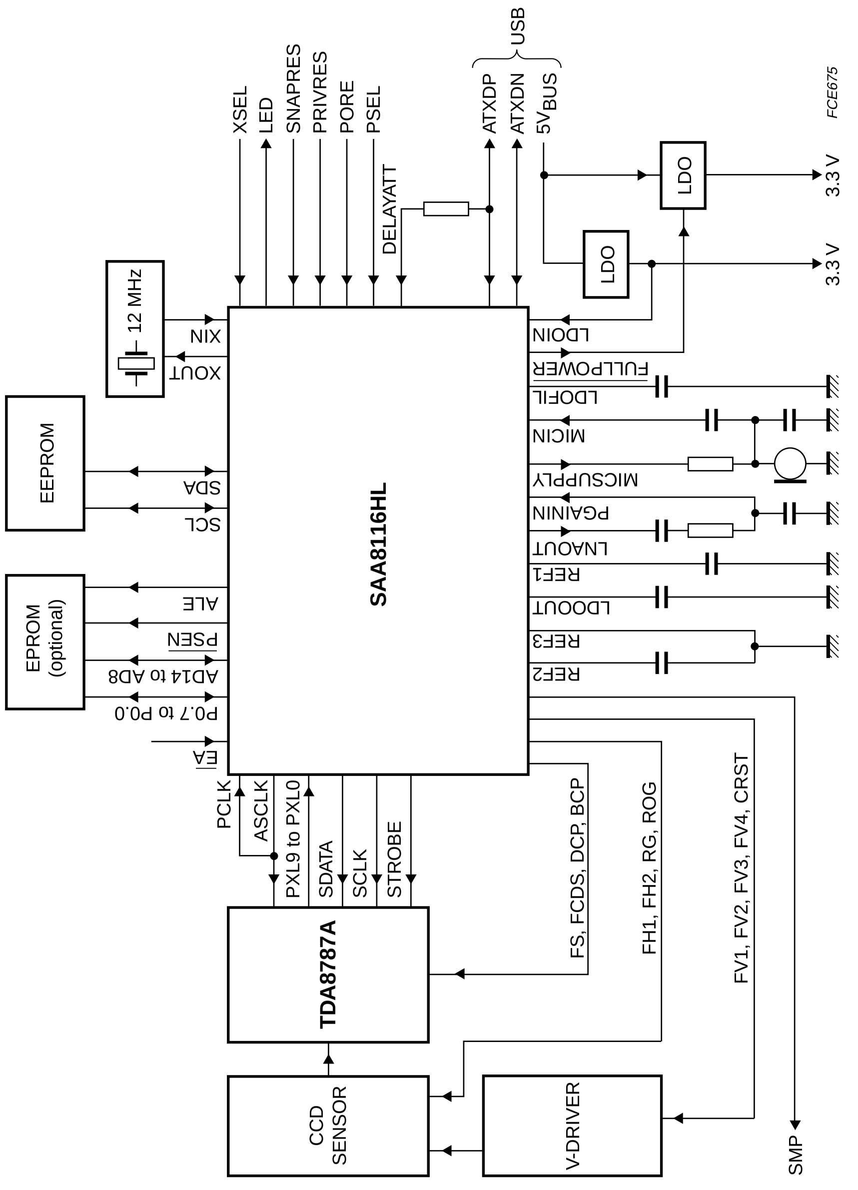


Fig.3 CCD sensor application.

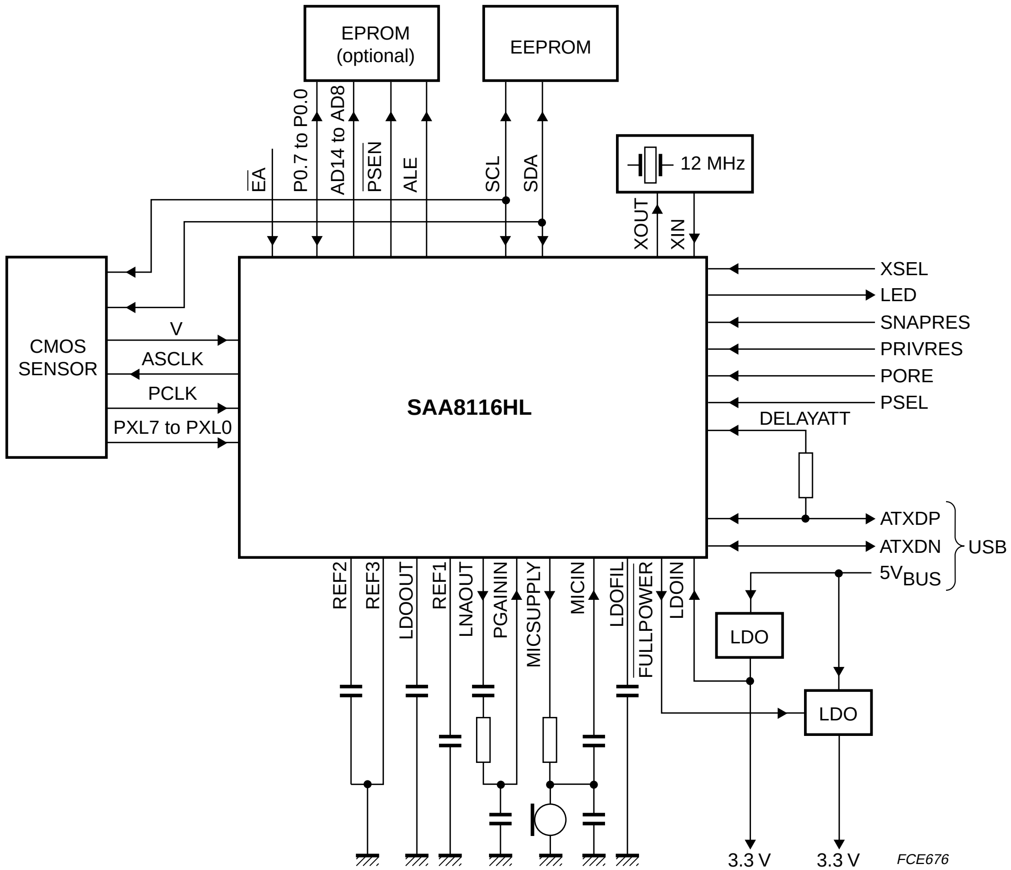
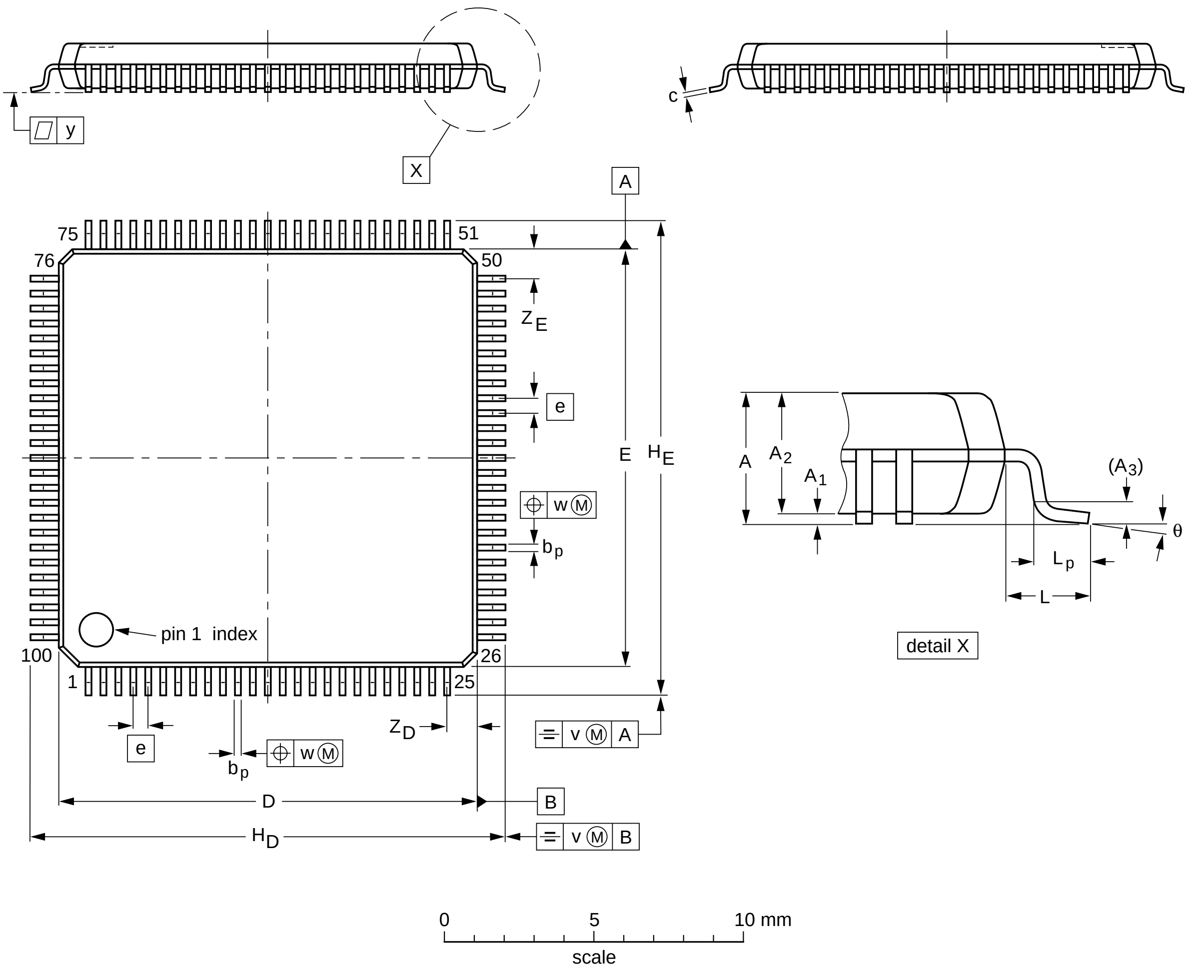


Fig.4 CMOS sensor application.

PACKAGE OUTLINE

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1.0	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT407-1	136E20	MS-026				~~00-01-19~~ 00-02-01

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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NOTES

NOTES

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