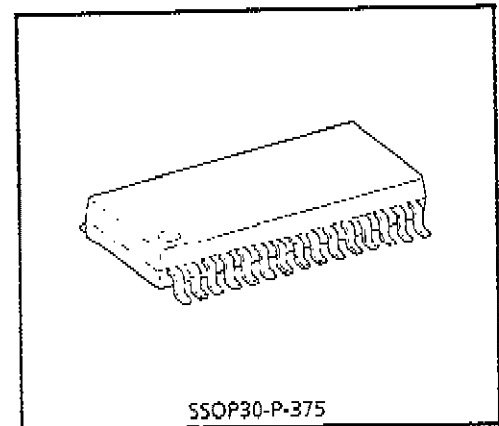


## FM DEMODULATION IC FOR BROADCASTING SATELLITE RECEIVER

The TA8804F combines the necessary function on a single monolithic integrated circuit to modulate FM signal of the 2nd IF of DBS.

### FEATURES

- 5V Power Supply
- 2nd IF AGC Amp
- dB-Linear Signal Level Amp
- PLL FM Detector
- Keyed AFT



Weight : 0.63g (Typ.)

© The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.

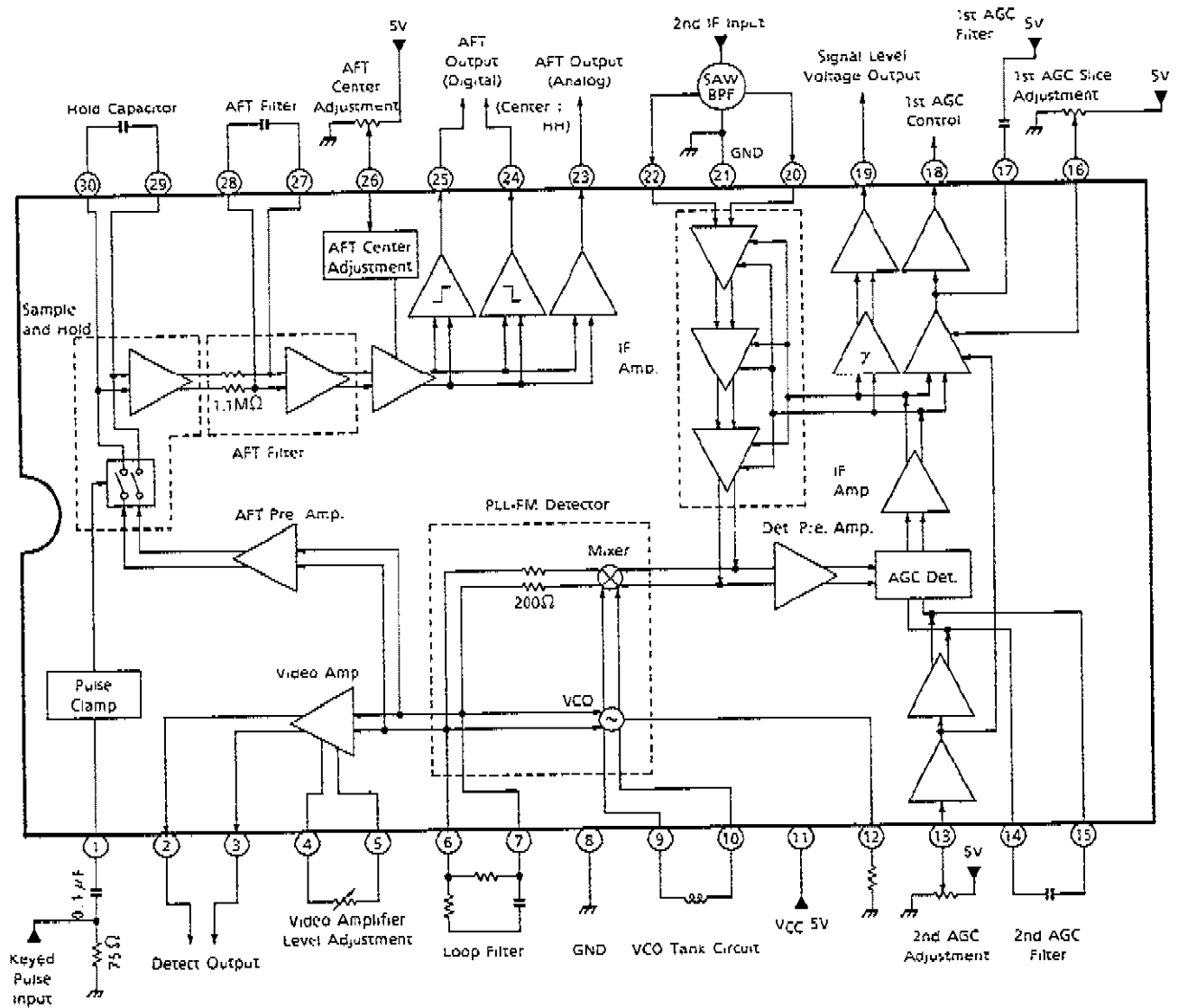
© These TOSHIBA products are intended for use in general commercial applications (office equipment, communication equipment, measuring equipment, domestic appliances, etc.) please make sure that you consult with us before you use these TOSHIBA products in equipment which requires extraordinarily high quality and/or reliability, and in equipment which may involve life threatening or critical application including but not limited to such uses as atomic energy control, airplane or spaceship instrumentation, traffic signals, medical instrumentation, combustion control, all types of safety devices, etc. TOSHIBA cannot accept and hereby disclaims liability for any damage which may occur in case the TOSHIBA products are used in such equipment or applications without prior consultation with TOSHIBA.

TA8804F - 1

1996 - 4 - 22

TOSHIBA CORPORATION

**BLOCK DIAGRAM**



**TERMINAL FUNCTION**

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
1	Keyed Pulse Input	<p>It clamps at the pulse peak and generates the reference level.</p> <p>The input impedance is <math>3k\Omega</math>.</p> <ul style="list-style-type: none"> <li>If any keyed pulse input, Keyed pulse : low level sample state Keyed pulse : high level hold state</li> <li>If no keyed pulse input, sample state at all time</li> </ul>	
2 3	Detect Output	<p>It outputs the detection output through a low-pass filter of 30MHz cut off frequency using an emitter follower.</p>	
4 5	Video Amplifier Level Adjustment	<p>It controls the level adjustment by varying the emitter resistance of a differential amplifier.</p> <p>If the resistance between pins 4 and 5 is reduced the output will be greater, however, since the output dynamic range is narrow the output level should be used in the range of lower than <math>0.7V_{p-p}</math>.</p>	
6 7	Loop Filter	<p>The output impedance is <math>200\Omega</math>.</p> <p>In the application circuit, <math>\omega \cong 174MHz</math> <math>\xi \cong 0.81</math></p>	

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
8	GND1	It is the GND of VCO circuit blocks that are VCO (pins 9, 10, 12), loop filter (pins 6, 7), video amplifier (pins 4, 5) AFT system (pins 1, 23, 24, 25, 26, 27, 28) and S/H (pins 29, 30).	-
9 10	VCO Coil	It is the VCO using variations in internal impedance of diode for control voltage from mixer. Use a UJ characteristic for the capacitor of the external tank circuit to correct the internal temperature drift.	
12	VCO Temperature Compensate Bias	The VCO bias is composed of a synthesis of bias in proportion to $V_{BE}$ and $V_T$ of transistor, and this terminal generates a bias proportioned to the $V_{BE}$ . If the external resistance reduced, the VCO sensitivity will rise.	
13	2nd AGC Adjustment	It changes the input level for a AGC detector. It adjusts by adding the direct current offset to pins 14 and 15. The variation width of about 8dB can be added. Internal bias is 2.5V.	

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
14 15	2nd AGC Filter	It generates the AGC voltage by filtering the 402.78MHz (479.5MHz) IF signal by means of an internal resistance and an external condenser. If applying the $V_{CC}$ to pin 15, the AGC will be minimum gain and the VCO oscillates at free-running frequency.	
16	1st AGC Slice Adjustment	It sets the input level threshold for generating the control signal to lower gain from the IC to the 2nd converter of front stage when excessive input. Even if the 2nd AGC adjustment varies, the 1st AGC adjustment point hardly changes. The internal bias is 2.5V.	
17	1st AGC Filter	It outputs by comparing with the AGC and 1st AGC slice level adjustment voltages. This comparator is constructed by the active load type high gain amplifier and determines its response by a capacitor connected to this terminal.	
18	1st AGC Control	It outputs the control voltage using an emitter follower (active low level). The internal current sink has only 25μA.	

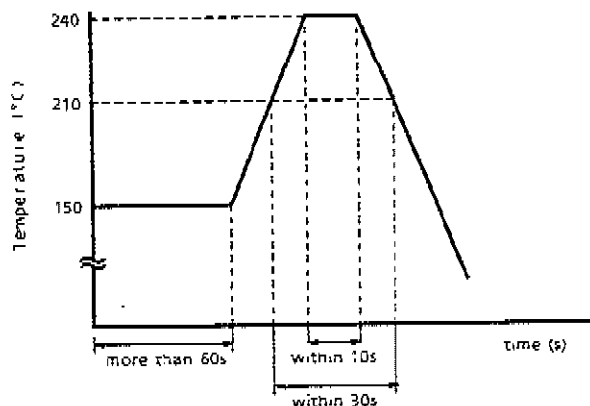
PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
19	Signal Level Out	It outputs the AGC voltage by doing logarithm <-> linear conversion. In the TA8804F the level detection can be carried out even after the 1st AGC is effective and input is reduced using the 1st AGC output.	
20 22	2nd IF In	The IF amplifier constructed by the 3-step series connection of variable gm type gain control, of which the maximum gain is 47dB and minimum gain - 8dB. In order to prevent a sneak of radio frequency all the circuits are balance-connected. Therefore, the differential combination is also desirable for the IC input. The internal bias is 2.0V and input impedance 1kΩ.	
23	AFT Output (Analog)	It outputs by integrating the detection output by means of pin 27 and 28 filters, doing center adjustment and multiplying about five times as much.	

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
24 25	AFT Output (Digital)	It outputs by converting the analog AFT output to binary with a comparator. In the case of center detection, the each output will be high level. The width of dead gone is determined by the internal threshold and VCO sensitivity, that cannot be adjusted externally.	
26	AFT Center Adjustment	It moves the AFT center frequency in the width of 10MHz and absorbs the center gap caused by dispersion of each AFT circuit.	
27 28	AFT Filter	It constructs a filter whose cut off frequency is less than 1Hz (capacitor : 0.7Hz at 0.1μF) with an internal 1.1MΩ resistance and external condenser.	
29 30	Hold Capacitor	Sample and hold by charge / discharging the condenser using the switching signal regenerated by keyed pulse.	

**MAXIMUM RATINGS (Ta = 25°C)**

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V <sub>CC</sub> MAX	6.0	V
Power Dissipation	P <sub>D</sub> MAX	1000	mW
Operation Temperature	T <sub>opr</sub>	-20~75	°C
Storage Temperature	T <sub>stg</sub>	-55~150	°C
Lead Temperature	—	260°C, 10s	

Recommended assembly method : Recommended temperature profile of reflow soldering of far and medium infrared rays



**RECOMMENDED POWER SUPPLY VOLTAGE**

PIN No.	PIN NAME	MIN.	TYP.	MAX.	UNIT
11	V <sub>CC</sub>	4.5	5.0	5.5	V



**ELECTRICAL CHARACTERISTICS**

DC CHARACTERISTICS (Unless otherwise specified,  $V_{CC} = 5.0V$ ,  $T_a = 25^\circ C$ )

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current	$I_{CC}$	1	—	55	80	105	mA
Terminal Voltage	Pin 1	$V_1$	—	2.0	2.5	3.0	V
	Pin 2	$V_2$	—	1.9	2.4	2.9	
	Pin 3	$V_3$	—	1.9	2.4	2.9	
	Pin 4	$V_4$	—	0.8	1.3	1.8	
	Pin 5	$V_5$	—	0.8	1.3	1.8	
	Pin 6	$V_6$	—	1.7	2.1	2.5	
	Pin 7	$V_7$	—	1.7	2.1	2.5	
	Pin 9	$V_9$	—	2.4	2.8	3.2	
	Pin 10	$V_{10}$	—	2.4	2.8	3.2	
	Pin 12	$V_{12}$	—	0.4	0.7	1.0	
	Pin 13	$V_{13}$	—	2.3	2.5	2.7	
	Pin 14	$V_{14}$	—	—	3.6	—	
	Pin 15	$V_{15}$	—	—	3.6	—	
	Pin 16	$V_{16}$	—	2.1	2.5	2.9	
	Pin 18	$V_{18h}$	Pin 17 : $1k\Omega$ -GND	—	1.0	1.3	
		$V_{18l}$	Pin 17 : $V_{CC}$	3.9	4.3	4.7	
	Pin 20	$V_{20}$	—	1.5	2.0	2.5	
	Pin 22	$V_{22}$	—	1.5	2.0	2.5	
	Pin 27	$V_{27}$	—	—	2.3	2.8	
	Pin 28	$V_{28}$	—	—	2.3	2.8	
Pin 29	$V_{29}$	—	1.8	2.3	2.8		
Pin 30	$V_{30}$	—	1.8	2.3	2.8		
Pin 2, 3 Acceptable Output Current	$I_2, I_3$	1	—	-1.0	—	6.0	mA
1'st AGC Output Current	$I_{18}$	1	—	-0.02	—	6.0	mA

AC CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
IF Input Frequency Range	$f_{in}$	—	—	350	400	550	MHz
IF Input Level Range	$V_{in}$	—	—	-60	—	-10	dBmW (50 $\Omega$ )
1st AGC Shoulder Level Range	AGC <sub>MAX</sub>	2	(Note 1)	—	-20	-10	dBmW (50 $\Omega$ )
1st AGC Control Sensitivity	$\Delta$ AGC	2	(Note 2)	1.0	3.5	6.0	V/dB
Signal Level Sensitivity	$\Delta V / \Delta V$	2	(Note 3)	10	35	60	mV/dB
VCO Conversion Sensitivity	$\beta$	2	Converting to output rate Pin 4, 5 : open / (Note 4)	—	110	130	MHz/V
VCO Temperature Drift	$\Delta f_{Ta}$	2	$T_a = -10 \sim 65^\circ\text{C}$ / (Note 5)	—	$\pm 1.0$	$\pm 2.5$	MHz
PLL Lock Range	$f_L$	2	(Note 6)	$\pm 25$	$\pm 30$	—	MHz
PLL Capture Range	$f_{ca}$	2	(Note 6)	$\pm 25$	$\pm 30$	—	MHz
Demodulation Output Level	$V_{out}$	2	$\Delta f = 10\text{MHz}_{p-p}$ / (Note 7)	0.15	0.26	0.40	$V_{p-p}$
Video Amplifier Variable Width	$V_{outS/5}$	2	Pin 4, 5 : short, 5k $\Omega$ / (Note 8)	10	14	—	dB
Demodulation Output Amplitude Frequency Characteristics 1	$V_{outA1}$	2	$f = 0.2 \sim 4\text{MHz}$ / (Note 9)	—	—	$\pm 0.5$	dB
Demodulation Output Amplitude Frequency Characteristics 2	$V_{outA2}$	2	$f = 4 \sim 9\text{MHz}$ / (Note 9)	—	—	$\pm 2$	dB
Group Delay Characteristics 1	$\tau_{pd1}$	2	$f = 0.2 \sim 4\text{MHz}$ / (Note 9)	—	—	$\pm 10$	ns
Group Delay Characteristics 2	$\tau_{pd2}$	2	$f = 4 \sim 9\text{MHz}$ / (Note 9)	—	—	$\pm 40$	ns
AFT Sensitivity	$\Delta f / \Delta V$	2	(Note 12)	2.4	3.2	4.0	MHz/V
S/H Sample Speed	$\Delta f_{spl}$	2	Converting to input frequency rate / (Note 10)	0.1	0.2	—	MHz / $\mu\text{s}$
Keyed AFT Input Range	$V_1$	2	—	0.35	0.5	0.65	$V_{p-p}$
Keyed AFT Input Frequency	$T_1$	2	(Note 11)	8.0	16.7	50	ms
AFT Width of Dead Zone	$V_{DEAD}$	2	(Note 13)	250	340	400	kHz
Digital AFT Voltage Low Level	$V_{20L}$	2	(Note 13)	—	0.3	0.5	V
DG	DG	application circuit	APL 90% / (Note 14)	—	$\pm 2.0$	$\pm 5.0$	%

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DP	DP	application circuit	APL 90% / (Note 14)	—	± 2.0	± 5.0	°
Inter-Modulation 2	IM2	application circuit	2.15MHz beat level / (Note 15)	40	45	—	dB
Inter-Modulation 3	IM3	application circuit	1.43MHz beat level / (Note 15)	40	50	—	dB
Video Output S/N	S/NSAT	application circuit	C/N = ∞	48	51	—	dB

**MEASUREMENT CONDITION**

(Note 1) 1st AGC Shoulder Level Range : AGC<sub>MAX</sub>

F = 402.78MHz input level  $v_{in} = 0$  to  $-40$ dBmW (50Ω) to pin 20. Measure  $v_{in}$  that pin 18 voltage is lower than 4V by opening pin 16 and raising  $v_{in}$ .

(Note 2) 1st AGC Control Sensitivity : ΔAGC

Input  $f = 402.78$ MHz  $v_{in} = 0$  ~  $-40$ dBmW (50Ω) to pin 20. Calculate  $v_{in}$  that pin 18 voltage is 4V/1V (as  $v_{in1}$ ,  $v_{in2}$ ), using the equation below.

$$\Delta AGC = -3 / (v_{in1} - v_{in2}) \quad V/dB$$

(Note 3) Signal Level Sensitivity : ΔV/ΔV

Measure each output voltage of pin 19 at  $v_{in} = -40$ ,  $-60$ dBmW (50Ω)

$$\Delta V / \Delta V = (V_{-60} - V_{-40}) / 20 \quad mV/dB$$

(Note 4) VCO Conversion Sensitivity : β

Input mainly  $f = 402.78$ MHz and sweep  $\pm 5$ MHz,  $v_{in} = -30$ dBmW (50Ω) to pin 20.

Calculate  $\beta = 10 / (V_{det+5} - V_{det-5})$  and multiply the gain portion (2.66) of video amplifier when outputting a direct current voltage to pin 3 at 407.78MHz, 397.78MHz as  $V_{det+5}$  and  $V_{det-5}$  each.

(Note 5) VCO Temperature Drift : Δf<sub>Ta</sub>

Short pin 6 and 7, and connect pin 14 to GND.

Measure the VCO frequency at ambient temperature  $T_a = 25^\circ C$ ,  $-10^\circ C$  +  $65^\circ C$  and calculate how much changes from  $25^\circ C$ . (read out the VCO leakage output by spectrum analyzer.)

(Note 6) PLL Lock Range : f<sub>L</sub>, Capture Range : f<sub>ca</sub>

Measure the range that synchronizes with VCO by putting pin 20 input frequency away from the free-running frequency.

(Note 7) Demodulation Output Level :  $V_{out}$

Input pin 20  $f = 402.78\text{MHz}$ ,  $f_m = 100\text{kHz}$ ,  $\Delta f = 10\text{MHz}_{p-p}$ ,  $v_{in} = -30\text{dBmW}$  ( $50\Omega$ )  
 Open pin 4 and 5 and measure the output level of pin 3.

(Note 8) Video Amplifier Variable Width :  $V_{outS}$ ,  $V_{out5}$

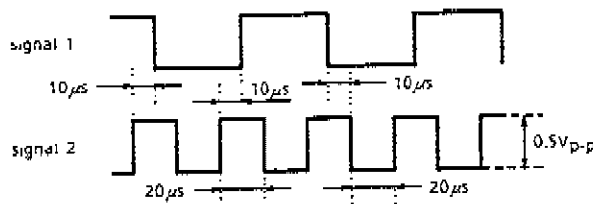
Input pin 20  $f = 402.78\text{MHz}$ ,  $f_m = 100\text{kHz}$ ,  $\Delta f = 10\text{MHz}_{p-p}$ ,  $v_{in} = -30\text{dBmW}$  ( $50\Omega$ )  
 Measure the variation of video output by shorting between pin 4 and 5 and connecting a  $5\text{k}\Omega$  resistance.

(Note 9) Demodulation Output level Width, Group Delay Characteristics :  $V_{outA}$ ,  $\tau_{pd}$

Input pin 20  $f = 402.78\text{MHz}$ ,  $f_m = 100\text{kHz}$ ,  $60\text{Hz}$  to  $4\text{MHz}$  to  $9\text{MHz}$ ,  $\Delta f = 5\text{MHz}_{p-p}$ ,  $v_{in} = -30\text{dBmW}$  ( $50\Omega$ )  
 Compare to the value at  $100\text{kHz}$  by opening pin 4 and 5, and measuring the output level and group delay of pin 3.

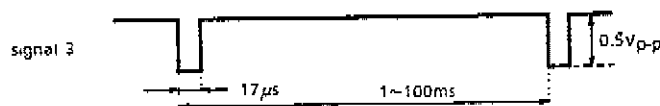
(Note 10) S/H Sample Speed :  $\Delta f_{sp}$

Input the signal 1 below for a modulation signal. Input the signal 2 below to pin 1. Observe the differential voltage waveform between pin 29 and 30, and measure the slew rate in the sampling period.



(Note 11) Keyed Pulse Allowable Period :  $T_1$

Input the signal below to pin 1 and open pin 27 and 28. Observe the pin 23 output and change  $f$  so as to be  $2.5\text{V}$  voltage.



Measure the frequency range in which a  $2\text{kHz}$  sine wave does not output to pin 23, by changing the signal 3 period.  
 If the sample-hold circuit malfunctions, the  $2\text{kHz}$  sine wave will be outputted from pin 23.

(Note 12) AFT Sensitivity :  $\Delta f / \Delta V_{23}$

Input pin 20  $f = 402.78\text{MHz} \pm 1\text{MHz}$ ,  $v_{in} = -30\text{dBmW}$  ( $50\Omega$ )

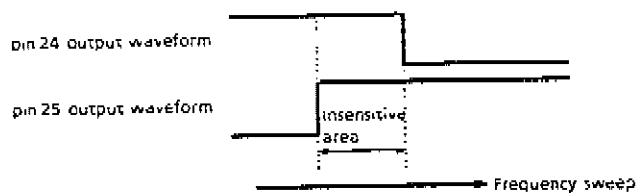
Adjust  $f$  so that pin 23 output will be 2.5V. By moving  $f$  up. and down, calculate each frequency as  $f_H$ ,  $f_L$  when pin 23 voltage varies 0.5V using the following equation.

$$\Delta f / \Delta V_{23} = f_H - f_L \text{ (MHz/V)}$$

(Note 13) AFT Digital Output Width of Blind Sector :  $f_{DEAD}$

Input pin 20  $f = 402.78\text{MHz} \pm 5\text{MHz}$ ,  $v_{in} = -30\text{dBmW}$  ( $50\Omega$ )

Measure the input frequency range in which both pin 24 and 25 become high level, by sweeping  $f$ .



(Note 14) DG, DP

Input pin 20  $f = 402.78\text{MHz} \pm 5\text{MHz}$ ,  $v_{in} = -30\text{dBmW}$  ( $50\Omega$ ),  $\Delta f = 17\text{MHz}_{p-p}$ , Gray level video signal (APL : 10~90%)...Pre-emphasis-on

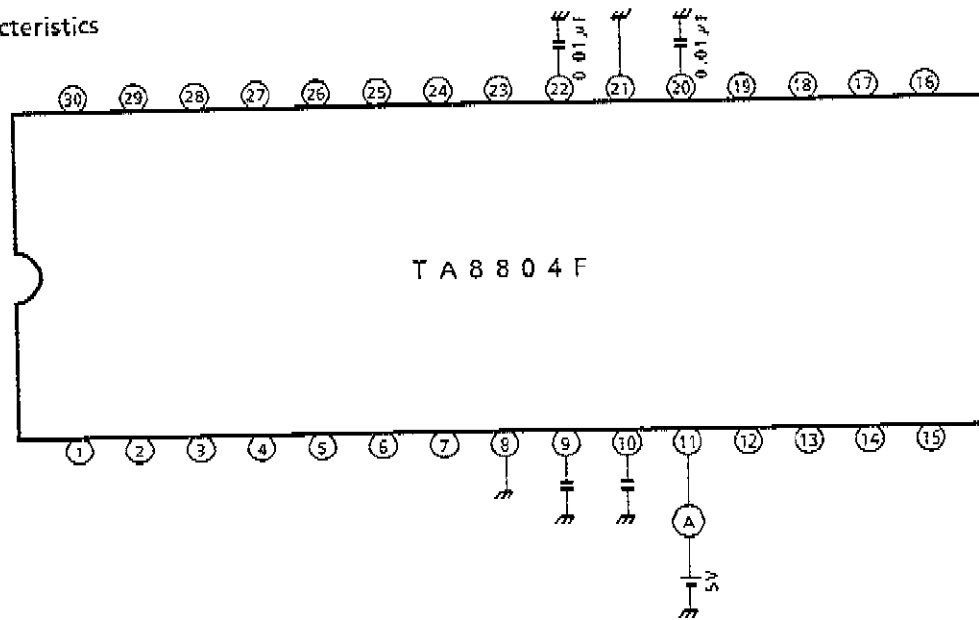
(Note 15) IM2, IM3

Input pin 20  $f = 402.78\text{MHz} \pm 5\text{MHz}$ ,  $v_{in} = -30\text{dBmW}$  ( $50\Omega$ ),  $\Delta f = 17\text{MHz}_{p-p}$ . Color subcarrier (3.579MHz), Sound subcarrier (5.7272MHz) ...

Observe the frequency component outputting to the screen output pin (pin 3) through the video gate of a video noise meter by spectrum analyzer, and measure the level difference between 3.579MHz component and 2.15MHz, 1.43MHz components.

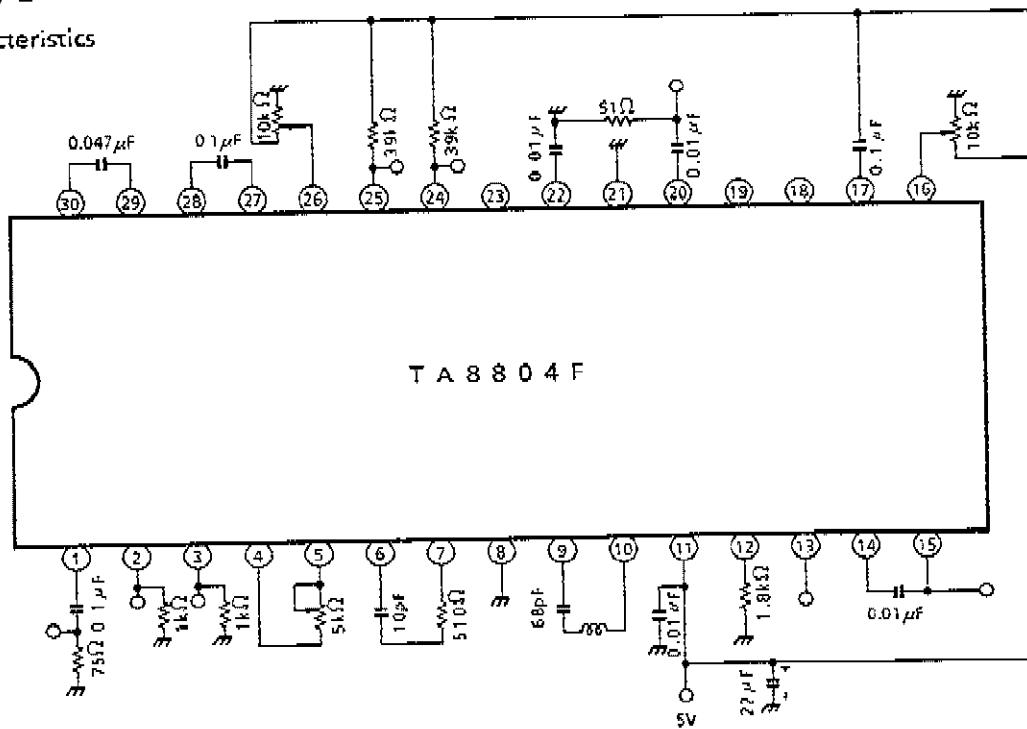
**TEST CIRCUIT 1**

DC characteristics



**TEST CIRCUIT 2**

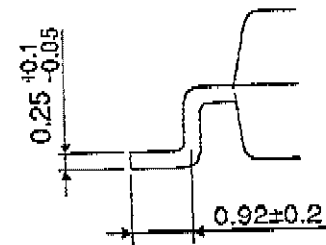
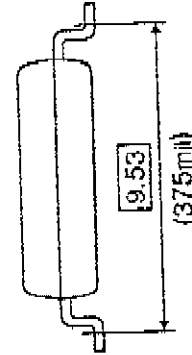
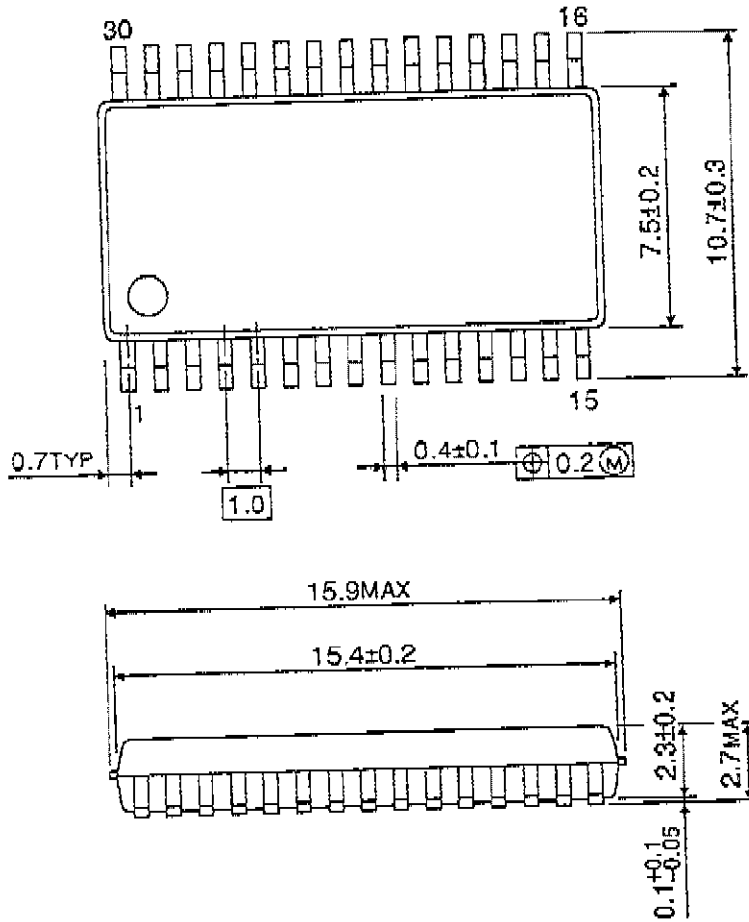
AC characteristics





OUTLINE DRAWING  
 SSOP30-P-375

Unit : mm



Weight : 0.63g (Typ.)