CMC7101A Low Power Operational Amplifier, RRIO, SOT23-5

Features

- Tiny SOT23-5 package
- Guaranteed specs at 2.7V, 3V and 5V
- Low supply current typically 300μA
- Rail-to-Rail input and output (RRIO)
- Typical total harmonic distortion of 0.01% at 5V
- 1.0MHz gain-bandwidth
- Input common mode range includes V- and V+

Applications

- Mobile Communications
- Cellular Phones
- Portable Equipment
- Notebooks and PDAs

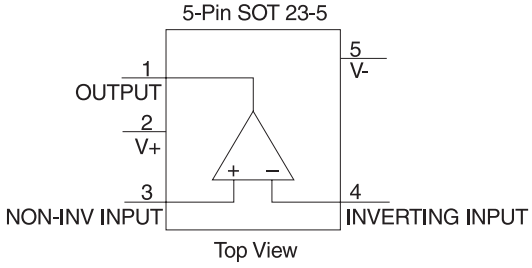
Product Description

The CMC7101A is a high performance CMOS operational amplifier available in a small SOT23-5 package. Operating with low supply current, it is ideal for battery operated applications where power, space and weight are critical.

Performance is compatible to the industry standard "7101" SOT Amp, with enhancements of reduced supply current, much higher output drive current, and enhanced operation at low supply voltage (2.7V). It is the economical solution for 3V to 5V applications.

Ideal for use in personal electronics such as cellular handsets, pagers, cordless telephones, and other products with limited space and battery power.

CONNECTION DIAGRAM



Top View

STANDARD PART ORDERING INFORMATION				
Package		Ordering Part Number		
Pins	Style	Tubes	Tape & Reel	Part Marking
5	SOT23-5	CMC7101AY/T	CMC7101AY/R	01A

ABSOLUTE MAXIMUM RATINGS (Note 1)		
Parameter	Rating	Unit
ESD Tolerance (see note 2)	2,000	V
Differential Input Voltage	± Supply Voltage	V
Voltage at Input /Output Pin	(V+) + 0.3V, (V-) -0.3V	V
Supply Voltage (V+ to V-)	7.5	V
Current at Input Pin	5	mA
Current at Output Pin (see note 3)	35	mA
Current at Power Supply Pins	35	mA
Lead Temp. (soldering, 10sec.)	260	ºC
Storage Temperature Range	-65 to +150	ºC
Junction Temp. (see note 4)	150	ºC

OPERATING CONDITIONS (unless specified otherwise)		
Parameter	Rating	Unit
Supply Voltage	$2.7 \leq V+ \leq 7$	V
Junction Temp. Range	$-40 \leq T_J \leq +85$	°C
Thermal Resistance	325	°C / W

2.7V ELECTRICAL OPERATING CHARACTERISTICS

Unless otherwise specified, all limits guaranteed for T_J=25°C, V+ =2.7V, V- = 0V, R_L > 1MΩ

Symbol	Parameter	Conditions	TYP	LIMIT	UNIT
V_{OS}	Input Offset Voltage		0.11	6	mV
TCV_{OS}	Input Offset Voltage Average Drift		1		µV/°C
I_B	Input Bias Current		1		pA
I_{OS}	Input Offset Current		0.5		pA
R_{IN}	Input Resistance		1		TΩ
CMRR	Common-Mode Rejection Ratio	$0V \leq V_{CM} \leq 2.7V$	70	55	dB
V_{CM}	Input Common Mode Voltage Range	V + = V	0	0	V
		For CMRR > 50dB	3.0	2.7	V
PSRR	Power Supply Rejection Ratio	V+ = 1.35V to 1.65V V- = -1.35V to -1.65V V_{CM} = 0	60	50	dB
C_{IN}	Common-Mode Input Capacitance		3		pf
V_O	Output Swing	R_L = 600Ω	2.60		V
			0.10		V
		R_L = 2KΩ	2.60	2.15	V
			0.10	0.5	V
		R_L = 10KΩ	2.68	2.64	V
			0.02	0.06	V
I_S	Supply Current		0.300	0.81	µA
SR	Slew Rate		0.7		V/µs
GBW	Gain Bandwidth Product		0.6		MHz

3V ELECTRICAL OPERATING CHARACTERISTICS

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V+ = 3V, V- = 0V, R_L > 1MΩ

Symbol	Parameter	Conditions	TYP	Limit	UNIT
V_{OS}	Input Offset Voltage		0.11	4	mV
TCV_{OS}	Input Offset Voltage Average Drift		1		µV/°C
I_B	Input Bias Current		1		pA
I_{OS}	Input Offset Current		0.5		pA
R_{IN}	Input Resistance		1		TΩ
CMRR	Common-Mode Rejection Ratio	0V < V_{CM} < 3V	74	64	dB
V_{CM}	Input Common Mode	V+ = V	0	0	V
	Voltage Range	For CMRR > 50dB	3.3	3.0	V
PSRR	Power Supply Rejection Ratio	V+ = 1.5V to 1.8V V- = -1.5V to -1.8V V_{CM} = 0	80	68	dB
C_{IN}	Common-Mode Input Capacitance		3		pF
V_O	Output Swing	R_L = 600Ω	2.9	2.6	V
			0.1	0.4	V
		R_L = 2KΩ	2.9	2.6	V
			0.1	0.4	V
		R_L = 10KΩ	2.99	2.7	V
			0.01	0.3	V
I_S	Supply Current		0.3	0.81	mA
SR	Slew Rate		0.7		V/µS
GBW	Gain Bandwidth Product		0.6		MHz

5V ELECTRICAL OPERATING CHARACTERISTICS

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V+ = 5V, V- = 0V, R_L > 1MΩ

Symbol	Parameter	Conditions	TYP	LIMIT	UNIT
V_{OS}	Input Offset Voltage	V+ = 5V	0.11	3	mV
TCV_{OS}	Input Offset Voltage Average Drift		1		µV/°C
I_B	Input Bias Current		1		pA
I_{OS}	Input Offset Current		0.5		pA
R_{IN}	Input Resistance		1		TΩ
CMRR	Common-Mode Rejection Ratio	0V < V_{CM} < 5V	82	65	dB
V_{CM}	Input Common-Mode	V+ = V	-0.3		V
	Voltage Range	For CMRR > 50dB	5.3		V
PSRR	Power Supply Rejection Ratio	V+ = 2.5V to 2.8V V- = -2.5V to -2.8V V_{CM} = 0	82	70	dB
C_{IN}	Common-Mode Input Capacitance		3		pF
V_0	Output Swing	R_L = 600Ω	4.9	4.5	V
			0.1	0.5	V
		R_L = 2KΩ	4.9	4.7	V
			0.1	0.18	V
		R_L = 10KΩ	4.99	4.8	V
			0.01	0.15	V
I_{SC}	Output Short Circuit Current	Sourcing V_0 = 0V (see note 5)	100	16	mA
		Sinking V_0 = 5V (see note 5)	80	11	mA
I_S	Supply Current		0.3	0.85	mA
T.H.D.	Total Harmonic Distortion	f = 10kHz, Av = -2 R_L = 10kΩ, Vo = 4.0Vpp	0.01		%
SR	Slew Rate		1.0		V/µs
GBW	Gain Bandwidth Product		1.0		MHz

Note 1 Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating conditions indicate ratings for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2 Human body model, 1.5KΩ in series with 100pF.

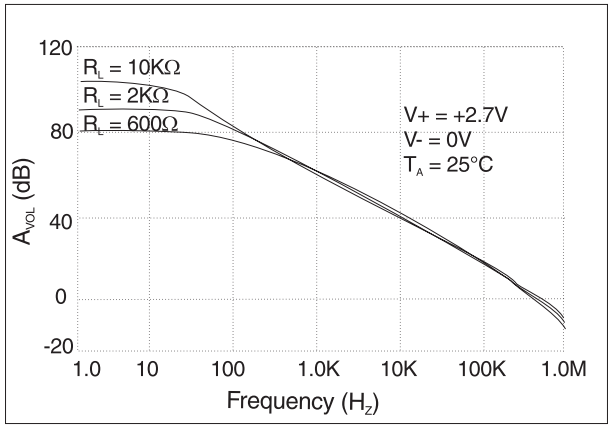
Note 3 Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperatures can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4 The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is PD = $(T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly to a PC board.

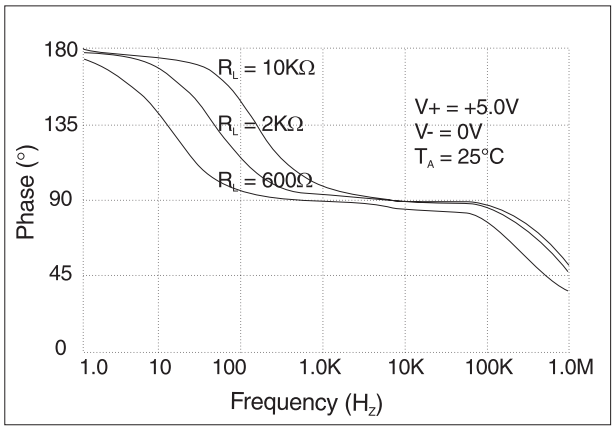
Note 5 See Application Section

TYPICAL PERFORMANCE CHARACTERISTICS

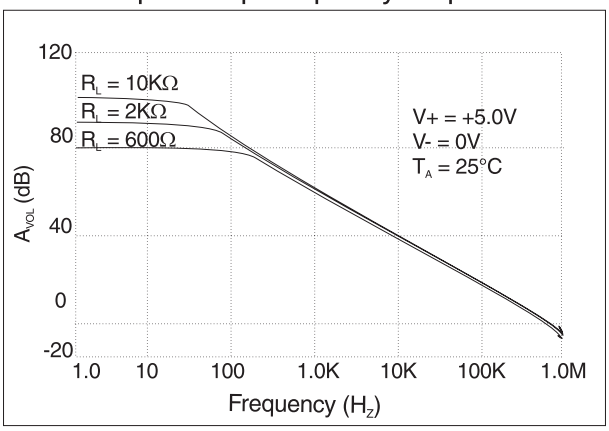
Open Loop Frequency Response



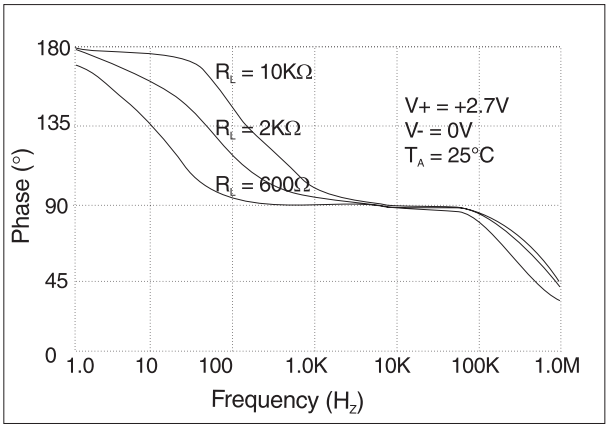
Open Loop Phase Response



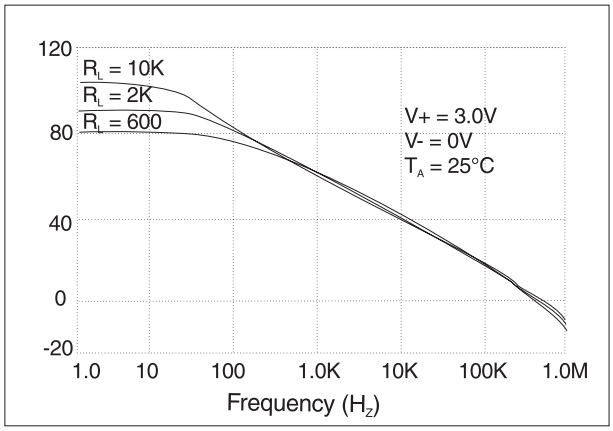
Open Loop Frequency Response



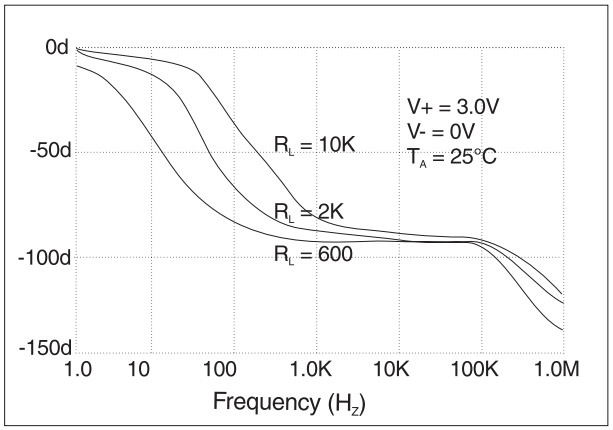
Open Loop Phase Response



Open Loop Frequency Response

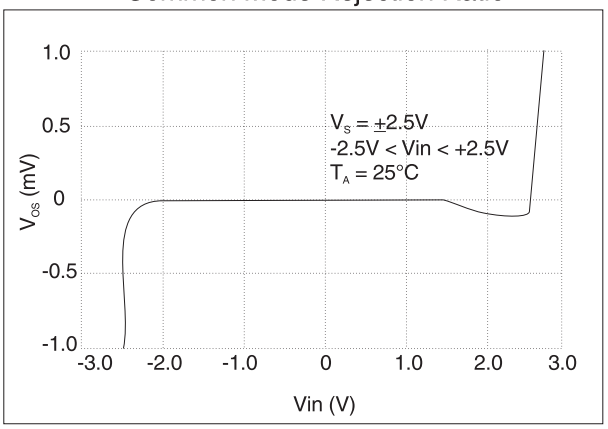


Open Loop Phase Response

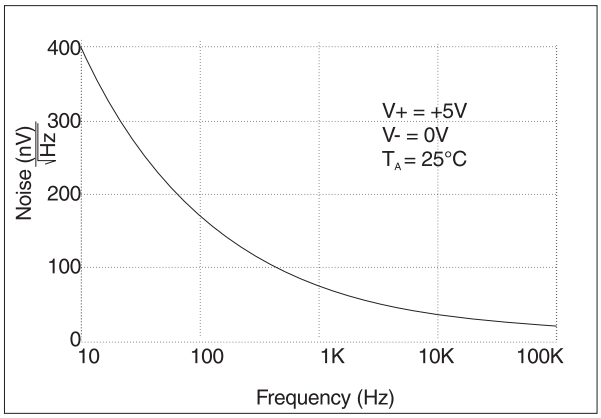


TYPICAL PERFORMANCE CHARACTERISTICS

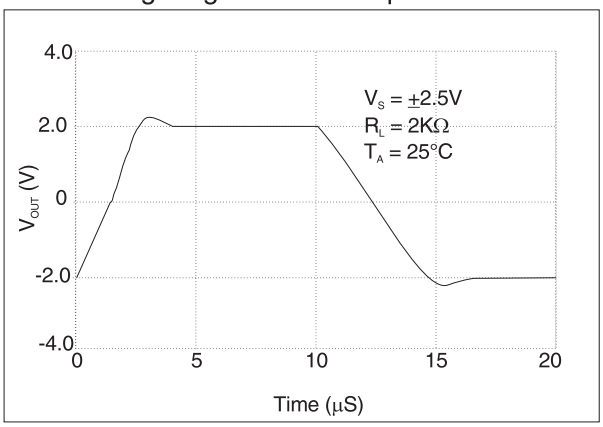
Common Mode Rejection Ratio



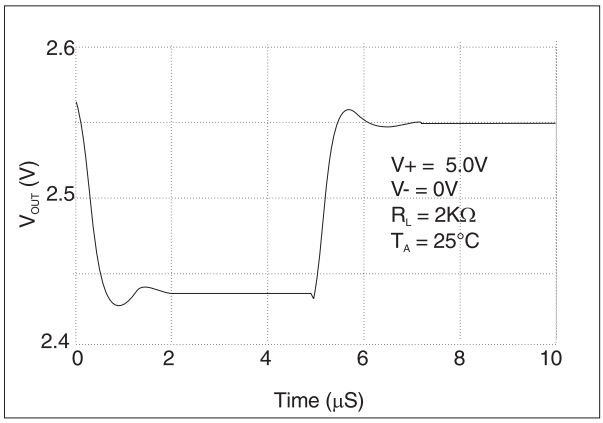
Input Noise Voltage Vs. Frequency



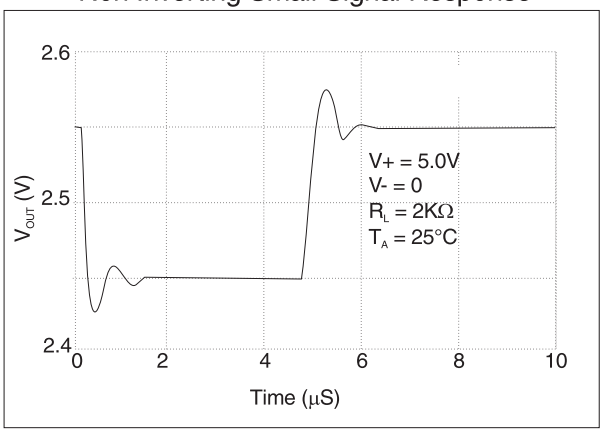
Large Signal Pulse Response



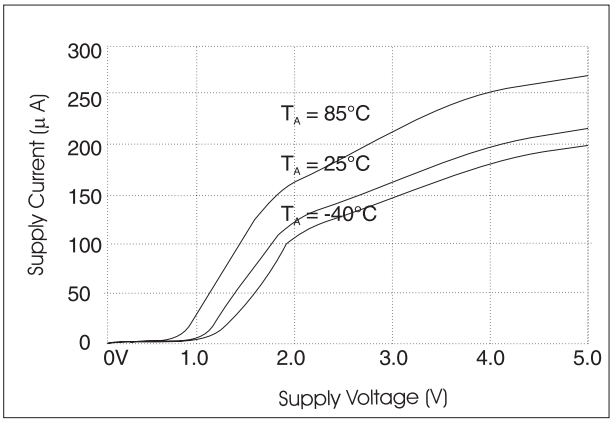
Inverting Small Signal Response



Non Inverting Small Signal Response

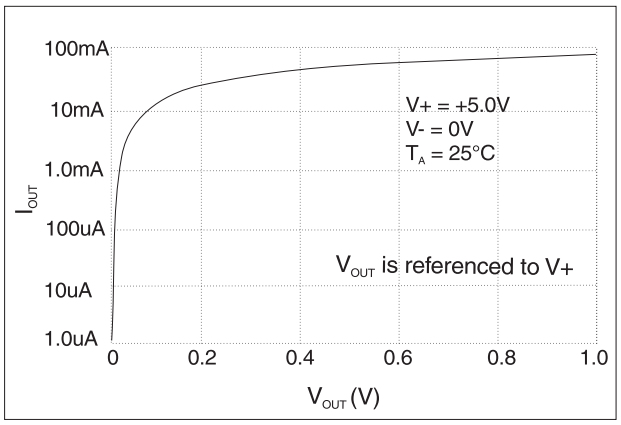


Supply Current Versus Supply Voltage

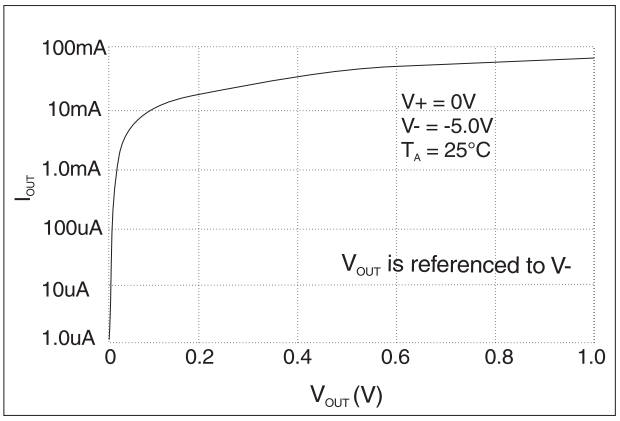


TYPICAL PERFORMANCE CHARACTERISTICS

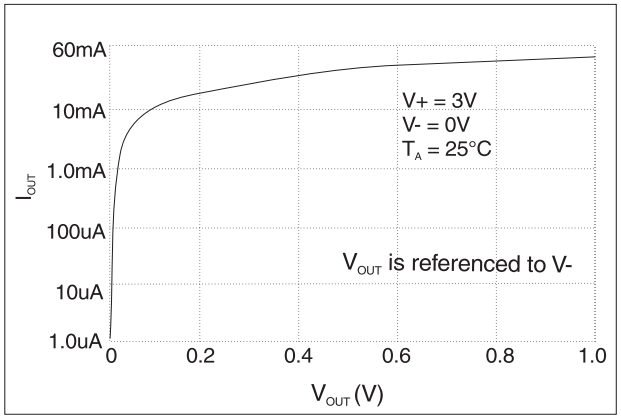
Current Sourcing Versus V_{OUT}



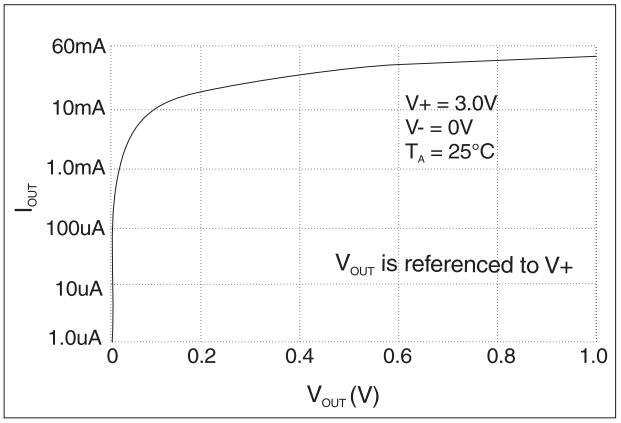
Current Sinking Versus V_{OUT}



Current Sinking Versus V_{OUT}



Current Sourcing Versus V_{OUT}



Application Benefits

1.0 Packaging

Most of the benefits of the CMC7101A are due to the use of a SOT package. The industry has readily adopted the SMT package technique and a SOT23-5 footprint is an easy way to save space. This leads to smaller finished products.

PC CARDS (PCMCIA type III cards) require low profile components. At 0.056 inches (1.43 mm), the CMC7101A is ideal.

1.1 Signal Integrity

As products become smaller, the natural space used to isolate circuits is lost. Signals can interact or pick up noise in these designs. By using a physically smaller amplifier package, the CMC7101A can be placed closer to the signal source, reducing noise pickup, and its small size makes it a simple buffer.

Rail to Rail Inputs and Output allow the amplifier to operate from lower supplies and also maintain signal level swings under large signal amplitude conditions.

1.2 Simplified Board Layout

Board layout is helped in a couple of ways due to the small size. Op Amps can be placed where amps are needed, shortening signal paths and PCB traces subject to noise pick up. Compared to a dual or quad device, two or four strategically placed SOT AMPs reduce cross-talk and avoid long PC wiring traces.

1.3 Lower Distortion

The CMC7101A has lower distortion than other SOT Amps, which combined with the high open loop gain allows it to achieve very low audio signal distortion.

1.4 Lower Power Supply Current Drain

The CMC7101A has lower power supply drain than other SOT Amps, making the part an instant upgrade to industry standard '7101' applications. Lower supply current means longer operation in battery operated products, and simpler power supply regulator or converter designs when many amplifiers are used in one system.

1.5 Higher Output Drive

The CMC7101A has higher output current than other SOT Amps, making the part an instant upgrade to industry standard '7101' applications. Higher output current means that existing circuits can start up sooner when power is applied (due to output current charging load capacitance), a feature needed when sections of a system are powered down frequently to save power or reduce cross-talk, such as a cellular handset.

Application Trouble Shooting

2.0 Input Common Mode Range and Output Voltage Considerations

The CMC7101A is capable of accommodating input common mode and output voltages equal to both power supply rails. Nor will voltages that exceed the supply voltages cause phase inversion of the output. However, ESD diode clamps are provided at the inputs that can be damaged if static currents in excess of ± 5 mA are allowed to flow through them. This can occur when the magnitude of input voltage exceeds the rail by more than 0.3 volt. To preclude damage, an current limiting resistor, R_s, in series with the input is recommended as illustrated in Figure 1 whose value for R_s is given by:

$$R_s > \frac{Vin - (V+ + 0.3\ V)}{5\ mA} \quad \textbf{(1)}$$

For V+ (or V-) equal to 2.7 volts and Vin equal to 10 volts, Rs should be chosen for a value of 1.5 KΩ or greater.

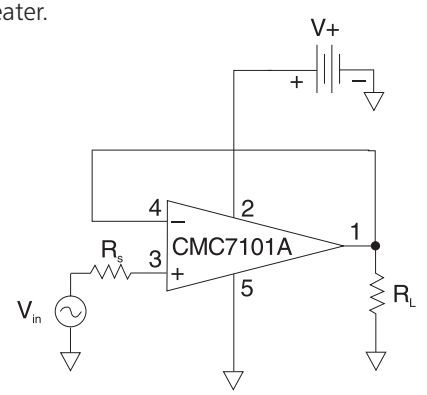


Figure 1 R_s Input Current Protection

2.1 Output Current and Power Dissipation Considerations

The CMC7101A is capable of sinking and sourcing output currents in excess of 75 mA at voltages very nearly equal to the rails. As such, it does not have any internal short circuit protection (which would in any event detract from its rail to rail capability). Accordingly, power dissipation and junction temperature should be considered in any application.

Obviously, the worst case from a power dissipation point of view is when the output is shorted to either ground in a single rail application or to the opposite supply voltage in split rail applications. Since this device only draws 300 micro Amps supply current, its contribution to the junction temperature, T_J, is negligible. As an example, let us analyze a situation in

which the CMC7101A is operated from a +5 volt supply, the output is "programmed" to positive saturation, and the output pin is indefinitely shorted to the opposite rail. In general:

$$P_{diss} = (V+ - Vout) * Iout \quad \textbf{(2)}$$

Where: P_{diss} = Power dissipated by the chip
$V+$ = Supply voltage
$Vout$ = The output voltage

In this example, V+ – Vout would equal 2.5 V– (-2.5 V) = 5 V, and power dissipation would be equal to 375 mW.

$$T_J = T_A + \theta_{JA} * P_{diss} \quad \textbf{(3)}$$

Where: T_A = The ambient temperature
θ_{JA} = The thermal impedance of the package junction to ambient

The SOT23 exhibits a θ_{JA} equal to 325 °C/W. Thus for our example the junction temperature rise would be about 122°C which is nearly a destructive situation since the maximum junction temperature rating is 150 °C. Under normal operating conditions with a resistive load, equations (2) and (3) may be used to determine T_J. For example, for Vout = 1.35 volts, V+ = 2.7 volts, V- = ground, and a load of 20 mA, P_{diss} = 27 mW with a corresponding junction temperature rise of a mere 9 °C. If the ambient temperature is 85 °C maximum, the junction temperature is a safe 94 °C.

2.2 Input Impedance Considerations

The CMC7101A exhibits an input impedance typically in excess of 1 Tera Ω (1 X 10^{12} ohms) making it very appropriate for applications involving high source impedance such as photodiodes and high output impedance transducers or long time constant integrators. High source impedances usually dictate large feedback resistors. But, the output capacitance of the source in parallel with the input capacitance of the CMC7101A (which is typically 3 pF) creates a parasitic pole with the feedback resistor which erodes the phase margin of the amplifier. The usual fix is to bypass, R_f, as shown in Figure 2 with a small capacitor to cancel the input pole. The usual formula for calculating C_f always results in a value larger than required:

$$\frac{1}{2 \pi R_s C_s} \geq \frac{1}{2 \pi R_f C_f} \quad \textbf{(4)}$$

Since the parasitic capacitance can change between the breadboard and the production printed circuit board, we favor the use of a "gimmick" , a technique perfected by TV technicians in the 1950's. A gimmick is made by taking two lengths (typically about a foot) of small gauge insulated wire such as AWG 24, twisting them together, and then after baring all ends soldering the gimmick across R_f. With the circuit operating, C_f is "adjusted" by clipping short lengths of the gimmick off until the compensation is nominal. Then simply remove the gimmick, take it to an impedance bridge, and select the capacitor accordingly.

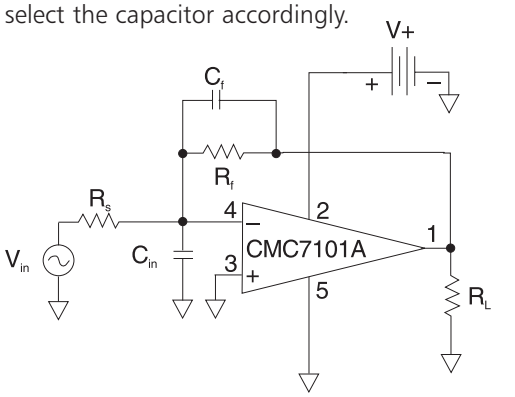


Figure 2 C_F High Frequency Compensation

2.3 Capacitive Load Considerations

The CMC7101A is capable of driving capacitive loads in excess of 100 pF without oscillation. However, significant peaking will result. Probably the easiest way to minimize this problem is to use an isolation resistor as shown in Figure 3.

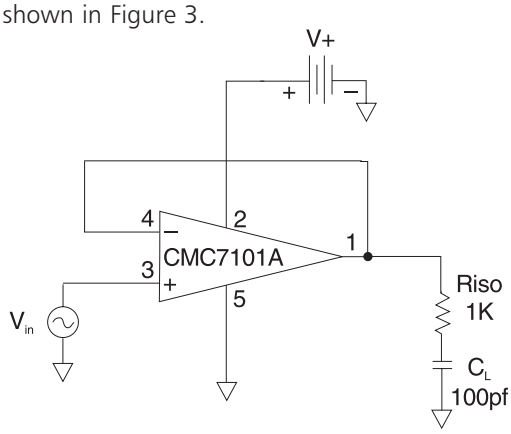


Figure 3 Riso Capacitive Load Isolation

2.4 Power Supply Decoupling

The CMC7101A is not prone to oscillation without the use of power supply decoupling capacitors, however to minimize hum and noise pick-up, it is recommended that the rails be bypassed with 0.01 micro farad capacitors.

CMC7101A Benefits

3.0 High Side Current Sense

To monitor a load current it is necessary to insert a current sense resistor in the power supply feed, as shown in figure 4. The resulting voltage drop is proportional to the load current, but as both ends of this resistor are at (or very near to) the supply voltage, it is difficult to use a conventional Op Amp.

The CMC7101A is ideal for this application as the inputs can operate at either supply rail (or at ground when used with a single supply). The output voltage is directly proportional to current in the load, scaled by the gain of the amplifier.

To reduce the power loss in the sense resistor and also keep the supply voltage to the load immune to load current variations, a small value Rsense is used.

An excellent application for this circuit is in a battery charger, where the charging current is monitored to detect end of charge (battery current will rise as the cells 'top off'), and charging must be reduced to prevent damage (out gassing or over heating).

The sense resistor can be placed in the negative side (known as Low Side Sensing), however this is less desirable due to disruption of the ground path.

3.1 Rail To Rail Output Swing

Making smaller and lighter products requires the reduction of battery size, lowering of battery voltage, or both. The lower voltage products have less headroom, for a given signal swing, and this demands better amplifier performance. Rail To Rail Outputs help maintain the existing signal level when products are redesigned for lower voltage supplies.

3.2 Rail to Rail input Swing

When the amplifier is used as a buffer, the input of the amplifier follows the input signal and if this is large compared to the available supply voltage, it is important that the Op Amp has a wide CMVR (Common Mode Voltage Range). RRIO Op Amps have a CMVR equal (or greater than) the supplies and this allows large signal swings without clipping or distortion.

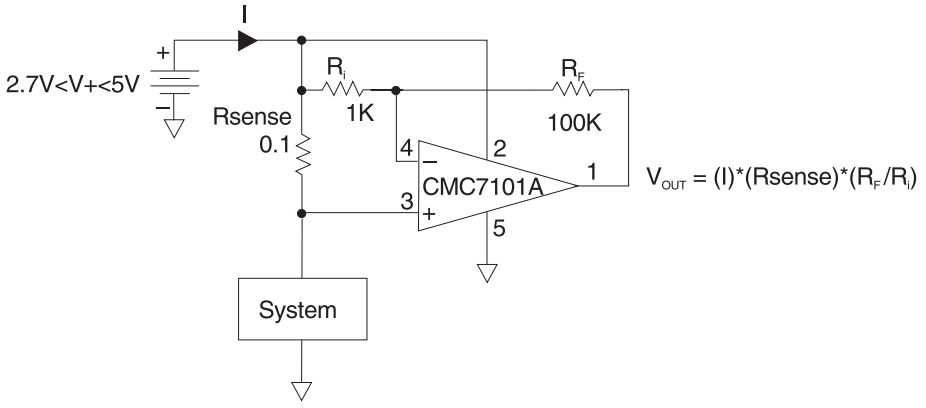


Figure 4 High Side Current Sense circuit

CMC7101A Physical Dimensions

For a complete mechanical drawing refer to http://www.calmicro.com/prod/data/package/sot-23.htm.