

FAN8403D3

3-Phase BLDC Motor Driver with PLL

Features

- 3-Phase BLDC motor drive IC with speed control
- Phase Locked Loop (PLL) speed control
- Built-in phase locked detector output
- External clock for control of motor speed
- Built-in FG amplifier and FG schmidt comparator
- Built-in integrating amplifier with phase error
- Auto Gain Control (AGC) circuit for compensation hall amplifier
- Built-in protection circuits (over-current limit, under-voltage limit, thermal shut down)

Description

The FAN8403D3 is a monolithic integrated circuit. It is suitable for polygon mirror motor of laser beam printer (LBP).

28-SSOPH-375SG2



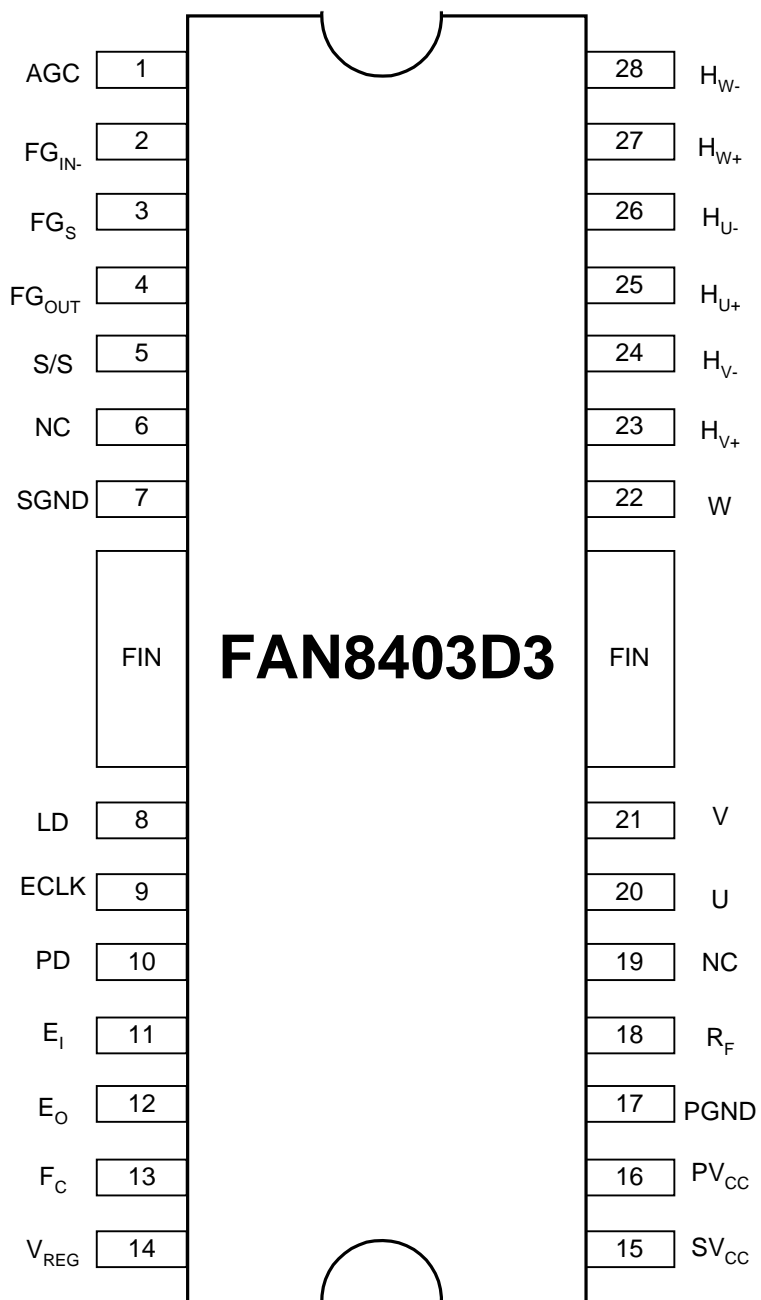
Typical application

- Polygon mirror motor for laser beam printer
- Polygon mirror motor for facsimile
- Polygon mirror motor for duplicator
- Polygon mirror motor for multi-function printer
- General 3 phase BLDC motor

Ordering Information

Device	Package	Operating Temp.
FAN8403D3	28-SSOPH-375SG2	-20°C ~ +80°C
FAN8403D3TF	28-SSOPH-375SG2	-20°C ~ +80°C

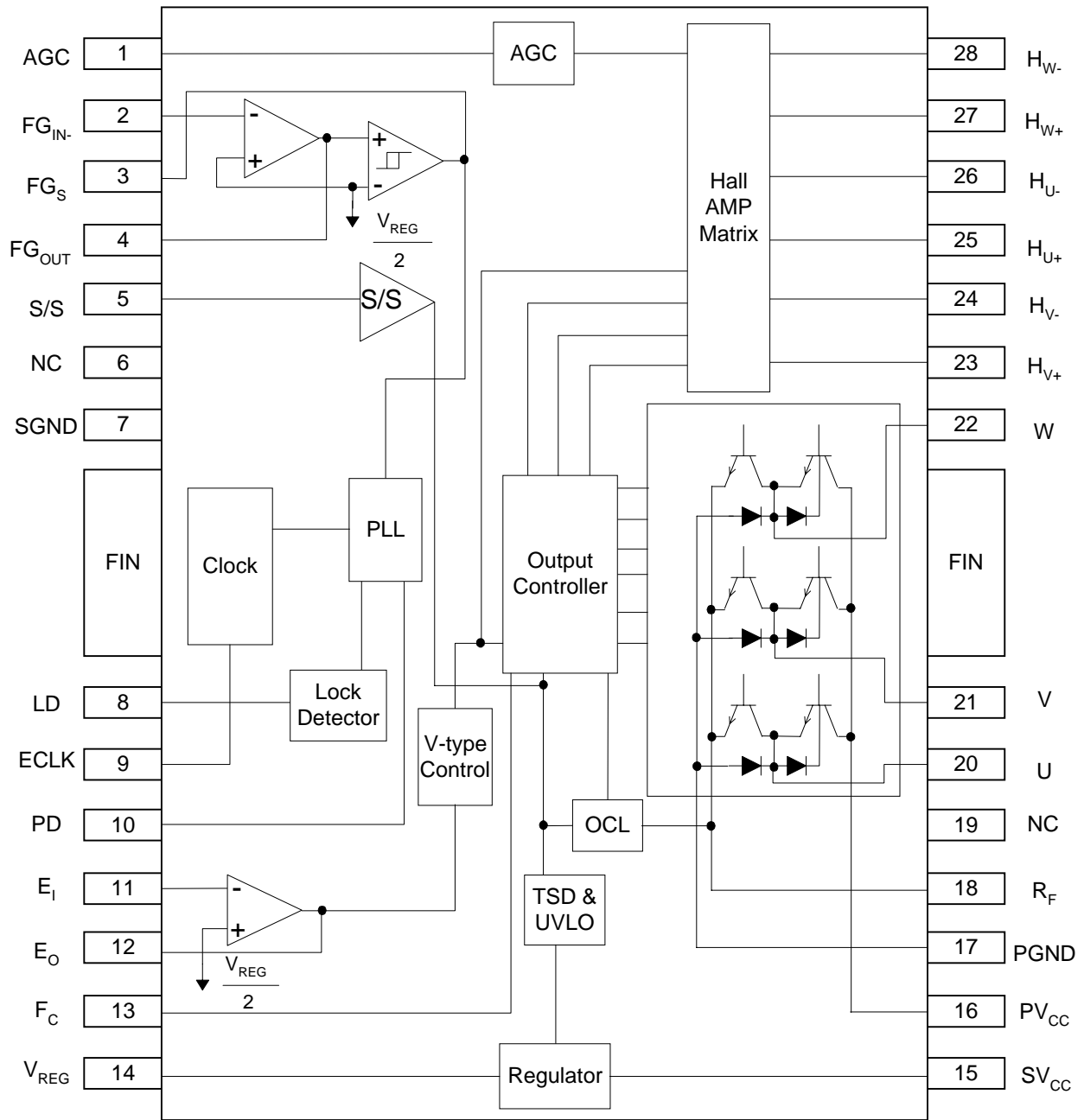
Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	AGC	AGC Amplifier Frequency Characteristics Correction
2	FGIN-	FG Amplifier Inverting Input
3	FGS	FG Pulse Output
4	FGOUT	FG Amplifier Output (Open collect)
5	S/S	Stop And Start
6	NC	-
7	SGND	Signal Ground
8	LD	Phase Locked Loop Detector Output (Open Collect)
9	ECLK	External Clock
10	PD	Phase Locked Loop Detector Output
11	EI	Error Amplifier Inverting Input
12	EO	Error Amplifier Output
13	FC	Control Amplifier Frequency Correction
14	VREG	Regulator Voltage Stabilization Output
15	SVCC	Signal VCC
16	PVCC	Power VCC
17	PGND	Power Ground
18	RF	Output Current Detection
19	NC	-
20	U	U Output
21	V	V Output
22	W	W Output
23	HV+	V Hall Amplifier Non Inverting Input
24	HV-	V Hall Amplifier Inverting Input
25	HU+	U Hall Amplifier Non Inverting Input
26	HU-	U Hall Amplifier Inverting Input
27	HW+	W Hall Amplifier Non Inverting Input
28	HW-	W Hall Amplifier Inverting Input

Internal Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Value	Unit	Remark
Maximum Supply Voltage	VCCMAX	30	V	-
Maximum Output Current	IOMAX	1.0	A	-
Maximum Power Dissipation ^{note1}	PDMAX	3.0 ^{note2}	W	-
		5.25 ^{note3}		
Thermal Resistance ^{note1}	Θ_{JA}	41.57 ^{note2}	°C/W	-
		23.81 ^{note3}		
Operating Temperature	TOPR	-20 ~ +80	°C	-
Storage Temperature	TSTG	-50 ~ +150	°C	-

Note 1.

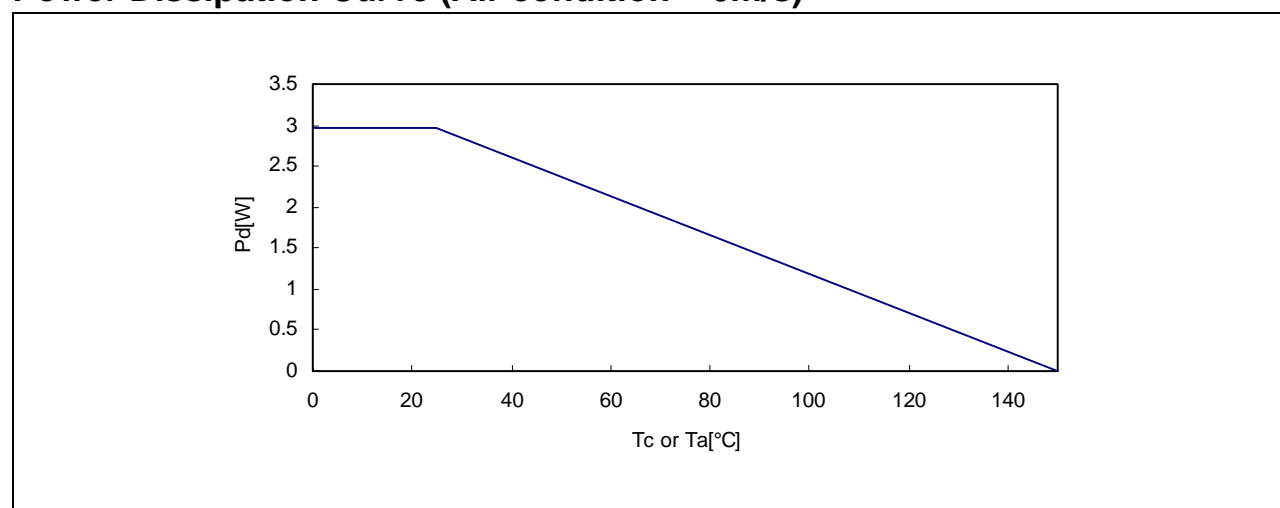
PCB Condition: Thickness (1.6mm), Dimension (76.2mm * 114.3mm)

Refer: EIA/JSED 51-3 & EIA/JSED 51-7

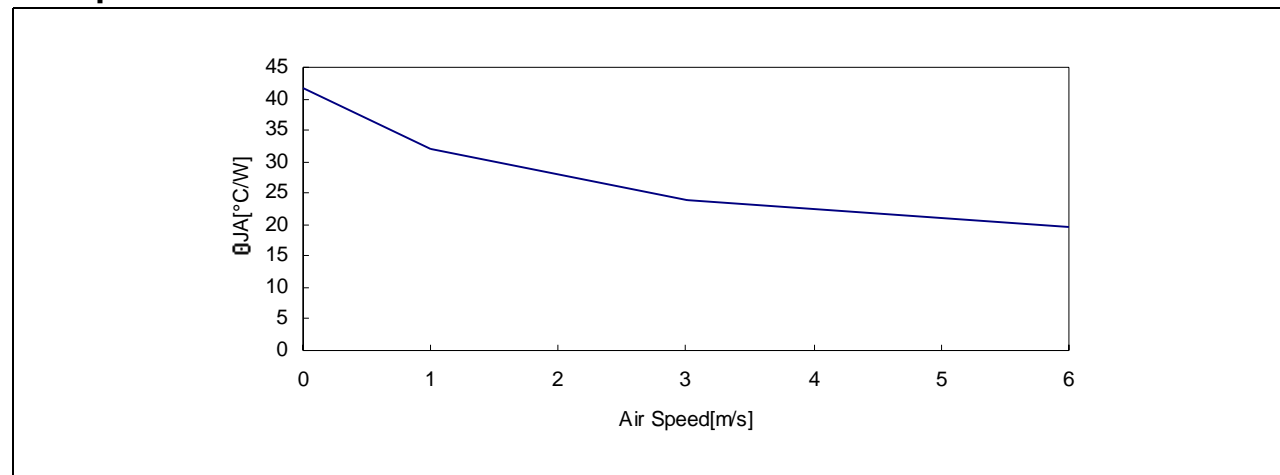
Note 2. Air condition (0m/s)

Note 3. Air condition (3m/s)

Power Dissipation Curve (Air condition = 0m/s)



Air Speed & Θ_{JA}



Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Voltage Range (PVCC,SVCC)	VCC	20	24	28	V

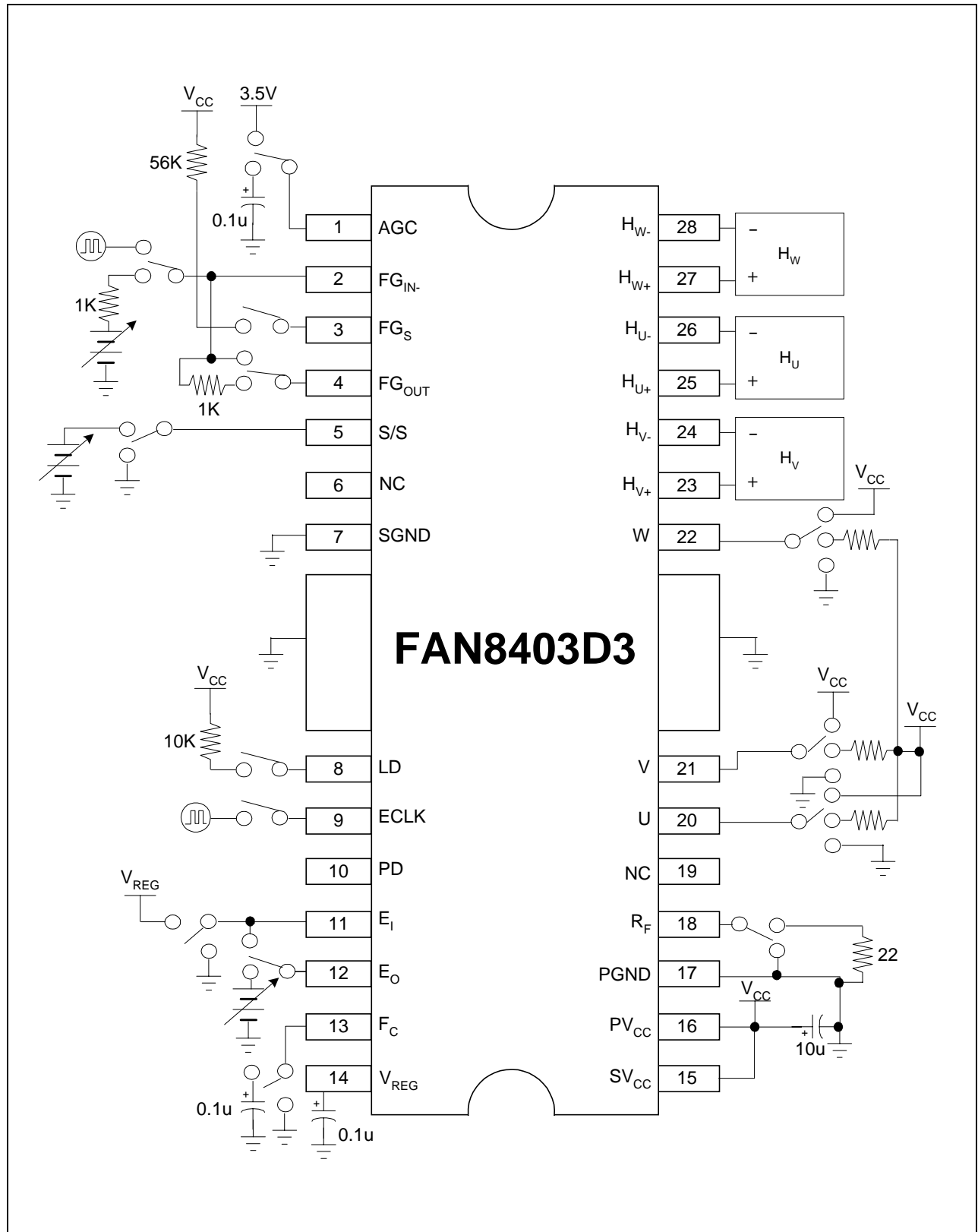
Electrical Characteristics (Ta = 25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLY CURRENT						
Low Power Supply Current	ICCL	Stop mode, VCC=20V	7	17	27	mA
Typical Power Supply Current	ICCT	Stop mode, VCC=24V	7.5	17.5	27.5	mA
High Power Supply Current	ICCH	Stop mode, VCC=28V	8	18	28	mA
OUTPUT POWER TRANSISTOR CHARACTERISTICS						
Source Saturation Voltage (1)	VSATU1	IO=0.6A, RF=0Ω	-	1.8	2.5	V
Source Saturation Voltage (2)	VSATU2	IO=0.3A, RF=0Ω	-	1.6	2.3	V
Sink Saturation Voltage (1)	VSATL1	IO=0.6A, RF=0Ω	-	0.5	1.0	V
Sink Saturation Voltage (2)	VSATL2	IO=0.3A, RF=0Ω	-	0.25	0.7	V
Output Leakage Current	IOLAK	VCC=28V, OUT=28V	-	-	100	μA
UNDER VOLTAGE LOCK-OUT						
UVLO Operating Voltage	VSD	-	8.7	9.3	9.9	V
UVLO Hysteresis	HVSD	-	1.3	1.6	1.9	V
REGULATOR VOLTAGE OUTPUT						
Regulator Output Voltage	VREG	-	5.8	6.3	6.8	V
Power Supply Variation	HVREG1	VCC=20~28V	-	-	100	mV
Load Variation	HVREG2	ILOAD=0~10mA	-	-	100	mV
HALL AMPLIFIER INPUT BLOCK						
H+ Hall Amp Input Bias Current	IBHA+	-	-	2	10	μA
H- Hall Amp Input Bias Current	IBHA-	-	-	2	10	μA
Hall Differential Input Range	VHIN	Sine wave input	50	-	350	mVp-p
Hall Common Input Range	VICM	Differential input: 50mVp-p	3.5	-	VCC-3.5	V
FG AMPLIFIER BLOCK						
FG AMP Input Bias Current	IBFG	-	-1	-	1	μA
FG AMP DC Bias Level	VBFG	-	2.90	3.15	3.40	V
FG Output High Level Voltage	VOHFG	No external load	VREG-1.1V	-	-	V
FG Output Low Level Voltage	VOLFG	No external load	-	0.8	1.2	V
FG SCHMIDT COMPARATOR BLOCK						
FGs High / Low Input Hysteresis	VSHL	-	-50	0	50	mV
FGs Low / High Input Hysteresis	VSLH	-	100	150	200	mV
FGs Hysteresis	VFGL	-	100	-	200	mV
FGs Input Operating Level	VFGSIL	-	400	-	-	mVp-p
FGs Output Saturation Voltage	VFGSSAT	IFGS=4mA	-	0.2	0.4	V
FGs Output Leakage Current	IFGSLEAK	VCC=28V	-	-	10	μA

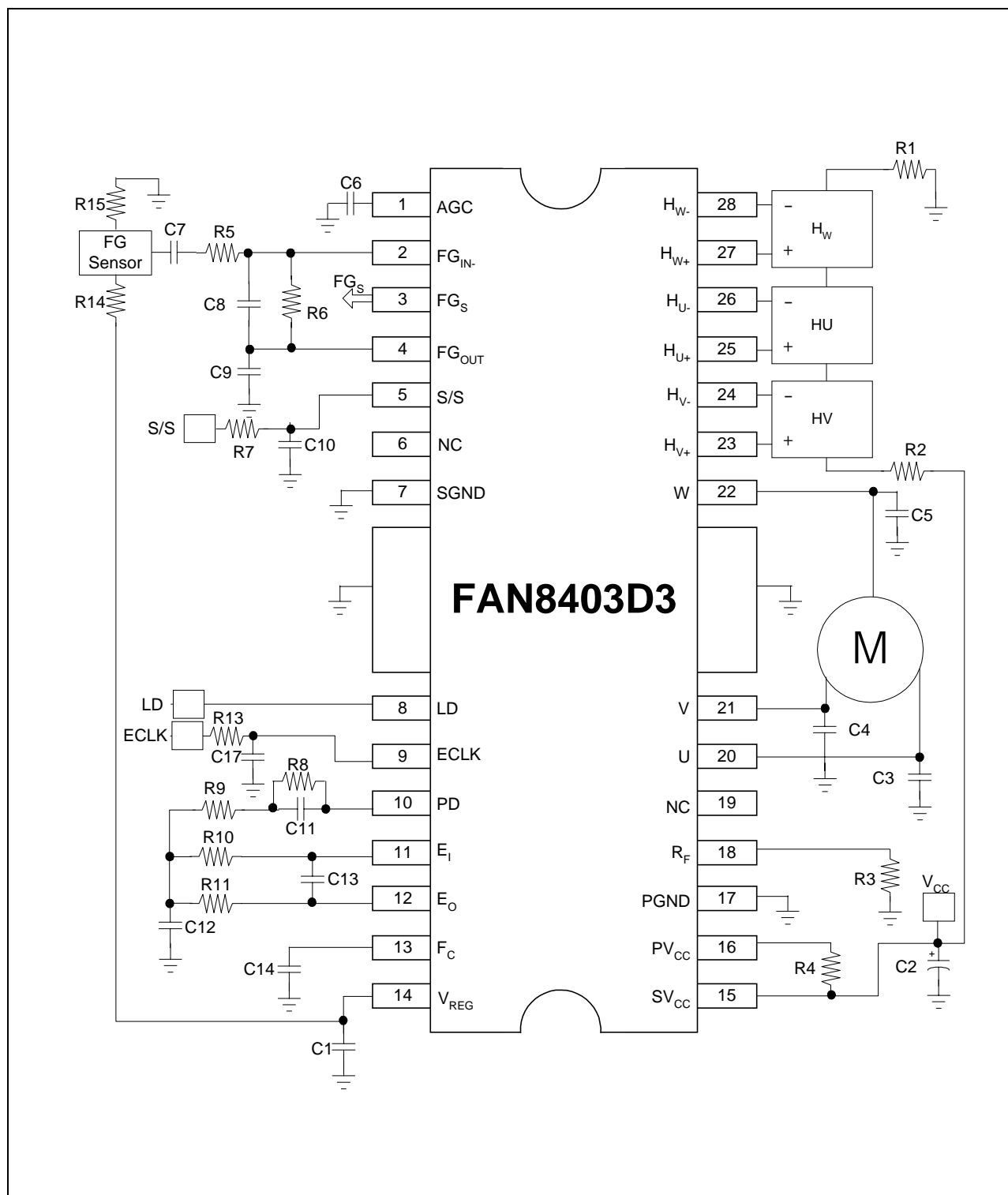
Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
ERROR AMPLIFIER BLOCK						
Error AMP Input Bias Current	IBER	-	-1	-	1	μA
Error AMP DC Bias Level	VBER	-	2.90	3.15	3.40	V
Error Output High Level Voltage	VOHER	No external load	VREG-1.1V	-	-	V
Error Output Low Level Voltage	VOLER	No external load	-	-	1.0	V
CONTROLLER BLOCK						
Dead Zone	VDZ	-	50	100	300	mV
Output Idle Voltage	VID	-	-	-	5	mV
Forward Gain	GDF+	-	0.4	0.5	0.6	-
Reverse Gain	GDF-	-	-0.6	-0.5	-0.4	-
Accelerate Command Voltage	VSTA	-	VREG-1.1V	-	-	V
Decelerate Command Voltage	VSTO	-	-	0.8	1.5	V
Forward Limit Voltage	VL+	RF=22Ω	-	0.60	-	V
Reverse Limit Voltage	VL-	RF=22Ω	-	0.60	-	V
CURRENT LIMIT OPERATION						
RF Output Voltage Limit	VRF	-	0.55	0.60	0.65	V
PHASE COMPARATOR OUTPUT BLOCK						
PD Output High Level Voltage	VPDH	No external load	5.2	-	-	V
PD Output Low Level Voltage	VPDL	No external load	-	-	0.7	V
PD Output Source Current	IPD+	VPD=0.5*VREG	-	-	-0.6	mA
PD Output Sink Current	IPD-	VPD=0.5*VREG	1.0	-	-	mA
PHASE LOCK DETECTOR OUTPUT BLOCK						
LD Output Saturation Voltage	VLDSAT	ILD=5mA	-	0.1	0.4	V
LD Output Leakage Current	ILDLEAK	VCC=28V	-	-	10	μA
S/S BLOCK						
S/S Input High Level Voltage	VIHSS	-	3.0	-	VREG	V
S/S Input Low Level Voltage	VILSS	-	0	-	2	V
S/S Hysteresis	VISSS	-	0.3	0.5	0.7	V
S/S Input Open Voltage	VI OSS	-	3.7	4.2	4.7	V
S/S Input High Level Current	I IHSS	VSS=VREG	100	150	200	μA
S/S Input Low Level Current	I I LSS	VSS=0V	-400	-300	-200	μA
EXTERNAL CLOCK INPUT BLOCK						
ECLK Input High Level Voltage	VIHCLK	-	3.3	-	VREG	V
ECLK Input Low Level Voltage	VILCLK	-	0	-	2.1	V
External Input Frequency	FCLK	External clock mode	0.5	-	7.0	KHz
ECLK Input Open Voltage	VIOCLK	-	3.7	4.2	4.7	V
ECLK Input High Level Current	I IHCLK	VCLK=VREG	100	150	200	μA
ECLK Input Low Level Current	I I LCLK	VCLK=0V	-400	-300	-200	μA

Test Circuits

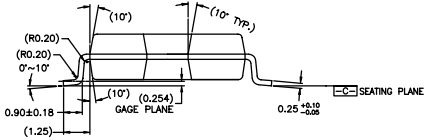
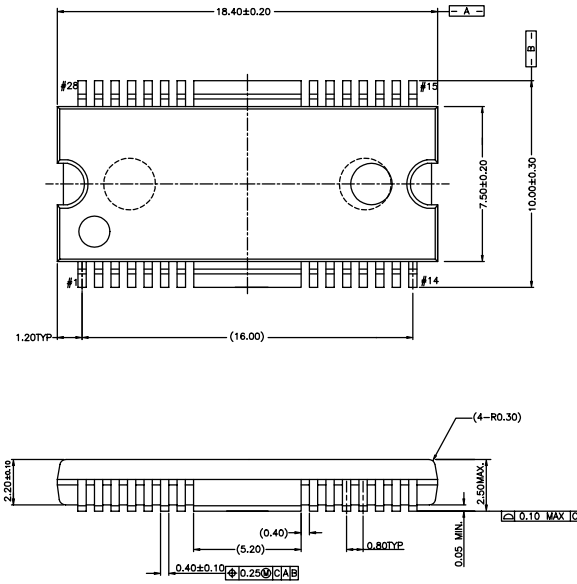


Typical Application Circuits



Package Dimensions (Unit: mm)

28-SSOPH-375SG2



DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.