Data Sheet | May 1999 | FN2815.3

16-Bit Numerically Controlled Oscillator

The Intersil HSP45106/883 is a high performance 16-bit quadrature Numerically Controlled Oscillator (NCO16). The NCO16 simplifies applications requiring frequency and phase agility such as frequency-hopped modems, PSK modems, spread spectrum communications, and precision signal generators. As shown in the Block Diagram, the HSP45106/883 is divided into a Phase/Frequency Control Section (PFCS) and a Sine/Cosine Section.

The inputs to the Phase/Frequency Control Section consist of a microprocessor interface and individual control lines. The frequency resolution is 32 bits, which provides for resolution of better than 0.006Hz at 25.6MHz. User programmable center frequency and offset frequency registers give the user the capability to perform phase coherent switching between two sinusoids of different frequencies. Further, a programmable phase control register allows for phase control of better than 0.006o. In applications requiring up to 8 level PSK, three discrete inputs are provided to simplify implementation.

The output of the PFCS is a 32-bit phase argument which is input to the Sine/Cosine Section for conversion into sinusoidal amplitude. The outputs of the Sine/Cosine Section are two 16-bit quadrature signals. The spurious free dynamic range of this complex vector is greater than 90dBc.

For added flexibility when using the NCO16 in conjunction with DAC's, a choice of either parallel of serial outputs with either two's complement or offset binary encoding is provided. In addition, a synchronization signal is available which signals serial word boundaries.

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- 25.6MHz Clock Rate
- 32-Bit Center and Offset Frequency Control
- 16-Bit Phase Control
- 8 Level PSK Supported Through Three Pin Interface
- Simultaneous 16-Bit Sine and Cosine Outputs
- Output in Two's Complement or Offset Binary
- <0.006Hz Tuning Resolution at 25.6MHz
- Serial or Parallel Outputs
- Spurious Frequency Components < -90dBc
- 16-Bit Microprocessor Compatible Control Interface

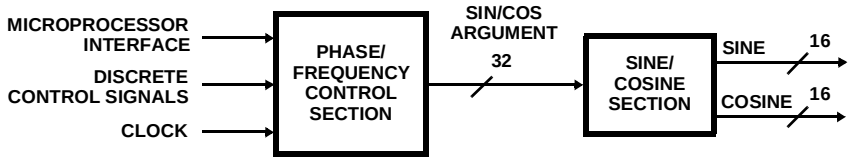
Applications

- Direct Digital Synthesis
- Quadrature Signal Generation
- Modulation - FM, FSK, PSK (BPSK, QPSK, 8PSK)
- Precision Signal Generation

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HSP45106GM-25/883	-55 to 125	85 Ld PGA	G85.A

Block Diagram



Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output Voltage Applied . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC
Voltage Range . . . . . +4.5V to +5.5V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PGA Package	36.0	7.0

Maximum Package Power Dissipation at 125^oC
PGA Package 1.39W
Maximum Junction Temperature . . . . . 175^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Die Characteristics

Gate Count 18,750

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TABLE 1. DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	TEST CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (^oC)	MIN	MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	$55 \le T_A \le +125$	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	$55 \le T_A \le +125$	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400µA V_{CC} = 4.5V (Note 2)	1, 2, 3	$55 \le T_A \le +125$	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +2.0mA V_{CC} = 4.5V (Note 2)	1, 2, 3	$55 \le T_A \le +125$	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	$55 \le T_A \le +125$	-10	+10	µA
Output Leakage Current	I_O	V_{OUT} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	$55 \le T_A \le +125$	-10	+10	µA
Clock Input High	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	$55 \le T_A \le +125$	3.0	-	V
Clock Input Low	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	$55 \le T_A \le +125$	-	0.8	V
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND V_{CC} = 5.5V, (Note 5)	1, 2, 3	$55 \le T_A \le +125$	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 25.6MHz V_{CC} = 5.5V (Notes 3, 5)	1, 2, 3	$55 \le T_A \le +125$	-	205	mA
Functional Test	FT	(Note 4)	7, 8	$55 \le T_A \le +125$	-	-	-

NOTES:

2. Interchanging of force and sense conditions is permitted.
3. Operating supply current is proportional to frequency, typical rating is 8mA/MHz.
4. Tested as follows: f = 1MHz, V_{IH} = 2.6, V_{IL} = 0.4, $V_{OH} \ge 1.5V$, $V_{OL} \le 1.5V$, V_{IHC} = 3.4V, and V_{ILC} = 0.4V.
5. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 2. AC ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	NOTES	GROUP A SUBGROUP	TEMPERATURE (^{O}C)	-25 (25.6MHz)		UNITS
					MIN	MAX	
CLK Period	t_{CP}		9, 10, 11	$-55 \le T_A \le 125$	39	-	ns
CLK High	t_{CH}		9, 10, 11	$-55 \le T_A \le 125$	15	-	ns
CLK Low	t_{CL}		9, 10, 11	$-55 \le T_A \le 125$	15	-	ns
$\overline{WR}$ Period	t_{WP}		9, 10, 11	$-55 \le T_A \le 125$	39	-	ns
$\overline{WR}$ High	t_{WH}		9, 10, 11	$-55 \le T_A \le 125$	15	-	ns
$\overline{WR}$ Low	t_{WL}		9, 10, 11	$-55 \le T_A \le 125$	15	-	ns
Setup Time A(2:0), $\overline{CS}$ to $\overline{WR}$ Going High	t_{AWS}		9, 10, 11	$-55 \le T_A \le 125$	13	-	ns
Hold Time A(2:0), $\overline{CS}$ from $\overline{WR}$ Going High	t_{AWH}		9, 10, 11	$-55 \le T_A \le 125$	2	-	ns
Setup Time C(15:0) to $\overline{WR}$ Going High	t_{CWS}		9, 10, 11	$-55 \le T_A \le 125$	15	-	ns
Hold Time C(15:0) from $\overline{WR}$ Going High	t_{CWH}		9, 10, 11	$-55 \le T_A \le 125$	1	-	ns
Setup Time $\overline{WR}$ High to CLK High	t_{WC}	Note 8	9, 10, 11	$-55 \le T_A \le 125$	16	-	ns
Setup Time MOD(2:0) to CLK Going High	t_{MCS}		9, 10, 11	$-55 \le T_A \le 125$	15	-	ns
Hold Time MOD(2:0) from CLK Going High	t_{MCH}		9, 10, 11	$-55 \le T_A \le 125$	1	-	ns
Setup Time $\overline{ENPOREG}$, $\overline{ENOFREG}$, $\overline{ENCFREG}$, $\overline{ENPHAC}$, $\overline{ENTIREG}$, $\overline{INHOFR}$, PMSEL, $\overline{INITPAC}$, $\overline{BINFMT}$, TEST, PAR/$\overline{SER}$, $\overline{PACI}$, $\overline{INITTAC}$ to CLK Going High	t_{ECS}		9, 10, 11	$-55 \le T_A \le 125$	12	-	ns
Setup Time $\overline{ENPOREG}$, $\overline{ENOFREG}$, $\overline{ENCFREG}$, $\overline{ENPHAC}$, $\overline{ENTIREG}$, $\overline{INHOFR}$, PMSEL, $\overline{INITPAC}$, $\overline{BINFMT}$, TEST, PAR/$\overline{SER}$, $\overline{PACI}$, $\overline{INITTAC}$ from CLK Going High	t_{ECH}		9, 10, 11	$-55 \le T_A \le 125$	1	-	ns
CLK to Output Delay SIN(15:0), COS(15:0), $\overline{TICO}$	t_{DO}		9, 10, 11	$-55 \le T_A \le 125$	-	18	ns
CLK to Output Delay $\overline{DACSTRB}$	t_{DSO}		9, 10, 11	$-55 \le T_A \le 125$	2	18	ns
Output Enable Time	t_{OE}	Note 7	9, 10, 11	$-55 \le T_A \le 125$	-	12	ns

NOTES:

6. AC Testing: V_{CC} = 4.5V and 5.5V. Inputs are driven at 3.0V for Logic “1” and 0.0V for a Logic “0”. Input and output timing measurements are made at 1.5V for both a Logic “1” and 0”. CLK is driven at 4.0V and 0V and measured at 2.0V. Output load per test load circuit with switch closed and C_L = 40pF.
7. Transition is measured at ±200mV from steady state voltage with loading as specified by test load circuit and C_L = 40pF.
8. If $\overline{ENOFRCTL}$, $\overline{ENCFRACTL}$, $\overline{ENTICTL}$, or $\overline{ENPHREG}$ are active, care must be taken to not violate setup and hold times to these registers when writing data into the chip via the C(15:0) port.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE (^oC)	-25 (25MHz)		UNITS
					MIN	MAX	
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1MHz, all measurements are referenced to device GND.	9	T_A = 25	-	10	pF
Output Capacitance	C_{OUT}	V_{CC} = Open, f = 1MHz, all measurements are referenced to device GND.	9	T_A = 25	-	10	pF
Output Disable Delay	t_{OEZ}		9, 10	$-55 \le T_A \le 125$	-	15	ns
Output Rise Time	t_{OR}	From 0.8V to 2.0V	9, 10	$-55 \le T_A \le 125$	-	8	ns
Output Fall Time	t_{OF}	From 20.V to 0.8V	9, 10	$-55 \le T_A \le 125$	-	8	ns

NOTES:

9. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

10. Loading is as specified in the test load circuit with switch closed and C_L = 40pF.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C and D	Samples/5005	1, 7, 9

Burn-In Circuit

HSP45106/833 (PGA)

	11	10	9	8	7	6	5	4	3	2	1	
L	GND	SIN0	SIN1	SIN3	SIN5	SIN4	SIN9	SIN12	SIN13	SIN14	$\overline{\text{DAC STRB}}$	L
K	FMT	V_{CC}	CLK	SIN2	V_{CC}	SIN8	SIN10	GND	SIN15	$\overline{\text{OES}}$	COSO	K
J	$\overline{\text{INIPAC}}$	$\overline{\text{PAR/SEL}}$			SIN6	SIN7	SIN11			$\overline{\text{OEC}}$	COS1	J
H	$\overline{\text{ENP HAC}}$	$\overline{\text{PACI}}$								COS2	COS3	H
G	$\overline{\text{ENTI REG}}$	$\overline{\text{INITT AC}}$	$\overline{\text{INHOF R}}$						COS6	COS4	COS5	G
F	$\overline{\text{ENCF REG}}$	$\overline{\text{ENPO REG}}$	$\overline{\text{ENOF REG}}$						COS7	COS8	V_{CC}	F
E	$\overline{\text{CS}}$	GND	$\overline{\text{WR}}$						COS11	COS10	COS9	E
D	V_{CC}	TEST								GND	COS12	D
C	MOD2	MOD0			C10	C9	C6		INDEX PIN	COS15	COS13	C
B	MOD1	A2	A1	C15	C12	C13	V_{CC}	C4	C1	$\overline{\text{TICO}}$	COS14	B
A	PMSEL	A0	GND	C14	C11	C8	C7	C5	C3	C2	C0	A

PIN "A1"

PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
A1	C0	F7	B11	MOD1	F13	F9	$\overline{\text{ENOFREG}}$	F8	K2	$\overline{\text{OES}}$	F14
A2	C2	F7	C1	COS13	$V_{CC}/2$	F10	$\overline{\text{ENPOREG}}$	F4	K3	SIN15	$V_{CC}/2$
A3	C3	F7	C2	COS15	$V_{CC}/2$	F11	$\overline{\text{ENCFREQ}}$	F7	K4	GND	GND
A4	C5	F8	C5	C6	F8	G1	COS5	$V_{CC}/2$	K5	SIN10	$V_{CC}/2$
A5	C7	F8	C6	C9	F10	G2	COS4	$V_{CC}/2$	K6	SIN8	$V_{CC}/2$
A6	C8	F10	C7	C10	F10	G3	COS6	$V_{CC}/2$	K7	V_{CC}	V_{CC}
A7	C11	F10	C10	MOD0	F12	G9	$\overline{\text{INHOFR}}$	F11	K8	SIN2	$V_{CC}/2$
A8	C14	F11	C11	MOD2	F14	G10	$\overline{\text{INITTAC}}$	F13	K9	CLK	F0
A9	GND	GND	D1	COS12	$V_{CC}/2$	G11	$\overline{\text{ENTIREG}}$	F12	K10	V_{CC}	V_{CC}
A10	A0	F8	D2	GND	GND	H1	COS3	$V_{CC}/2$	K11	$\overline{\text{BINFMT}}$	F6
A11	PMSEL	F14	D10	TEST	F14	H2	COS2	$V_{CC}/2$	L1	$\overline{\text{DACSTRB}}$	$V_{CC}/2$
B1	COS14	$V_{CC}/2$	D11	V_{CC}	V_{CC}	H10	$\overline{\text{PACI}}$	F11	L2	SIN14	$V_{CC}/2$
B2	$\overline{\text{TICO}}$	$V_{CC}/2$	E1	COS9	$V_{CC}/2$	H11	$\overline{\text{ENPHAC}}$	F10	L3	SIN13	$V_{CC}/2$
B3	C1	F7	E2	COS10	$V_{CC}/2$	J1	COS1	$V_{CC}/2$	L4	SIN12	$V_{CC}/2$
B4	C4	F8	E3	COS11	$V_{CC}/2$	J2	$\overline{\text{OEC}}$	F14	L5	SIN9	$V_{CC}/2$
B5	V_{CC}	V_{CC}	E9	$\overline{\text{WR}}$	F4	J5	SIN11	$V_{CC}/2$	L6	SIN4	$V_{CC}/2$
B6	C13	F11	E10	GND	GND	J6	SIN7	$V_{CC}/2$	L7	SIN5	$V_{CC}/2$
B7	C12	F11	E11	$\overline{\text{CS}}$	F6	J7	SIN6	$V_{CC}/2$	L8	SIN3	$V_{CC}/2$
B8	C15	F11	F1	V_{CC}	V_{CC}	J10	$\overline{\text{PAR/SER}}$	F13	L9	SIN1	$V_{CC}/2$
B9	A1	F7	F2	COS8	$V_{CC}/2$	J11	$\overline{\text{INITPAC}}$	F12	L10	SIN0	$V_{CC}/2$
B10	A2	F10	F3	COS7	$V_{CC}/2$	K1	COS0	$V_{CC}/2$	L11	GND	GND

NOTES:

11. $V_{CC}/2$ (2.7V ±10%) used for outputs only.
12. 47kΩ (±20%) resistor connected to all pins except V_{CC} and GND.
13. V_{CC} = 5.5V ±0.5V.
14. 0.1µF (min) capacitor between V_{CC} and GND per position.
15. F0 = 100kHz ±10%, F1 = F0/2, F2 = F1/2...., F11 = F10/2, 40% - 60% Duty Cycle.
16. Input voltage limits: V_{IL} = 0.8V max., V_{IH} = 4.5V ±10%.

Die Characteristics

DIE DIMENSIONS:

251 mils x 240 mils x 19 ±1mils

METALLIZATION:

Type: Si-Al, or Si-Al-Cu
Thickness: 8kÅ

GLASSIVATION:

Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY:

0.8×10^5 A/cm^2

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