Integrated Circuit Systems, Inc.

ICS9279-03

Preliminary Product Preview

Low Skew Fan Out Buffers

General Description

The **ICS9279-03** generates low skew clock buffers required for high speed RISC or CISC microprocessor systems such as Intel PentiumPro. Outputs will handle up to 133 MHz clocks. An output enable is provided for testability.

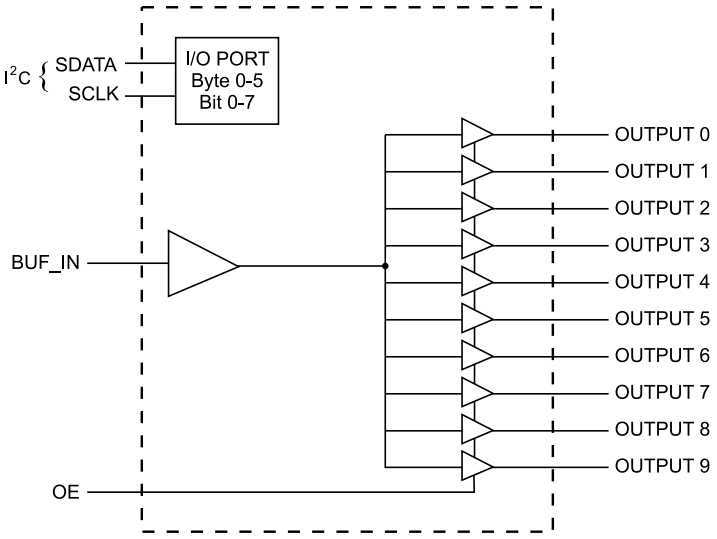
The device is a buffer with low output to output skew. This is a Fanout buffer device, not using an internal PLL. This buffer can also be a feedback to an external PLL stage for phase synchronization to a master clock. There are a total of ten outputs, sufficient for feedback to a PLL source and to drive four small outline DIMM modules (S.O. DIMM) at 2 clocks each. Or a total of ten outputs as a Fanout buffer from a common clock source.

The individual clock outputs are addressable through I^2C to be enabled, or stopped in a low state for reduced EMI when the lines are not needed.

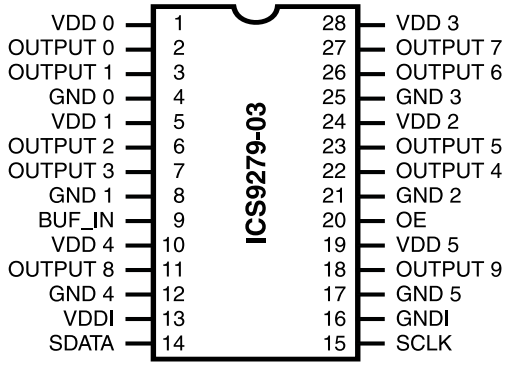
Features

- Ten High speed, low noise non-inverting buffers for (to 133 MHz), clock buffer applications.
- Output slew rate faster than 1.5V/ns into 20pF
- Supports up to four small outline DIMMS (S.O. DIMM).
- Synchronous clocks skew matched to 250 ps window on OUTPUTs (0:9).
- I^2C Serial Configuration interface to allow individual OUTPUTs to be stopped low.
- Multiple VDD, VSS pins for noise reduction
- Tri-state pin for testing
- 3.0V – 3.7V supply range
- 28-pin (209 mil) SSOP package

Block Diagram



Pin Configuration



28-Pin SSOP

PentiumPro is a trademark of Intel Corporation
I^2C is a trademark of Philips Corporation

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2, 3	OUTPUT (0:1)	OUT	Clock outputs[1], uses VDD0, GND0
6, 7	OUTPUT (2:3)	OUT	Clock outputs[1], uses VDD1, GND1
22, 23	OUTPUT (4:5)	OUT	Clock outputs[1] uses VDD2, GND2
26, 27	OUTPUT (6:7)	OUT	Clock output[1] uses VDD3, GND3
11	OUTPUT8	OUT	Clock output[1] uses VDD4, GND4
18	OUTPUT9	OUT	Clock output[1] uses VDD5, GND5
9	BUF_IN	IN	Input for buffers
20	OE	IN	Tri-states all outputs when held LOW. Has internal pull-up.[2]
14	SDATA	I/O	Data pin for I^2C circuitry[3]
15	SCLK	I/O	Clock pin for I^2C circuitry[3]
1, 5, 10, 19, 24, 28	VDD (0:5)	PWR	3.3V Power supply for OUTPUT buffers
4, 8, 12, 16, 17, 21, 25	GND (0:5)	PWR	Ground for OUTPUT buffers
13	VDDI	PWR	3.3V Power supply for I^2C circuitry and internal logic
16	GNDI	PWR	Ground for I^2C circuitry and internal logic

Notes:

1. At power up all ten OUTPUTs are enabled and active.
2. OE has a 100K Ohm internal pull-up resistor to keep all outputs active.
3. The SDATA and SCLK inputs both also have internal pull-up resistors with values above 100K Ohms as well for complete platform flexibility.

Power Groups

VDD (0:5), GND (0:5) = Power supply for OUTPUT buffer

VDDI, GNDI = Power supply for I^2C circuitry

Technical Pin Function Descriptions

VDD
This is the power supply to the internal core logic of the device as well as the clock output buffers for OUTPUT (0:9).

This pin operates at 3.3V volts. Clocks from the listed buffers that it supplies will have a voltage swing from Ground to this level. For the actual guaranteed high and low voltage levels for the Clocks, please consult the DC parameter table in this data sheet.

GND
This is the power supply ground (common or negative) return pin for the internal core logic and all the output buffers.

OUTPUT (0:9)
These Output Clocks are use to drive Dynamic RAM's and are low skew copies of the CPU Clocks. The voltage swing of the OUTPUTs output is controlled by the supply voltage that is applied to VDD of the device, operates at 3.3 volts.

I^2C
The SDATA and SCLOCK Inputs are use to program the device. The clock generator is a slave-receiver device in the I^2C protocol. It will allow read-back of the registers. See configuration map for register functions. The I^2C specification in Philips I^2C Peripherals Data Handbook (1996) should be followed.

BUF_IN
Input for Fanout buffers (OUTPUT 0:9).

OE
OE tristates all outputs when held low.

VDD1
This is the power supply to I^2C circuitry.

General I²C serial interface information

A. For the clock generator to be addressed by an I²C controller, the following address must be sent as a start sequence, with an acknowledge bit between each byte.

Clock Generator Address (7 bits)	ACK	+ 8 bits dummy command code	ACK	+ 8 bits dummy Byte count	ACK
A(6:0) & R/W#					
D2(H)					

Then Byte 0, 1, 2, etc in sequence until STOP.

B. The clock generator is a slave/receiver I²C component. It can "read back "(in Philips I²C protocol) the data stored in the latches for verification. (set R/W# to 1 above). There is no BYTE count supported, so it does not meet the Intel SMB PIIX4 protocol.

Clock Generator Address (7 bits)	ACK	Byte 0	ACK	Byte 1	ACK
A(6:0) & R/W#					
D3(H)					

Byte 0, 1, 2, etc in sequence until STOP.

C. The data transfer rate supported by this clock generator is 100K bits/sec (standard mode)

D. The input is operating at 3.3V logic levels.

E. The data byte format is 8 bit bytes.

F. To simplify the clock generator I²C interface, the protocol is set to use only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.

G In the power down mode (PWR_DWN# Low), the SDATA and SCLK pins are tristated and the internal data latches maintain all prior programming information.

H. At power-on, all registers are set to a default condition. See Byte 0 detail for default condition, Bytes 1 through 5 default to a 1 (Enabled output state).

Serial Configuration Command Bitmaps

Byte 0: OUTPUT Clock Register (Default=0)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	1	Reserved
Bit6	-	1	Reserved
Bit5	-	1	Reserved
Bit4	-	1	Reserved
Bit3	7	1	OUTPUT3
Bit2	6	1	OUTPUT2
Bit1	3	1	OUTPUT1
Bit0	2	1	OUTPUT0

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Note: PWD = Power-Up Default

Functionality

OE#	OUTPUT (0:9)
0	Hi-Z
1	1 X BUF_IN

Byte 1: OUTPUT Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	27	1	OUTPUT7 (Act/Inact)
Bit 6	26	1	OUTPUT6 (Act/Inact)
Bit 5	23	1	OUTPUT5 (Act/Inact)
Bit 4	22	1	OUTPUT4 (Act/Inact)
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 2: OUTPUT Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	18	1	OUTPUT9 (Act/Inact)
Bit 6	11	1	OUTPUT8 (Act/Inact)
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Note: PWD = Power-Up Default

ICS9279-03 Power Management

The values below are estimates of target specifications.

Condition	Max 3.3V supply consumption Max discrete cap loads VDD = 3.465V All static inputs = VDD or GND
No Clock Mode (BUF_IN - VDD1 or GND) I^2C Circuitry Active	3mA
Active 66MHz (BUF_IN = 66.66MHz)	230mA
Active 100MHz (BUF_IN = 100.00MHz)	360mA

Absolute Maximum Ratings

Supply Voltage . . . . . 7.0 V

Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 –70° C unless otherwise stated

Electrical Characteristics - Input & Supply

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}			5	uA
Input Low Current	I_{IL}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA
	I_{IL}	V_{IN} = 0 V; Inputs with 100K pull-up resistors	-60	-33		uA
Operating Supply Current	I_{DD1}	C_L = 0 pF; F_{IN} @ 66M		80	120	mA
	I_{DD2}	C_L = 0 pF; F_{IN} @ 100M		120	180	mA
	I_{DD3}	C_L = 30 pF; RS=33Ω; F_{IN} @ 66M		180	260	mA
	I_{DD4}	C_L = 30 pF; RS=33Ω; F_{IN} @ 100M		240	360	mA
Input frequency	F_i[1]	V_{DD} = 3.3 V; All Outputs Loaded	10		133	MHz
Input Capacitance	C_{IN}[1]	Logic Inputs			5	pF

[1]Guarenteed by design, not 100% tested in production.

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 –70° C unless otherwise stated

Electrical Characteristics - Outputs

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 - 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP}	V_O = V_{DD}*(0.5)	10		24	Ω
Output Impedance	R_{DSN}	V_O = V_{DD}*(0.5)	10		24	Ω
Output High Voltage	V_{OH}	I_{OH} = -30 mA	2.6	3		V
Output Low Voltage	V_{OL}	I_{OL} = 23 mA		0.27	0.4	V
Output High Current	I_{OH}	V_{OH} = 2.0 V		-115	-54	mA
Output Low Current	I_{OL}	V_{OL} = 0.8 V	40	57		mA
Rise Time[1]	T_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V		0.95	1.33	ns
Fall Time[1]	T_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V		0.95	1.33	ns
Duty Cycle[1]	D_t	V_T = 1.5 V	45	51	55	%
Skew[1]	T_{sk}	V_T = 1.5 V		110	250	ps
Propagation[1]	T_{PROP1}	V_T = 1.5 V	1	5.2	5.5	ns
	T_{PROP2}	V_T = 50% BIN to 10% OUT	1	4.3	5	ns
	T_{PROPEN}	V_T = 1.5 V	1		8	ns
	$T_{PROPDIS}$	V_T = 1.5 V	1		8	ns

[1]Guarenteed by design, not 100% tested in production.

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

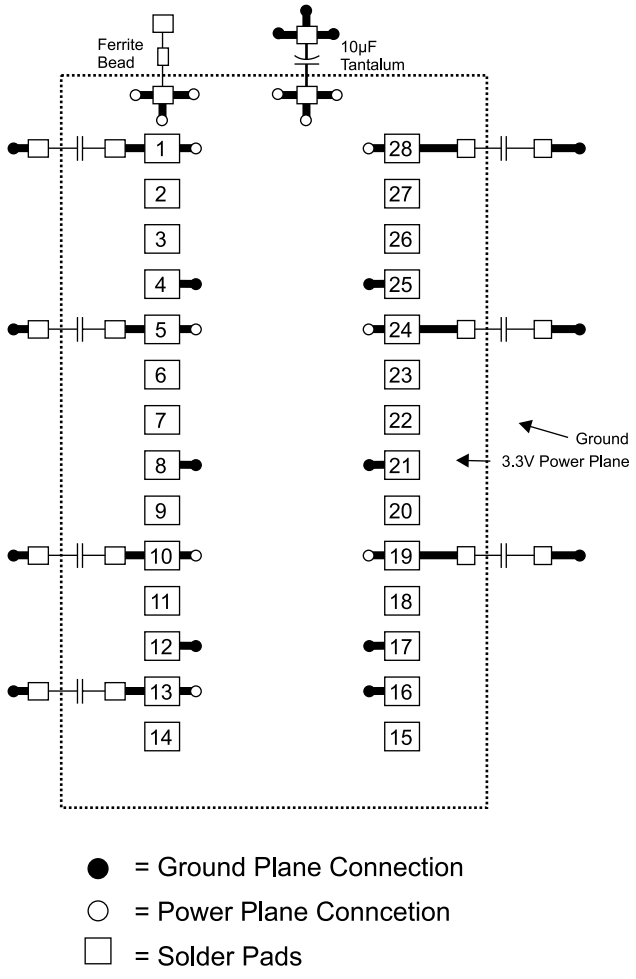
General Layout Precautions:

1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
2) Make all power traces and vias as wide as possible to lower inductance.

Notes:

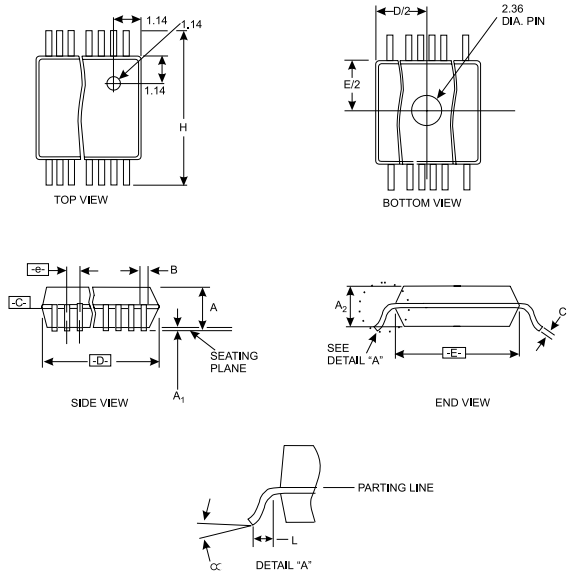
1 All clock outputs should have series terminating resistor. Not shown in all places to improve readibility of diagram

2 Optional EMI capacitor should be used on all CPU, SDRAM, and PCI outputs.



Capacitor Values:

All unmarked capacitors are 0.01µF ceramic



SYMBOL	COMMON DIMENSIONS			VARIATIONS	D		
	MIN.	NOM.	MAX.	N	MIN.	NOM.	MAX.
A	0.068	0.073	0.078	28	0.397	0.402	0.407
A1	0.002	0.005	0.008				
A2	0.066	0.068	0.070				
b	0.010	0.012	0.015				
c	0.004	0.006	0.008				
D	See Variations						
E	0.205	0.209	0.212				
e		0.0256 BSC					
H	0.301	0.307	0.311				
L	0.025	0.030	0.037				
N	See Variations						
∝	0°	4°	8°				

Dimensions in inches

209 mil 28 Pin SSOP Package

Ordering Information

ICS9279F-03

Example:

ICS XXXX F - PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
F=SSOP

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device