New Product

Power Selector Switch

FEATURES

- MOSFETs Configured To Give Spdt Switch With One Control Input
- 2.5- to 8-V Ground Referenced Control Input
- 30-mΩ Main Switch On-Resistance
- 70-mΩ Alternate Switch On-Resistance
- SOIC-8 Package
- 3000-V ESD Protection On Control Input
- Zero Power Consumption In Alternate Power Mode

APPLICATIONS

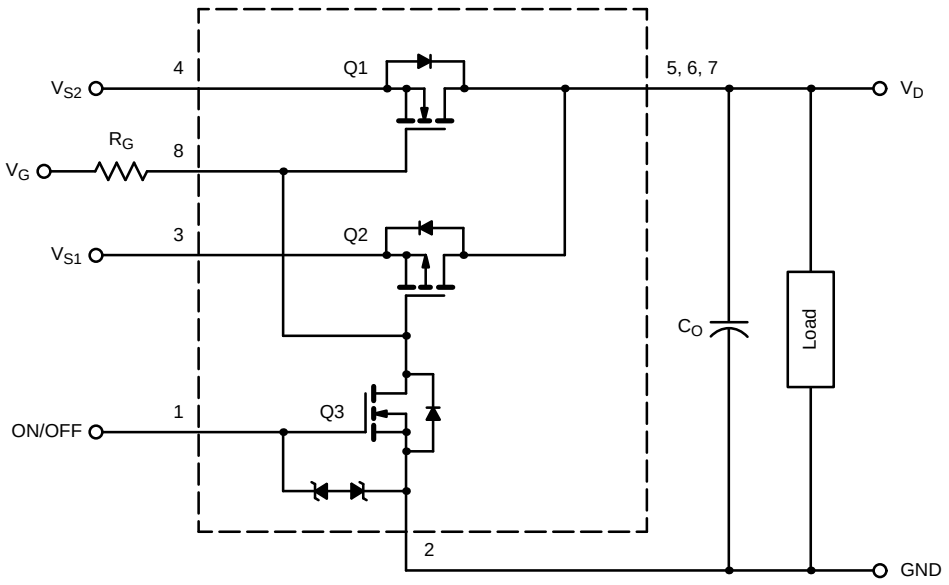
- ACPI Power Switching In Desktop Computers

ESD Protected
3000 V

DESCRIPTION

The Si4700DY consists of two MOSFETs configured for use as a single-pole, double-throw (SPDT) switch. A single ground referenced input, controls which switch is on. The Si4700DY is intended for use in applications where two power sources are available and the circuit must select one of the two depending on the conditions. An example of such a circuit is ACPI implementation in computers where part of a circuit must switch to an “always-on” power supply when the computer is in suspend mode, but runs off the main power supply for normal operation.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter		Symbol	10 sec	Steady State	Unit
Drain-Source Voltage	Q1	V_{DS}	12		V
	Q2		–12		
Logic Control Input		V_{IN}	8		
Continuous Drain Current[a]	Q1	I_D	7.6	5.3	A
	Q2		5.0	3.5	
Pulsed Drain Current[b]	Q1	I_{DM}	20		
	Q2		20		
Continuous Intrinsic Diode Conduction[a]	Q1	I_S	2.1	1.15	
	Q2		2.1	1.15	
Maximum Power Dissipation[a]		P_D	2.35	1.25	W
Operating Junction and Storage Temperature Range		T_j, T_{stg}	–55 to 150		°C
ESD Voltage[c]		ESD	3		KV

Notes
a. Surface mounted on 1” x1” FR4 board.
b. Pulse test: pulse width ≤ 300 μS, duty cycle ≤ 2%.
c. Equivalent to MIL-STD-883D Human Body Model (100 pF, 1500 Ω)

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	43	53	°C/W
	Steady State		82	100	
Maximum Junction-to-Foot (Drain)[b]	Steady State	R_{thJF}	25	30	

Notes
a. Surface Mounted on 1” x 1” FR4 Board.
b. Junction-to-foot thermal impedance represents the effective thermal impedance of all heat carrying leads in parallel and is intended for use in conjunction with the thermal impedance of the PC board pads to ambient ($R_{thJA} = R_{thJF} + R_{thPCB-A}$). It can also be used to estimate chip temperature if power dissipation and the lead temperature of a heat carrying (drain) lead is known.

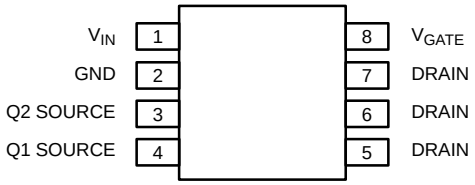
SPECIFICATIONS

Parameter	Symbol	Specific Test Conditions		Limits Min	Limits Typ[a]	Limits Max	Unit
Off State Leakage Current	I_{DSS}	V_{DS} = –12 V, V_{GS} = 0 V	Q1			1	μA
			Q2			–1	
		V_{DS} = –8 V, V_{GS} = 0 V	Q3			1	
		V_{DS} = –12 V, V_{GS} = 0 V, T_J = 55°C	Q2			–5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±4.5 V	Q3			±1	
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	Q3	0.6			V
On-Resistance	$r_{DS(on)}$	V_S = 4.5 V, I_D = 1 A, $V_{ON/OFF}$ = 2.5 V	Q1		25	30	mΩ
		V_S = 2.5 V, I_D = 1 A, $V_{ON/OFF}$ = 2.5 V	Q1		32	40	
		V_S = 4.5 V, I_D = 1 A, $V_{ON/OFF}$ = 2.5 V	Q2		58	70	
		V_S = 2.5 V, I_D = 1 A, $V_{ON/OFF}$ = 2.5 V	Q2		90	110	

Notes
a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

PIN CONFIGURATION

SO-8



Top View

Order Number: **Si4700DY**

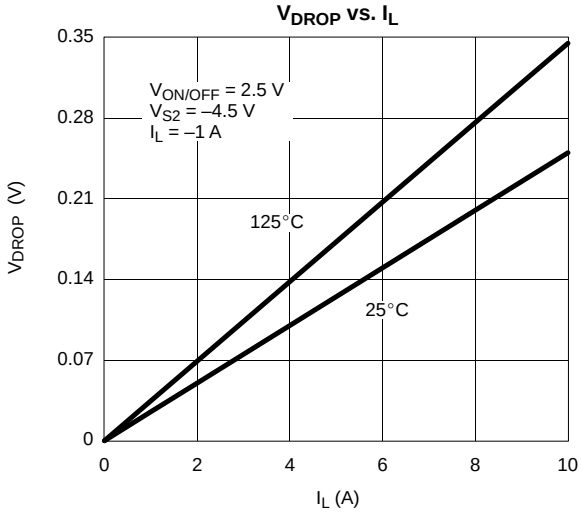
TRUTH TABLE

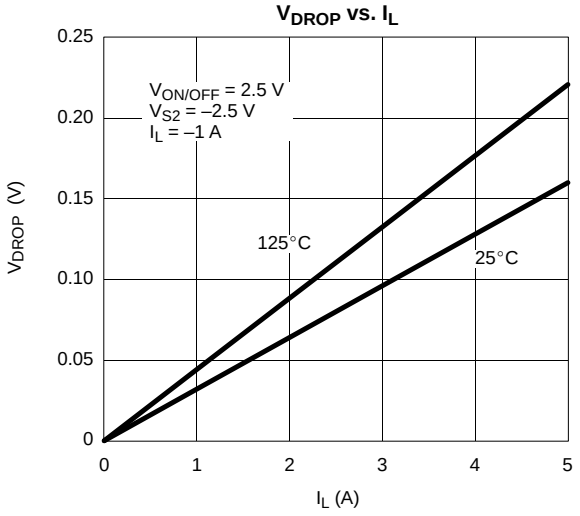
V_{IN}	Q1	Q2
L	ON	OFF
H	OFF	ON

PIN DESCRIPTION

Pin Number	Symbol	Description
1	$V_{ON/OFF}$	Logic Input Signal
2	GND	Ground (reference for logic input and power ground)
3	Q2 SOURCE	Input for alternate power
4	Q1 SOURCE	Input for main power
5, 6, 7	DRAIN	Output
8	V_{GATE}	Gate drive voltage via pull-up resistor

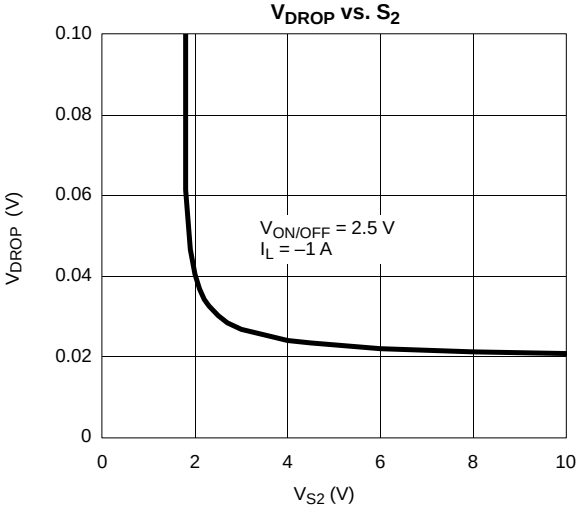
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL



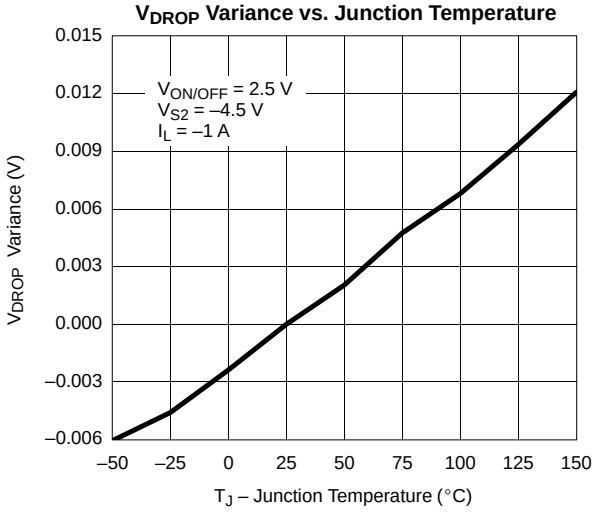


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL

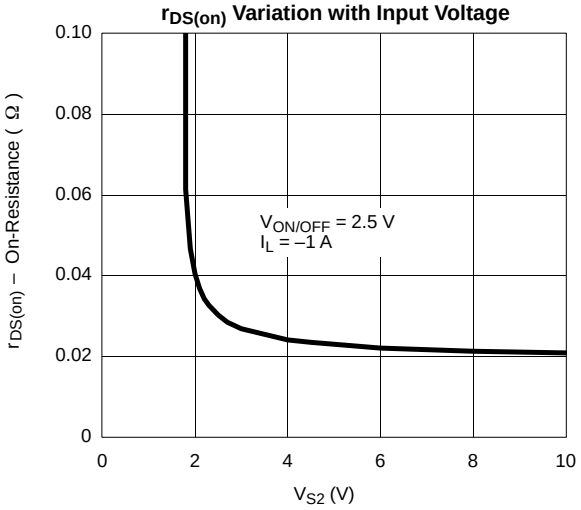
V_{DROP} vs. S_2



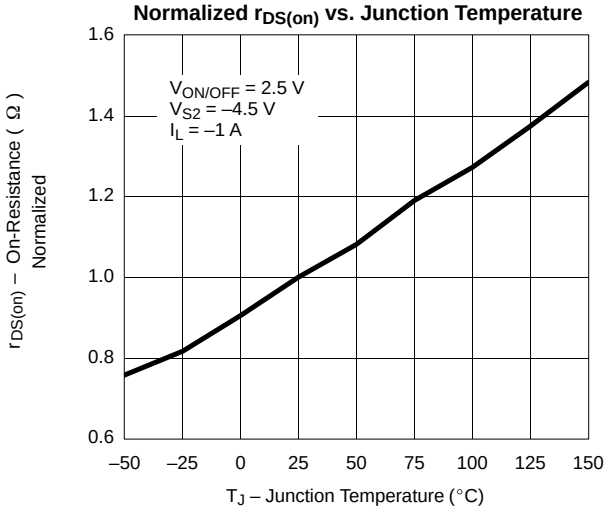
V_{DROP} Variance vs. Junction Temperature



$r_{DS(on)}$ Variation with Input Voltage

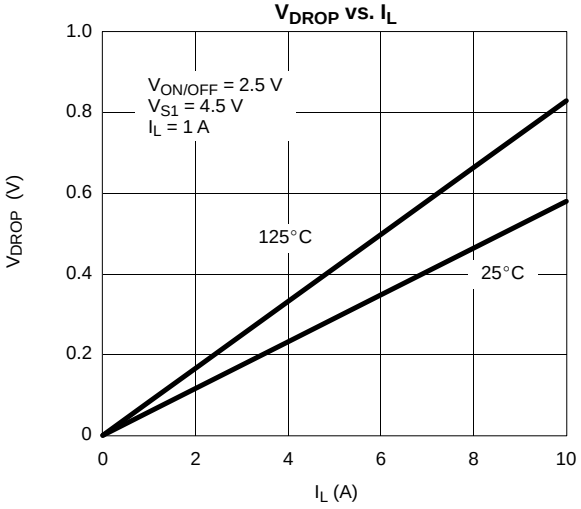


Normalized $r_{DS(on)}$ vs. Junction Temperature

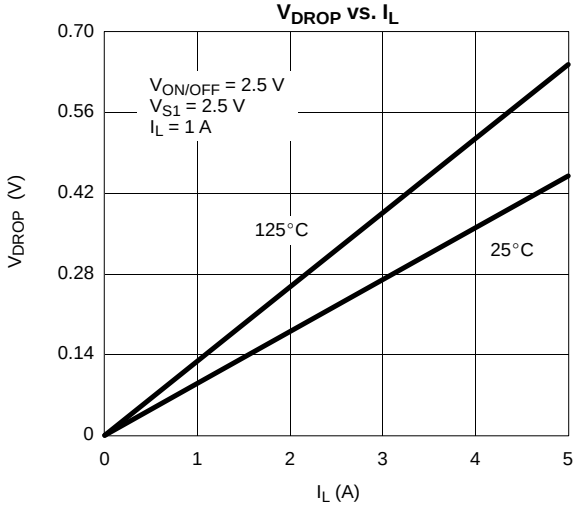


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL

V_{DROP} vs. I_L

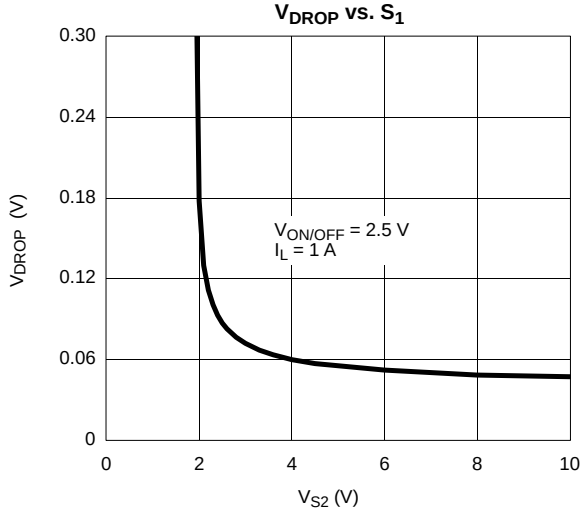


V_{DROP} vs. I_L

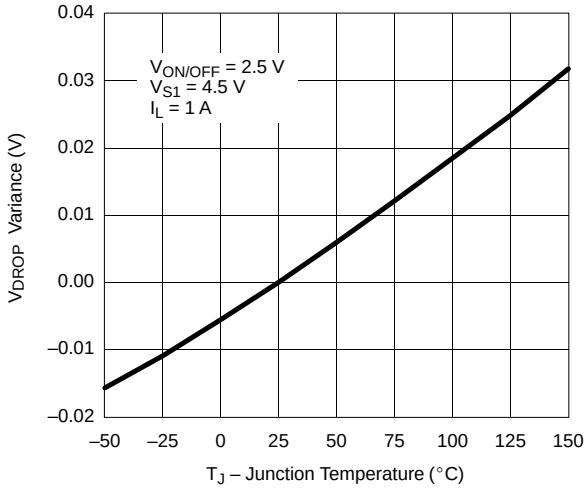


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) — P-CHANNEL

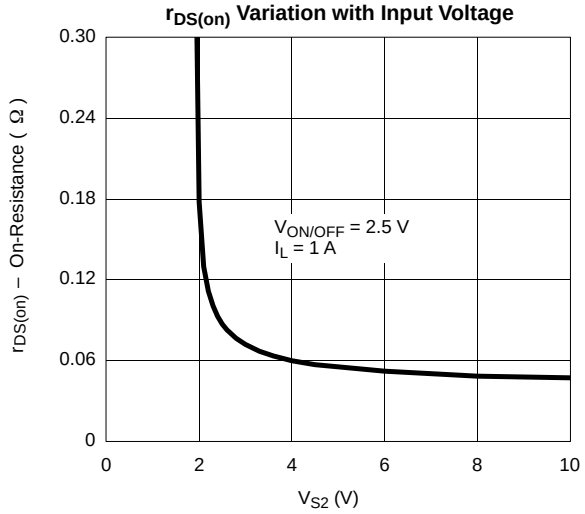
V_{DROP} vs. S_1



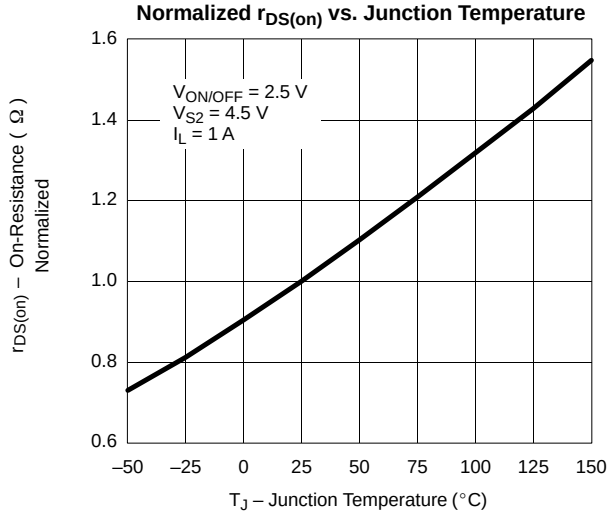
V_{DROP} Variance vs. Junction Temperature



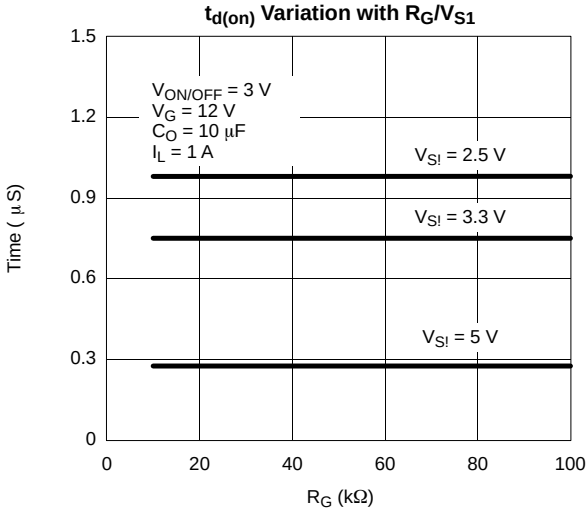
$r_{DS(on)}$ Variation with Input Voltage



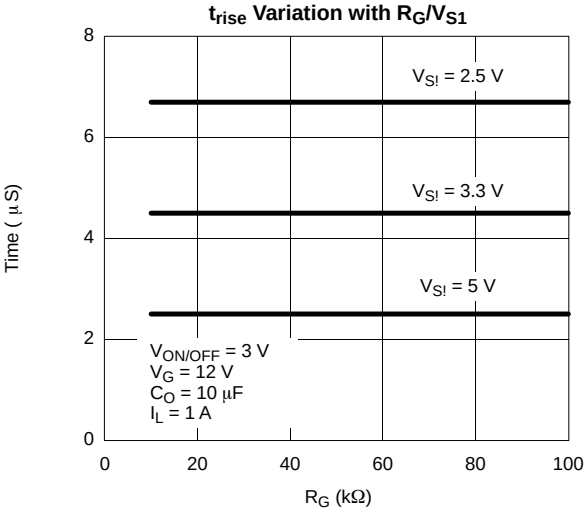
Normalized $r_{DS(on)}$ vs. Junction Temperature



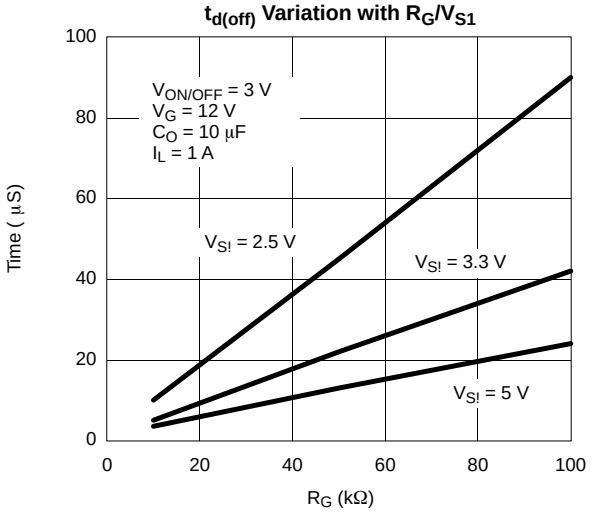
$t_{d(on)}$ Variation with R_G/V_{S1}

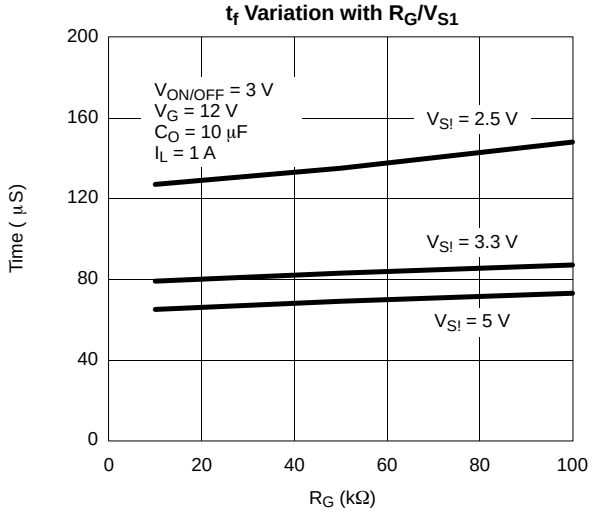


t_{rise} Variation with R_G/V_{S1}

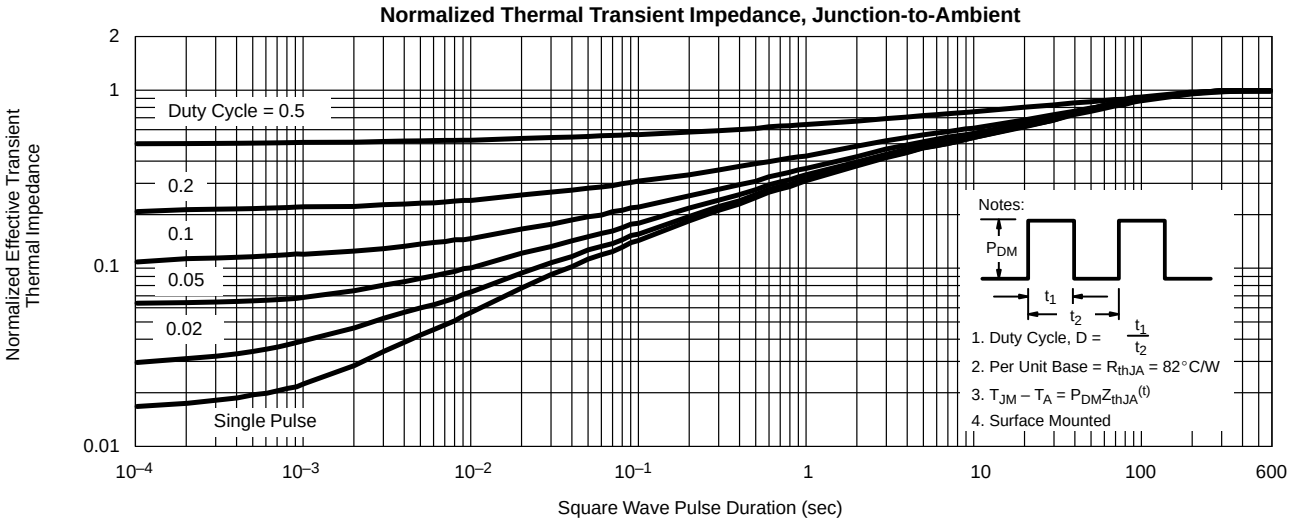


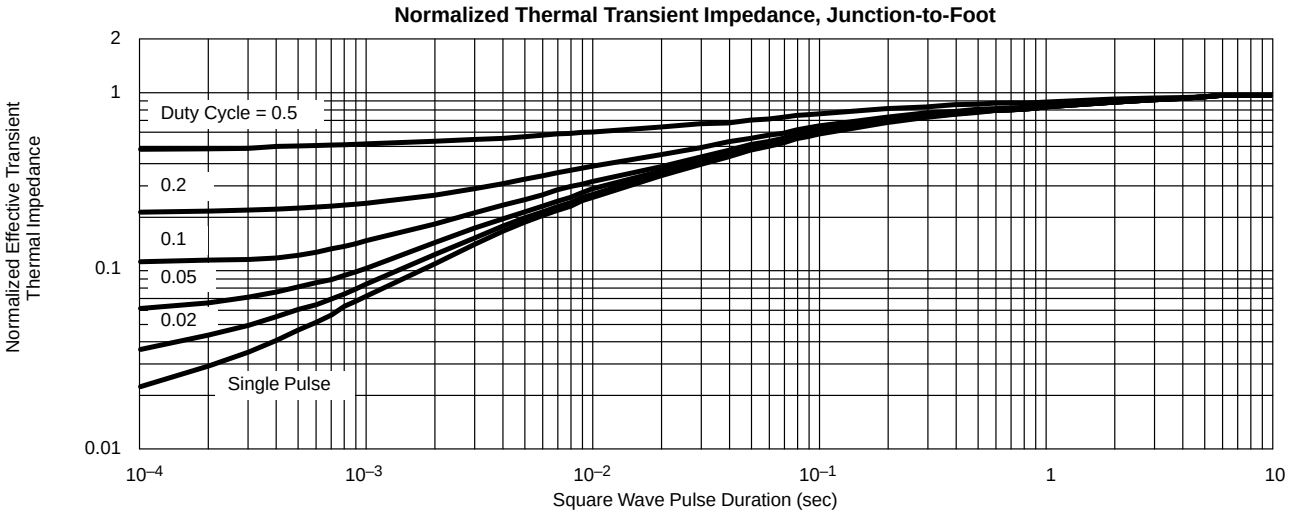
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL





TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) ALL CHANNELS





TYPICAL APPLICATIONS

The Si4700 is designed to be used to select one of two power sources for a circuit, such as needed to implement ACPI in desktop computers. In this application, parts of the circuit must run off an always-on power supply when the computer is in suspend mode. When in normal mode, these circuits run off the main power supply.

The Si4700DY contains an n-channel MOSFET and a p-channel MOSFET switch connected together to make a single-pole, double-throw switch. An additional on-board small signal MOSFET provides a ground referenced logic input. When the control input is high, the power MOSFET gates are pulled to ground, and the p-channel MOSFET is on. When the input is low, the gates are pulled above the supply rail, and the n-channel MOSFET is on (pulling the gate of the p-channel above the source potential has no effect).

The gate drive for the n-channel device, Q1, uses an external 12-V supply via an external resistor. A typical value for this resistor is around 20 kΩ, but the value is not critical as long as the current in Q3 is kept below 0.05 A. A higher value of resistance reduces the current while in suspend mode, but also introduces a longer delay when turning on Q1.

The Si4700DY switch is a break-before-make configuration, therefore sufficient capacitance must be present on the isolated load to ensure hold up during switching. Due to fast switching times this should not be significant and is preferred over a make-before-break that would connect the two power supplies directly for a short period.

Note that the n-channel MOSFET is oriented to ensure that the internal diode does not conduct while the sub-circuit is isolated. In this direction it also provides a fail-safe path for the circuit's power through the diode. The forward drop of the p-channel MOSFET's diode will block any current back-feeding the secondary supply, assuming the two supplies are very close in voltage.

The Si4700DY has a maximum $r_{DS(on)}$ of 30 mΩ for the n-channel MOSFET used during normal operation and 70 mΩ for the p-channel used when the computer is in suspend, making it ideal for loads up to 3 A or higher depending on voltage drop requirements. It can be used on any rail voltage between 2.5 V and 8 V (based on an absolute max of 12 V), with a logic input between 2.5-V and 5-V nominal.

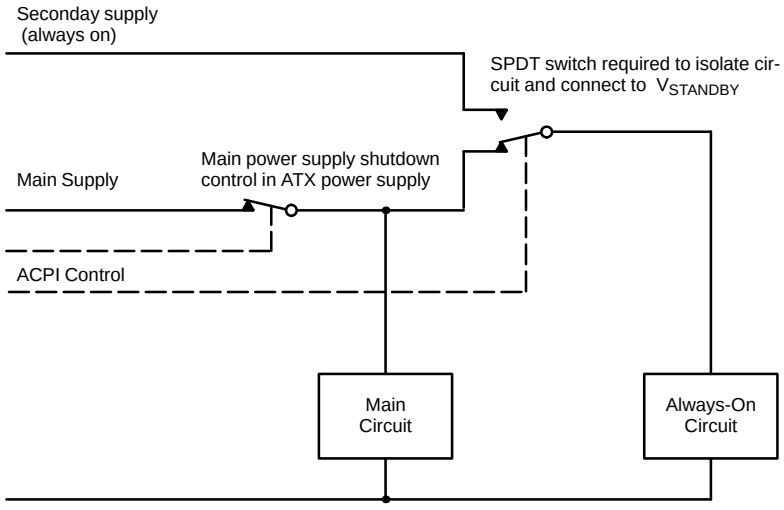


FIGURE 1. ACPI Power Switching Application

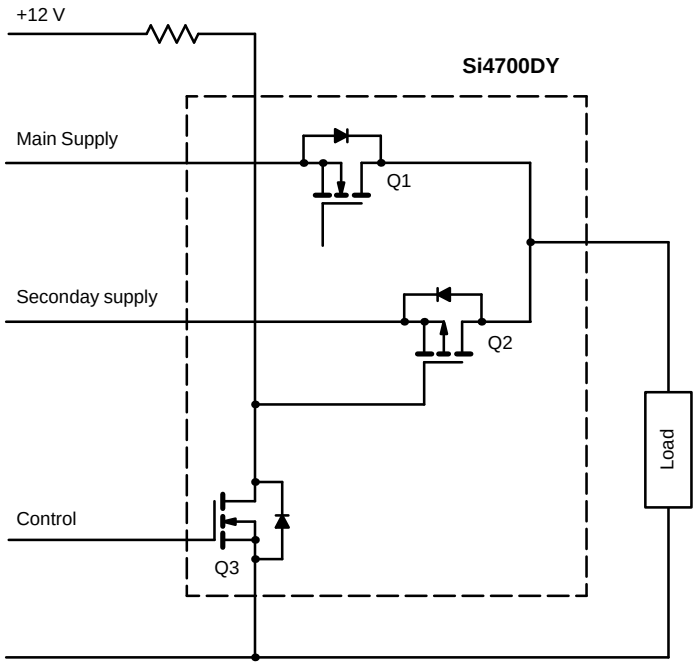


FIGURE 2. Si4700DY used for ACPI Power Switching