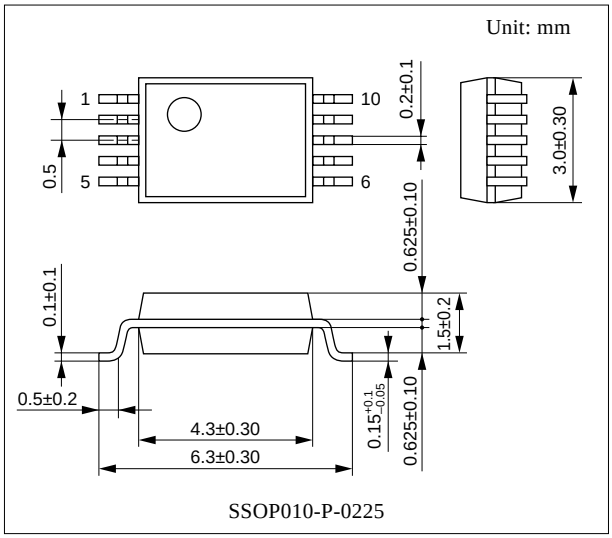
AN8538SH

Single PLL IC for cellular phone

■ Overview

The AN8538SH is a single PLL IC with a fixed frequency dividing ratio for IF local oscillation of a cellular phone. You can generate a local signal of 260.76 MHz by using a reference signal of 19.68 MHz or 19.8 MHz.



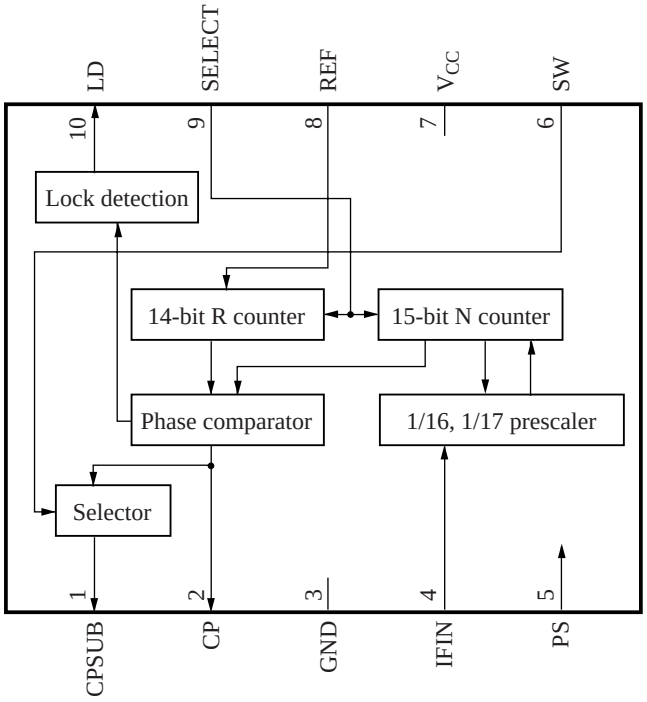
■ Features

- Two reference frequencies of 19.68 MHz and 19.8 MHz are available. (Select by SELECT pin.)
- Power saving operation (V_{CC} = 2.7 V, 0.9 mA typ.)
- Power saving function (10 µA max.)
- Two systems of charge pump output (one of them can be switched to on/off with SW pin.)
- Lock detection function
- SSONF-10D small package

■ Applications

- IF local oscillation for cellular phone terminal (CDMA for North America)

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Description	I/O	Level
1	CPSUB	Sub charge pump output	O	CMOS
2	CP	Charge pump output	O	CMOS
3	GND	GND pin	—	—
4	IFIN	IF input	I	ECL
5	PS	Power save control	I	CMOS
6	SW	Sub charge pump control	I	CMOS
7	V_{CC}	Power supply pin	—	—
8	REF	Reference frequency input	I	ECL
9	SELECT	IF frequency changeover control	I	CMOS
10	LD	Lock detection output	O	CMOS

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	3.6	V
Supply current	I_{CC}	3.5	mA
Power dissipation *2	P_D	12.6	mW
Operating ambient temperature *1	T_{opr}	–30 to +85	°C
Storage temperature *1	T_{stg}	–55 to +125	°C

Note) *1: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.
*2: T_a = 85°C

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC}	2.55 to 3.3	V

■ Electrical Characteristics at V_{CC} = 2.7 V, f_{REFIN} = 19.68 MHz, V_{REFIN} = 0.6 V[p-p], T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Consumption current 1	I_{CC1}	SELECT = low At 260.76 MHz lock	—	0.90	1.21	mA
Consumption current 2	I_{CC2}	Power save mode At PS = low setting	—	0	10	µA
Reference signal input level	V_{REFIN}	f_{REFIN} = 19.68 MHz	0.5	—	1.2	V[p-p]
High-level input voltage	V_{IH}		2.16	—	3.30	V
Low-level input voltage	V_{IL}		0	—	0.4	V
High-level input current	I_{IH}	At V_{IH} = 2.16 V applied	– 1	0	1	µA
Low-level input current	I_{IL}	At V_{IL} = 0 V applied	– 1	0	1	µA

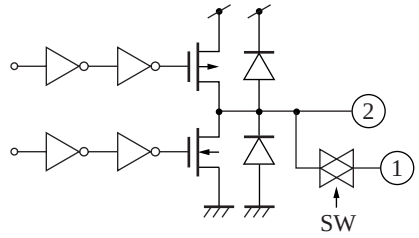
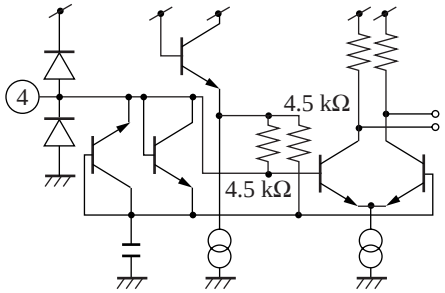
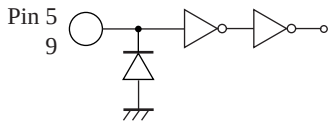
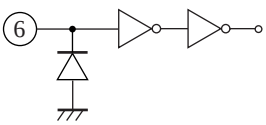
■ Electrical Characteristics at V_{CC} = 2.7 V, f_{REFIN} = 19.68 MHz, V_{REFIN} = 0.6 V[p-p], T_a = 25°C (continued)

• Design reference data

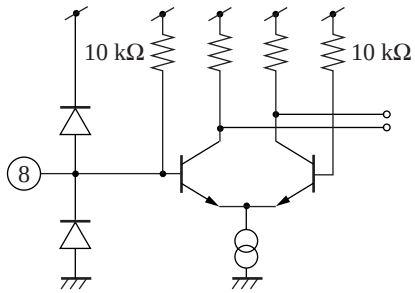
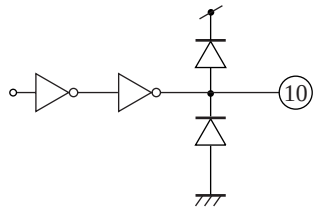
Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Consumption current 1	I_{CC1}	SELECT = low At 260.76 MHz lock	—	0.90	1.34	mA
Consumption current 2	I_{CC2}	SELECT = high At 260.76 MHz lock	—	0.90	1.34	mA
IF input level	V_{IFIN}	f_{IFIN} = 100 MHz to 350 MHz	– 10	—	+2	dBm
Reference signal input level	V_{REFIN}	f_{REFIN} = 10 MHz to 25 MHz	0.5	—	1.2	V[p-p]
Output leak current	I_{OZ}	At V_{OZ} = 0 V, 2.7 V applied	– 1.0	—	+1.0	µA

■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description
1 2		Pin 1: CPSUB Pin 2: CP
3	—	GND
4		IFIN
5		PS
6		SW

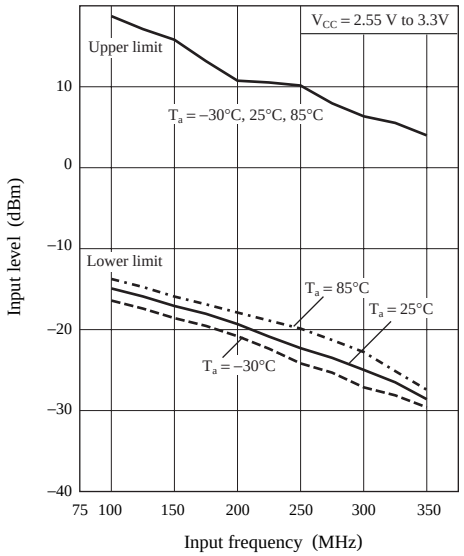
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
7	—	V_{CC}
8		REF
9	Refer to pin 5	SELECT
10		LD

■ Application Notes

1. Input level characteristics

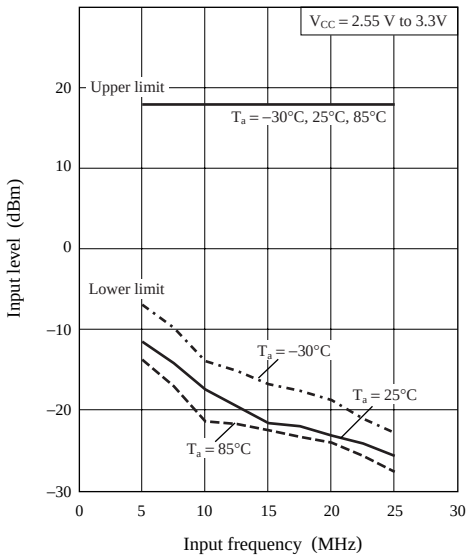
1) IF input level characteristics



■ Application Notes (continued)

1. Input level characteristics (continued)

2) REF input level characteristics



2. Characteristics specification

1) IF select specification

SELECT pin control enables you to switch IF as below:

SELECT = low $\rightarrow f_{OUT}$ = 260.76 MHz, f_R = 60 kHz (P = 16, N = 271, A = 10, R = 328)

SELECT = high $\rightarrow f_{OUT}$ = 260.76 MHz, f_R = 60 kHz (P = 16, N = 271, A = 10, R = 330)

2) Unlock detection and LD output specification

LD output is high in a lock mode and low in an unlock mode. Lock signal is outputted in a power save mode.

SELECT = high: Detection time is 16 µs. About detection accuracy, when a dividing output shifts by $\pm(51 \times 3)$ ns for f_{REF} = 60 kHz, it generates an unlock output.

SELECT = low : Detection time is 16 µs. About detection accuracy, when a dividing output shifts by $\pm(51 \times 3)$ ns for f_{REF} = 60 kHz, it generates an unlock output.

3) Power save control specification

When power save control pin (PS) is high, it is set to an operating mode. When it is low, it is set to power save mode.

4) Analog SW control specification

CPSUB is controlled by SW pin.

SW = low : CPSUB open

SW = high: CPSUB operation

5) Other specification

Set CMOS input pins, such as PS pin, SW pin, SELECT pin, etc., normally to V_{CC} or GND.