AN8539SH

300 MHz-band single PLL IC

■ Overview

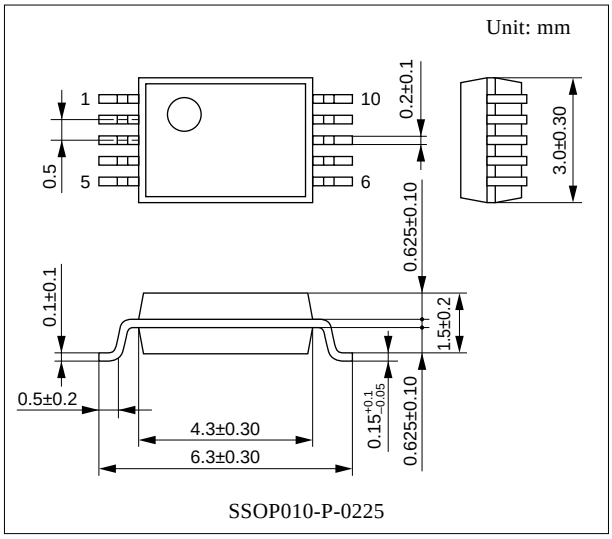
The AN8539SH is a 300 MHz-band, 2nd local OSC PLL IC designed for a cellular phone which allows IF switching to high or low.

■ Features

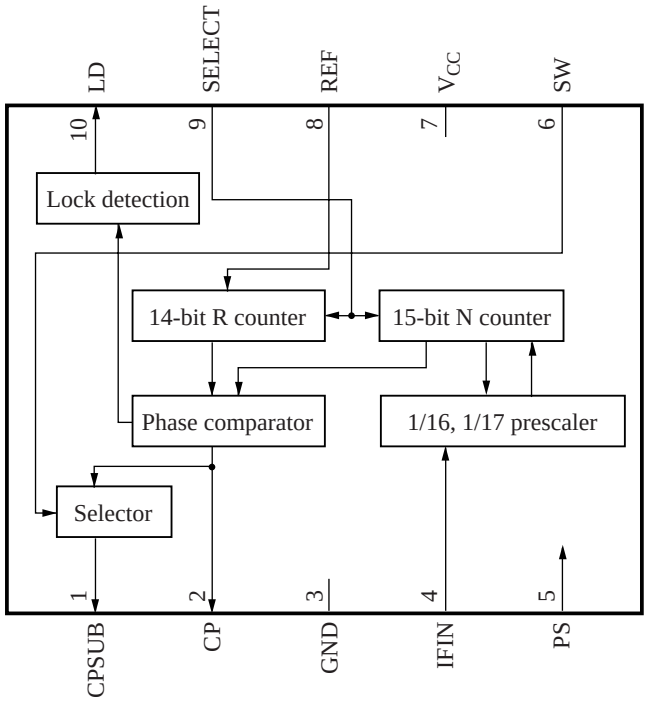
- To be switched to two frequencies. (Select by SELECT pin.)
- Analog SW built-in
- I_{CC} = 900 µA

■ Applications

- Cellular phone



■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Description	I/O	Level
1	CPSUB	Sub charge pump output	O	CMOS
2	CP	Charge pump output	O	CMOS
3	GND	GND pin	—	—
4	IFIN	IF input	I	ECL
5	PS	Power save control	I	CMOS
6	SW	Sub charge pump control	I	CMOS
7	V_{CC}	Power supply pin	—	—
8	REF	Reference frequency input	I	ECL
9	SELECT	IF frequency changeover control	I	CMOS
10	LD	Lock detection output	O	CMOS

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	3.6	V
Supply current	I_{CC}	3.5	mA
Power dissipation *2	P_D	12.6	mW
Operating ambient temperature *1	T_{opr}	–30 to +85	°C
Storage temperature *1	T_{stg}	–55 to +125	°C

Note) *1: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.
*2: T_a = 85°C

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC}	2.55 to 3.3	V

■ Electrical Characteristics at V_{CC} = 2.7 V, f_{REFIN} = 12.8 MHz, V_{REFIN} = 0.6 V[p-p], T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Consumption current 1	I_{CC1}	SELECT = high At 178 MHz lock	—	0.90	1.21	mA
Consumption current 2	I_{CC2}	Power save mode At PS = GND setting	—	0	10	µA
Reference signal input level	V_{REFIN}	f_{REFIN} = 12.8 MHz	0.5	—	1.2	V[p-p]
High-level input voltage	V_{IH}		2.16	—	3.30	V
Low-level input voltage	V_{IL}		0	—	0.54	V
High-level input current	I_{IH}	At V_{IH} = 2.16 V applied	– 1	0	1	µA
Low-level input current	I_{IL}	At V_{IL} = 0 V applied	– 1	0	1	µA

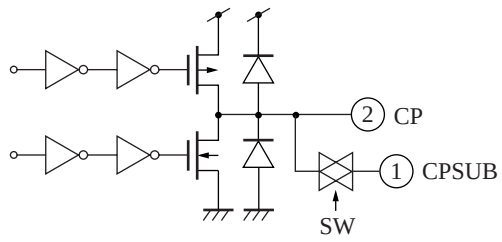
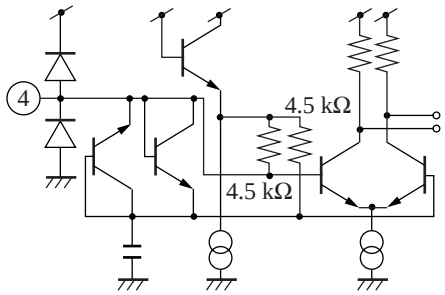
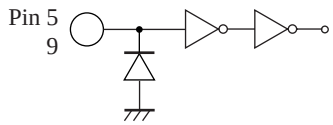
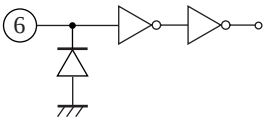
■ Electrical Characteristics at V_{CC} = 2.7 V, f_{REFIN} = 12.8 MHz, V_{REFIN} = 0.6 V[p-p], T_a = 25°C (continued)

• Design reference data at T_a = –30°C to 80°C

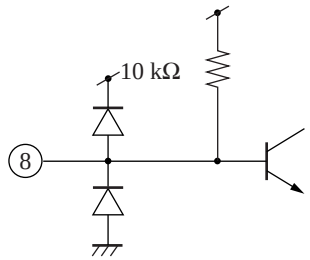
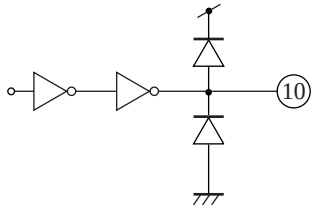
Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Consumption current 1	I_{CC1}	SELECT = high, at 178 MHz lock	—	0.90	1.34	mA
Consumption current 2	I_{CC2}	SELECT = low, at 129.55 MHz lock	—	0.83	1.27	mA
IF input level	V_{IFIN}	f_{IFIN} = 100 MHz to 350 MHz	– 10	—	+2	dBm
Reference signal input level	V_{REFIN}	f_{REFIN} = 10 MHz to 25 MHz	0.5	—	1.2	V[p-p]
Output leak current	I_{OZ}	At V_{OZ} = 0 V, 2.7 V applied	– 1.0	—	+1.0	µA
Charge pump output current 1	I_{OH}	At V_{OH} = 2.16 V applied	– 0.67	– 0.48	– 0.30	mA
Charge pump output current 2	I_{OL}	At V_{OL} = 0.54 V applied	0.32	0.51	0.72	mA

■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description
1 2		Pin 1: CPSUB Pin 2: CP
3	—	GND
4		IFIN input
5		PS input
6		SW input

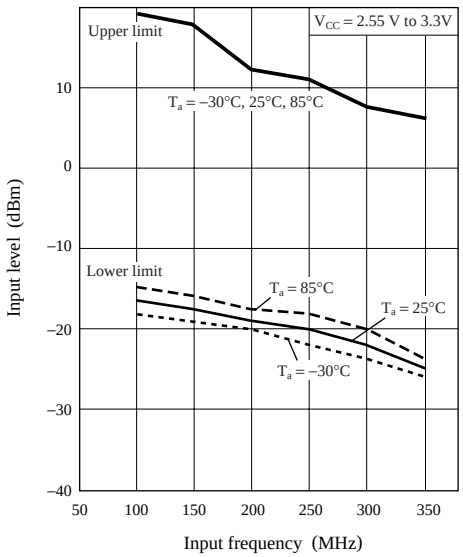
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
7	—	V_{CC}
8		REF
9	Refer to pin 5	SELECT inpuit
10		LD output

■ Application Notes

1. Input level characteristics

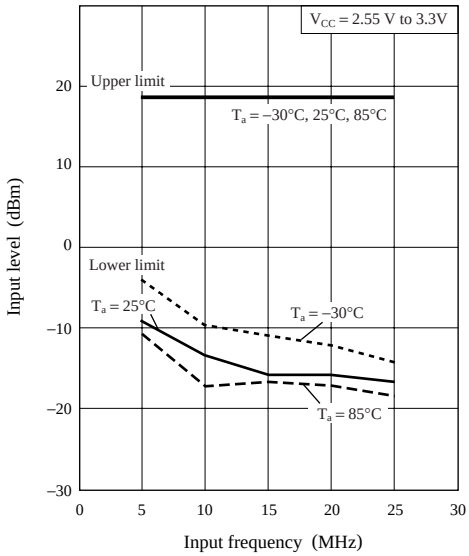
1) IF input level characteristics



■ Application Notes (continued)

1. Input level characteristics (continued)

2) REF input level characteristics



2. Characteristics specification

1) IF select specification

SELECT pin control enables you to switch IF as below:

SELECT = low → f_{OUT} = 129.55 MHz, f_R = 50 kHz (P = 16, N = 161, A = 15, R = 256)

SELECT = high → f_{OUT} = 178 MHz, f_R = 400 kHz (P = 16, N = 27, A = 13, R = 32)

2) Unlock detection and LD output specification

LD output is high in a lock mode and low in an unlock mode. Lock signal is outputted in a power save mode.

SELECT = high: Detection time is 2.6 µs. About detection accuracy, when a dividing output shifts by ±(78 × 3) ns for f_{REF} = 400 kHz, it generates an unlock output.

SELECT = low : Detection time is 20 µs. About detection accuracy, when a dividing output shifts by ±(78 × 3) ns for f_{REF} = 50 kHz, it generates an unlock output.

3) Power save control specification

When power save control pin (PS) is high, it is set to an operating mode. When it is low, it is set to power save mode.

4) Analog SW control specification

CPSUB is controlled by SW pin.

SW = low : CPSUB open

SW = high: CPSUB operation

5) Other specification

Set CMOS input pins, such as PS pin, SW pin, SELECT pin, etc., normally to V_{CC} or GND.

■ Application Circuit Example