

COMMUNICATION SEMICONDUCTORS

**Consumer  
Microcircuits  
Limited**

# CMX639

## Consumer / Commercial CVSD Digital Voice Codec

D/639/2 November 2000

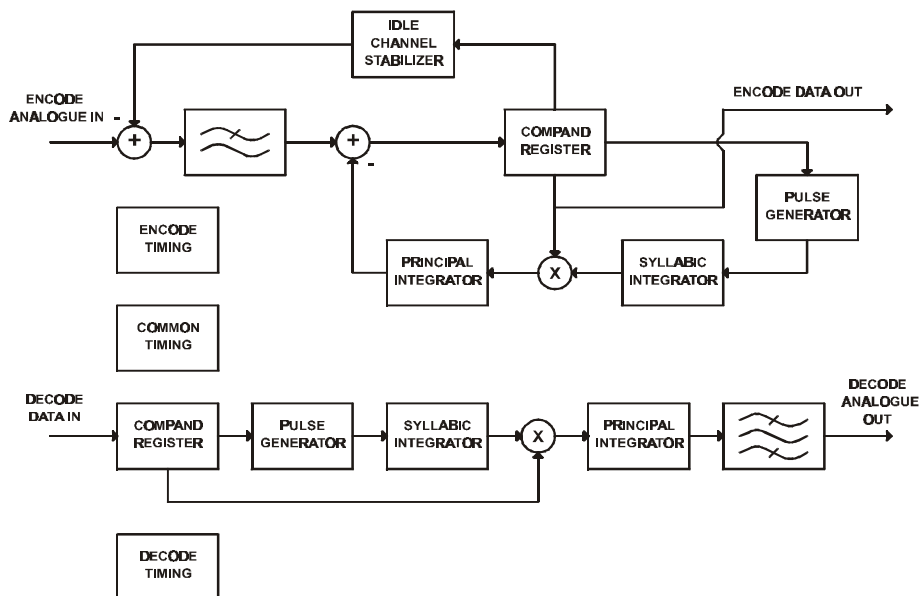
Provisional Issue

### Features

- **Single Chip Full Duplex CVSD codec**
  - Integrated Input and Output Filters
  - Robust Coding for Wireless Links
  - Programmable Sampling Clocks
  - 3 and 4 bit Companding Algorithms
- **Low Power/Small Size for Portable Devices**
  - 1.9mA/2.75mA typ. @ 3.0V/5.0V
  - 3.0V to 5.5V Operation
  - Powersave Mode

### Applications

- **Consumer and Business Handheld Devices**
- **Digital Voice Appliances**
  - Spread Spectrum Wireless
  - Cordless Phones
  - Voice Recording and Storage
  - Delay Lines
- **Time Domain Scramblers**
- **Multiplexers and Switches**



### 1.1 Brief Description

The CMX639 is a Continuously Variable Slope Delta Modulation (CVSD) full duplex CODEC for use in consumer and commercial digital voice communication systems. With its robust and selectable coding algorithms, low cost, very low power, and small size, the CMX639 is ideal for use in a wide variety of consumer and business digital voice applications. Its completely integrated CODEC simplifies design and eliminates the costs, complexity and risk of external filters and software algorithms.

8kbps to 128kbps data/sampling clock rates are supported both via external clock signals or internally generated, programmable clocks. Internal data/sampling clocks are derived from an on-chip reference oscillator that uses an external clock crystal. An internal data/sampling clock output signal is provided to synchronize external circuits, if desired. Multiplexer applications are also well supported by the encoder output's three-state/high impedance enable feature.

The CMX639 operates from 2.7V to 5.5V supplies and is available in the following packages: 24-pin TSSOP (CMX639E2), 16-pin SOIC (CMX639D4) and 22-pin PDIP (CMX639P6).

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## 1.2 Block Diagram

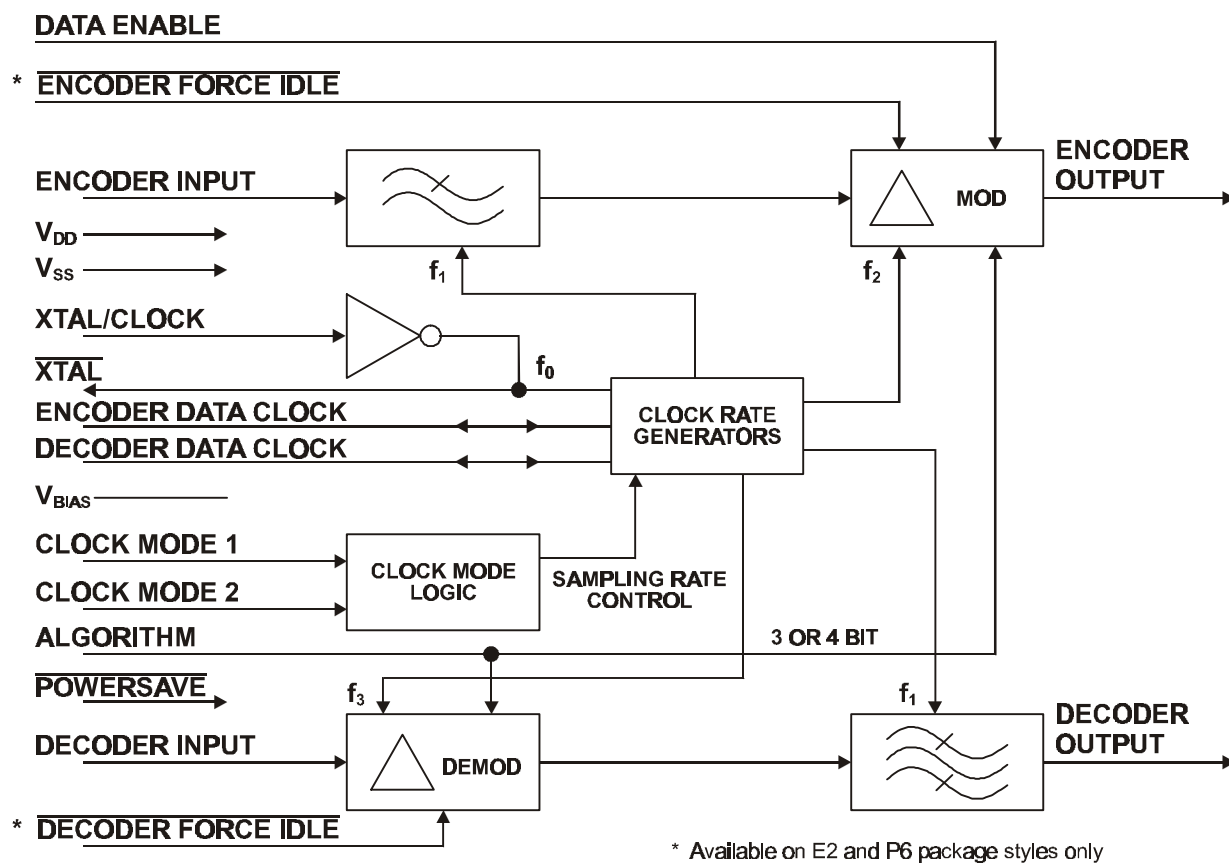


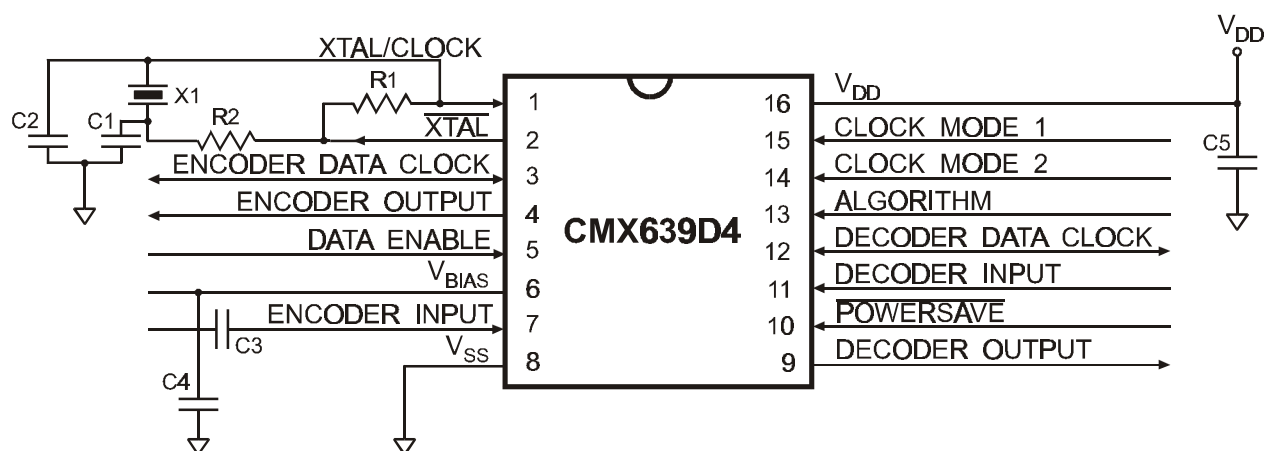
Figure 1 Block Diagram

### 1.3 Signal List

| P6<br>22-pin<br>PDIP | E2<br>24-pin<br>TSSOP | D4<br>16-pin<br>SOIC | Signal Name              | Type             | Description                                                                                                                                                                                                                                                                                   |
|----------------------|-----------------------|----------------------|--------------------------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                    | 1                     | 1                    | Xtal/Clock               | input            | Input to the clock oscillator inverter. A 1.024MHz Xtal input or externally derived clock is injected here.                                                                                                                                                                                   |
|                      | 2                     |                      | N/C                      |                  | No Connection                                                                                                                                                                                                                                                                                 |
| 2                    | 3                     | 2                    | $\overline{\text{Xtal}}$ | output           | The 1.024 MHz output of the clock oscillator inverter.                                                                                                                                                                                                                                        |
| 3                    | 4                     |                      | N/C                      |                  | No Connection                                                                                                                                                                                                                                                                                 |
| 4                    | 5                     | 3                    | Encoder Data Clock       | input/<br>output | A logic I/O port. External encode clock input or internal data clock output. Clock frequency is dependent upon Clock Mode 1 and 2 inputs and Xtal frequency. Note: No internal pull-up is provided. See Table 3.                                                                              |
| 5                    | 6                     | 4                    | Encoder Output           | output           | The encoder digital output. This is a three-state output whose condition is set by the Data Enable and Powersave inputs. See Table 2.                                                                                                                                                         |
| 6                    | 7                     | Not present          | Encoder Force Idle       | input            | When this pin is at a logical '0' the encoder is forced to an idle state and the encoder digital output is '0101...', a perfect idle pattern. When this pin is a logical '1' the encoder encodes as normal. Internal 1M $\Omega$ pull-up.                                                     |
| 7                    | 8                     | 5                    | Data Enable              | input            | Data is made available at the encoder output pin by control of this input. See Encoder Output pin. Internal 1 M $\Omega$ pull-up.                                                                                                                                                             |
| 8                    | 9                     |                      | N/C                      |                  | No Connection                                                                                                                                                                                                                                                                                 |
| 9                    | 10                    | 6                    | V <sub>BIAS</sub>        |                  | Normally at V <sub>DD</sub> /2, this pin should be externally decoupled by capacitor C4. Internally pulled to V <sub>SS</sub> when Powersave is a logical '0'.                                                                                                                                |
| 10                   | 11                    | 7                    | Encoder Input            | input            | The analog signal input. Internally biased at V <sub>DD</sub> /2, this input requires an external coupling capacitor. The source impedance driving the coupling capacitor should be less than 1k $\Omega$ . A lower driving source impedance will reduce encoder output channel noise levels. |
| 11                   | 12                    | 8                    | V <sub>SS</sub>          | power            | Negative Supply                                                                                                                                                                                                                                                                               |
| 12                   | 13                    |                      | N/C                      |                  | No Connection                                                                                                                                                                                                                                                                                 |
| 13                   | 14                    | 9                    | Decoder Output           | output           | The recovered analog signal is output at this pin. It is the buffered output of a lowpass filter and requires external components. During 'Powersave' this output is open circuit.                                                                                                            |
| 14                   | 15                    |                      | N/C                      |                  | No Connection                                                                                                                                                                                                                                                                                 |

| P6<br>22-pin<br>PDIP | E2<br>24-pin<br>TSSOP | D4<br>16-pin<br>SOIC | Signal Name                            | Type             | Description                                                                                                                                                                                                                                                                                                                                                |
|----------------------|-----------------------|----------------------|----------------------------------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15                   | 16                    | 10                   | $\overline{\text{Powersave}}$          | Input            | A logic '0' at this pin puts most parts of the codec into a quiescent, non-operational state. When at a logical '1', the codec operates normally. Internal 1 M $\Omega$ pull-up.                                                                                                                                                                           |
|                      | 17                    |                      | N/C                                    |                  | No Connection                                                                                                                                                                                                                                                                                                                                              |
| 16                   | 18                    | Not present          | $\overline{\text{Decoder Force Idle}}$ | input            | A logic '0' at this pin gates a '0101...' pattern internally to the decoder so that the Decoder Output goes to $V_{DD}/2$ . When this pin is a logical '1' the decoder operates as normal. Internal 1M $\Omega$ pull-up.                                                                                                                                   |
| 17                   | 19                    | 11                   | Decoder Input                          | input            | The received digital signal input. Internal 1 M $\Omega$ pull-up.                                                                                                                                                                                                                                                                                          |
| 18                   | 20                    | 12                   | Decoder Data Clock                     | input/<br>output | A logic I/O port. External decode clock input or internal data clock output. Clock frequency is dependent upon Clock Mode 1 and 2 inputs and Xtal frequency. Note: No internal pull-up is provided. See Table 3.                                                                                                                                           |
| 19                   | 21                    | 13                   | Algorithm                              | input            | A logic '1' at this pin sets this device for a 3-bit companding algorithm. A logical '0' sets a 4-bit companding algorithm. Internal 1 M $\Omega$ pull-up.                                                                                                                                                                                                 |
| 20                   | 22                    | 14                   | Clock Mode 2                           | input            | Clock rates refer to $f = 1.024\text{MHz}$ Xtal/Clock input. During internal operation the data clock frequencies are available at these ports for external circuit synchronization. Independent or common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode. Internal 1M $\Omega$ pull-ups. See Table 3. |
| 21                   | 23                    | 15                   | Clock Mode 1                           | input            |                                                                                                                                                                                                                                                                                                                                                            |
| 22                   | 24                    | 16                   | $V_{DD}$                               | power            | Positive Supply. A single 3.0V to 5.5V supply is required. This pin should be externally decoupled to $V_{SS}$ by capacitor C5.                                                                                                                                                                                                                            |

## 1.4 External Components



**Figure 2 Recommended External Connections**

|    |        |             |            |
|----|--------|-------------|------------|
| R1 | Note 1 | 1M $\Omega$ | $\pm 10\%$ |
| C1 | Note 2 | 33pF        | $\pm 20\%$ |
| C2 | Note 2 | 33pF        | $\pm 20\%$ |
| C3 | Note 3 | 1.0 $\mu$ F | $\pm 20\%$ |

|    |           |             |            |
|----|-----------|-------------|------------|
| C4 | Note 4    | 1.0 $\mu$ F | $\pm 20\%$ |
| C5 | Note 5    | 1.0 $\mu$ F | $\pm 20\%$ |
| X1 | Note 6, 7 | 1.024MHz    |            |

**Table 1 Recommended External Components**

### Notes:

- Oscillator inverter bias resistor
- Xtal circuit load capacitor
- The drive source impedance connected to the coupling capacitor's input node, rather than the CMX639 ENCODER INPUT pin node, should be less than 1k $\Omega$ . Output idle channel noise levels will improve with even lower source impedances driving the coupling capacitor's input node.
- Bias decoupling capacitor
- V<sub>DD</sub> decoupling capacitor
- A 1.024MHz Xtal/Clock input will yield exactly 16kbps/32kbps/64kbps internally generated data clock rates
- For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V<sub>DD</sub>, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, please consult your crystal manufacturer.

## 1.5 General Description

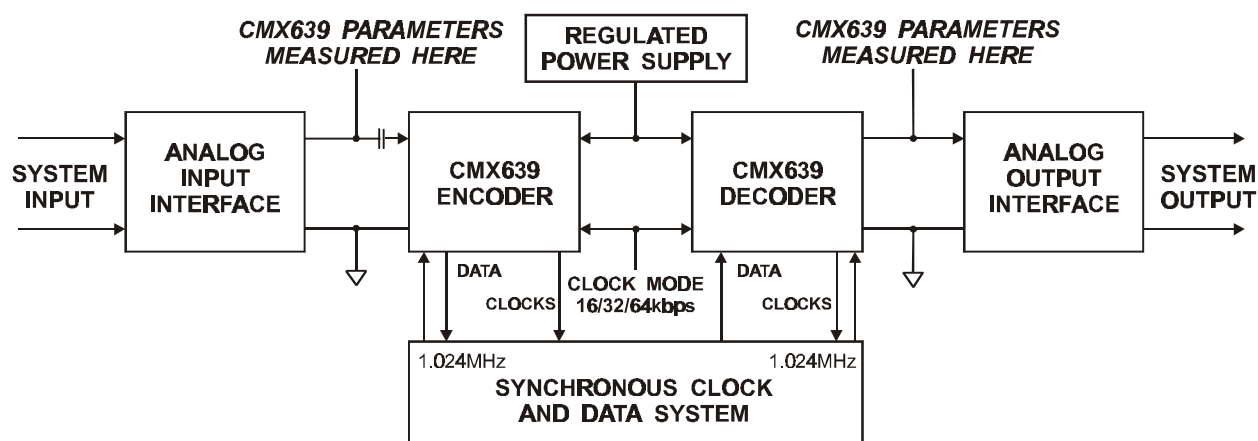
| Data Enable | Powersave  | Encoder Output        |
|-------------|------------|-----------------------|
| 1           | 1          | Enable                |
| 0           | don't care | High Z (open circuit) |
| 1           | 0          | V <sub>SS</sub>       |

**Table 2 Encoder Output**

| Clock Mode 1 | Clock Mode 2 | Data/Sampling Clock Rate<br>(CLOCK/XTAL = f = 1.024MHz) | Example for f = 1.024MHz      |
|--------------|--------------|---------------------------------------------------------|-------------------------------|
| 0            | 0            | External Clocks                                         | External Clocks               |
| 0            | 1            | Internally generated @ f/16                             | Internally generated @ 64kbps |
| 1            | 0            | Internally generated @ f/32                             | Internally generated @ 32kbps |
| 1            | 1            | Internally generated @ f/64                             | Internally generated @ 16kbps |

**Table 3 Clock Modes and Pins**

## 1.6 Application Notes



**Figure 3 System Configuration using the CMX639**

## 1.7 Performance Specification

### 1.7.1 Electrical Performance

#### 1.7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

|                                                   | Min. | Max.           | Units |
|---------------------------------------------------|------|----------------|-------|
| Supply ( $V_{DD} - V_{SS}$ )                      | -0.3 | 7.0            | V     |
| Voltage on any pin to $V_{SS}$                    | -0.3 | $V_{DD} + 0.3$ | V     |
| Current into or out of $V_{DD}$ and $V_{SS}$ pins | -30  | +30            | mA    |
| Current into or out of any other pin              | -20  | +20            | mA    |

| <b>P6 Package</b>                                                   | Min. | Max. | Units                  |
|---------------------------------------------------------------------|------|------|------------------------|
| Total Allowable Power Dissipation at $T_{amb} = 25^{\circ}\text{C}$ |      | 800  | mW                     |
| ... Derating                                                        |      | 10   | mW/ $^{\circ}\text{C}$ |
| Storage Temperature                                                 | -40  | +125 | $^{\circ}\text{C}$     |
| Operating Temperature                                               | -40  | +85  | $^{\circ}\text{C}$     |

| <b>E2 Package</b>                                                   | Min. | Max. | Units                  |
|---------------------------------------------------------------------|------|------|------------------------|
| Total Allowable Power Dissipation at $T_{amb} = 25^{\circ}\text{C}$ |      | 300  | mW                     |
| ... Derating                                                        |      | 3.0  | mW/ $^{\circ}\text{C}$ |
| Storage Temperature                                                 | -40  | +125 | $^{\circ}\text{C}$     |
| Operating Temperature                                               | -40  | +85  | $^{\circ}\text{C}$     |

| <b>D4 Package</b>                                                   | Min. | Max. | Units                  |
|---------------------------------------------------------------------|------|------|------------------------|
| Total Allowable Power Dissipation at $T_{amb} = 25^{\circ}\text{C}$ |      | 800  | mW                     |
| ... Derating                                                        |      | 10   | mW/ $^{\circ}\text{C}$ |
| Storage Temperature                                                 | -40  | +125 | $^{\circ}\text{C}$     |
| Operating Temperature                                               | -40  | +85  | $^{\circ}\text{C}$     |

#### 1.7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

|                              | Notes | Min.  | Max.  | Units              |
|------------------------------|-------|-------|-------|--------------------|
| Supply ( $V_{DD} - V_{SS}$ ) |       | 2.7   | 5.5   | V                  |
| Operating Temperature        |       | -40   | +85   | $^{\circ}\text{C}$ |
| Xtal Frequency               |       | 0.500 | 2.048 | MHz                |



### 1.7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 1.024 MHz, Sample Clock Rate = 32 kbps, Audio Test Frequency = 820 Hz,  
 $V_{DD}$  = 3.0V to 5.5V,  $T_{amb}$  = - 40°C to +85°C, Audio Level 0dB ref (0dBm0) = 489mV rms.

| Static Values                        | Notes | Min.         | Typ.    | Max.         | Units      |
|--------------------------------------|-------|--------------|---------|--------------|------------|
| $I_{DD}$ (powersaved)                | 6     |              | 600     |              | $\mu A$    |
| $I_{DD}$ (enabled) @ $V_{DD}$ = 3.0V | 6     |              | 1.90    |              | mA         |
| $I_{DD}$ (enabled) @ $V_{DD}$ = 5.0V | 6     |              | 2.75    |              | mA         |
| Input Logic '1'                      |       | 70% $V_{DD}$ |         |              | V          |
| Input Logic '0'                      |       |              |         | 30% $V_{DD}$ | V          |
| Output Logic '1'                     |       | 80% $V_{DD}$ |         |              | V          |
| Output Logic '0'                     |       |              |         | 20% $V_{DD}$ | V          |
| Digital Input Impedance              |       |              |         |              |            |
| Logic I/O pins                       |       | 1.0          |         |              | M $\Omega$ |
| Logic Input pins, Pull-up Resistor   | 1     | 300          |         |              | k $\Omega$ |
| Digital Output Impedance             |       |              |         | 4.0          | k $\Omega$ |
| Analog Input Impedance               | 2     |              | 100     |              | k $\Omega$ |
| Analog Output Impedance              |       |              |         | 800          | $\Omega$   |
| Three State Output Leakage           |       |              | $\pm 4$ |              | $\mu A$    |
| Insertion Loss                       | 3     |              | 0       |              | dB         |

| Dynamic Values                       | Notes  | Min.  | Typ.  | Max.  | Units |
|--------------------------------------|--------|-------|-------|-------|-------|
| <b>Encoder:</b>                      |        |       |       |       |       |
| Analog Signal Input Levels           |        |       |       |       |       |
| V <sub>DD</sub> = 3.0V               | 7      | -37   |       | 6     | dB    |
| V <sub>DD</sub> = 5.0V               | 7      | -33   |       | 10    | dB    |
| Principal Integrator Frequency       |        |       | 160   |       | Hz    |
| Encoder Passband                     | 4      |       | 3240  |       | Hz    |
| Compand Time Constant                |        |       | 5     |       | ms    |
| <b>Decoder:</b>                      |        |       |       |       |       |
| Analog Signal Output Levels          |        |       |       |       |       |
| V <sub>DD</sub> = 3.0V               | 7      | -37   |       | 6     | dB    |
| V <sub>DD</sub> = 5.0V               | 7      | -33   |       | 10    | dB    |
| Decoder Passband                     | 4      |       | 3200  |       | Hz    |
| <b>Encoder Decoder (Full Codec):</b> |        |       |       |       |       |
| Passband                             | 4      | 300   |       | 3400  | Hz    |
| Stopband                             |        | 6     |       | 10    | kHz   |
| Stopband Attenuation                 |        |       | 60    |       | dB    |
| Passband Gain                        |        |       | 0     |       | dB    |
| Passband Ripple                      |        | -3.0  |       | 3.0   | dB    |
| Output Noise (Input Short Circuit)   | 8      |       | -60   |       | dBm0p |
| Perfect Idle Channel Noise           |        |       |       |       |       |
| (Encode Forced)                      | 8, 9   |       | -63   |       | dBm0p |
| Group Delay Distortion               | 5      |       |       |       |       |
| (1000Hz - 2600Hz)                    |        |       |       | 450   | μs    |
| (600Hz - 2800Hz)                     |        |       |       | 750   | μs    |
| (500Hz - 3000Hz)                     |        |       |       | 1500  | μs    |
| Xtal/Clock Frequency                 | 10, 11 | 0.500 | 1.024 | 2.048 | MHz   |

**Notes:**

1. All logic inputs except Encoder and Decoder Data clocks.
2. The source impedance driving the coupling capacitor should be less than 1kΩ. A lower driving source impedance will reduce encoder output channel noise levels.
3. For an Encoder/Decoder combination.
4. See Figure 5.
5. Group Delay Distortion for the full codec is relative to the delay with an 820Hz, -20dB signal at the encoder input.
6. Not including any current drawn from the device pins by external circuits.
7. Recommended values.
8. dBm0p units are measured after the application of a psophometrically weighted filter that is commonly applied in voice communication applications per CCITT Recommendation G.223.
9. Forced idle encode/decode control not available on D4 (16-pin SOIC) package.
10. Some applications may benefit from the use of an Xtal/Clock frequency other than 1.024MHz.  
Note: Codec time constants and filter response curves are effectively proportional to Xtal/Clock frequency

and so will shift with the use of Xtal/Clock frequencies other than 1.024MHz. For example, the specified Encoder Decoder (Full Codec) passband of 300Hz min. to 3400Hz max. for a 1.024MHz Xtal/Clock will shift to 600Hz min. to 6800Hz max. when the device is operated from a 2.048MHz Xtal/Clock. For this reason, all CMX639 codecs involved in the same communications link should usually be operated from the same Xtal/Clock frequency.

Example 1: A design saves the cost of a 1.024MHz Xtal or clock generator by making use of an already existing clock source of a frequency other than 1.024MHz.

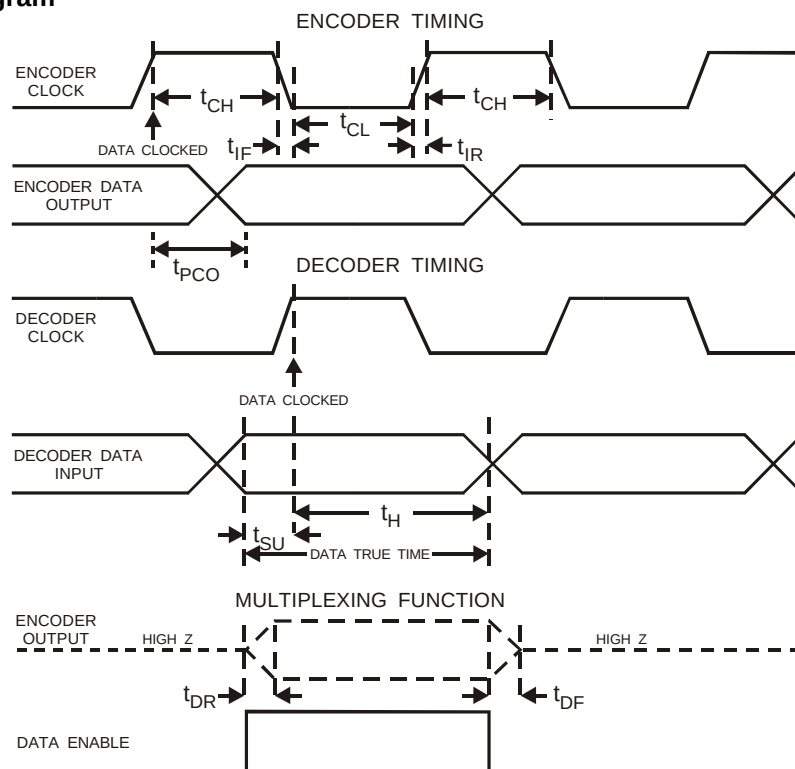
Example 2: Best noise performance is achieved when the CMX639 codec data clock is internally generated. If a codec bit rate other than 16kbps, 32kbps or 64kbps is desired then an Xtal/Clock different from 1.024MHz can be used to proportionately shift the available set of internally generated clock rates, as needed.

Example 3: To increase the codec high frequency response and audio bandwidth a faster Xtal/Clock speed can be used. Other designs may prefer the proportionately higher codec bandwidths and data rates that can be supported with faster clock speeds.

11. In general, optimum codec performance is achieved when both encoder and decoder Xtal/Clock signals are synchronized. While this is practical in many telecom applications, it may not be so for others such as wireless data links. The CMX639 decoder can generally deliver best performance when its data clock is recovered/derived from the received data stream and applied as an external data clock to the decoder as per the decoder timing depicted in Figure 4. Nonetheless, some Xtal/Clock frequency and data rate combinations are better served by the use of internal clocks. Experimentation with each specific design may provide the best guidance for making this design choice.

### 1.7.1.3 Operating Characteristics (continued)

#### Timing Diagram



**Figure 4 Serial Bus Timing**

For the following conditions unless otherwise specified:

Xtal Frequency = 1.024 MHz,  $V_{DD}$  = 3.0V to 5.0V,  $T_{amb}$  = - 40°C to +85°C.

| Serial Bus Timing (ref. Figure 4) |                            | Notes | Min. | Typ. | Max. | Units   |
|-----------------------------------|----------------------------|-------|------|------|------|---------|
| $t_{CH}$                          | Clock 1 pulse width        |       | 1.0  |      |      | $\mu$ s |
| $t_{CL}$                          | Clock 0 pulse width        |       | 1.0  |      |      | $\mu$ s |
| $t_{IR}$                          | Clock rise time            |       | 0    | 100  |      | ns      |
| $t_{IF}$                          | Clock fall time            |       |      | 100  |      | ns      |
| $t_{SU}$                          | Data set-up time           |       |      |      | 450  | ns      |
| $t_H$                             | Data hold time             |       | 600  |      |      | ns      |
| $t_{SU} + t_H$                    | Data true time             |       |      | 1.5  |      | $\mu$ s |
| $t_{PCO}$                         | Clock to output delay time |       |      | 750  |      | ns      |
| $t_{DR}$                          | Data rise time             |       |      | 100  |      | ns      |
| $t_{DF}$                          | Data fall time             |       |      | 100  |      | ns      |

### 1.7.1.3 Operating Characteristics (continued)

#### Typical Codec Performance

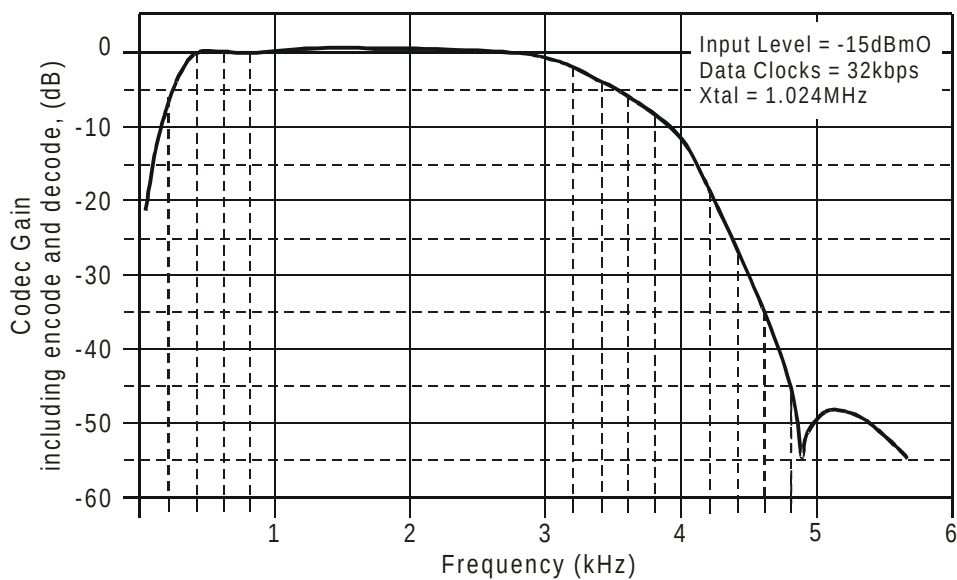


Figure 5 Typical Frequency Response (32kbps)

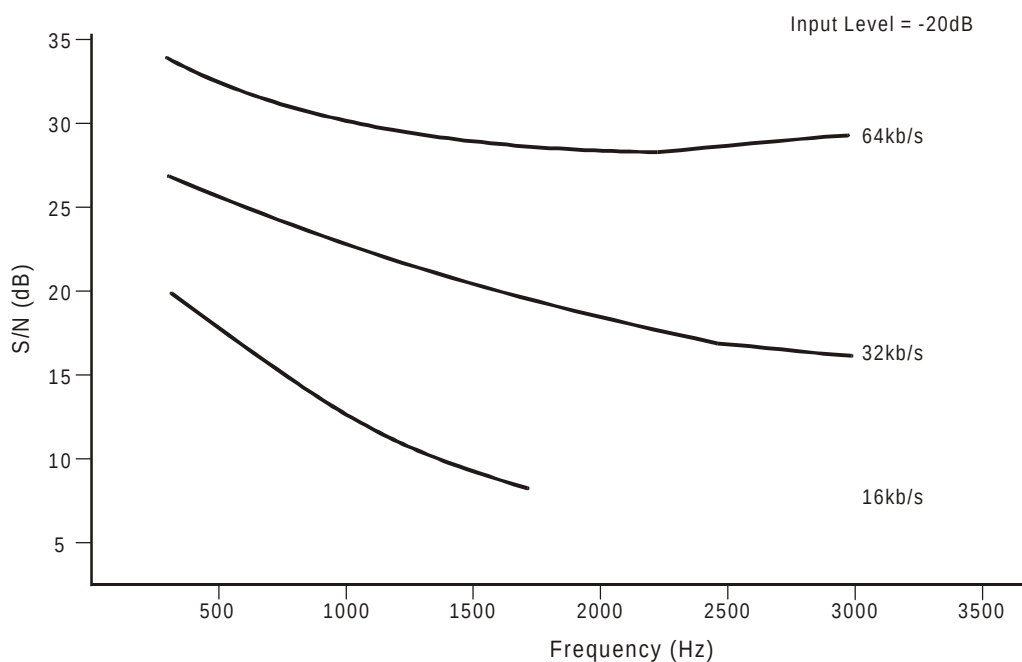
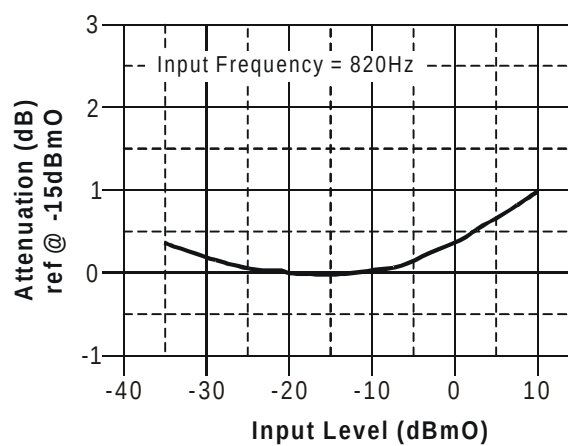
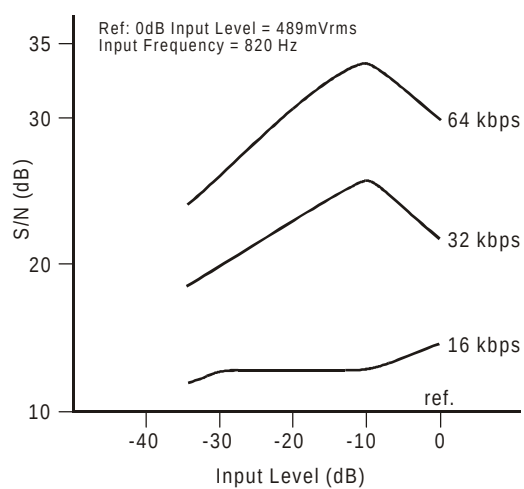


Figure 6 Typical S/N Ratio with Input Frequency



**Figure 7 Typical Variation of Gain with Input Level (32kbps)**



**Figure 8 Typical S/N Ratio with Input Level**

## 1.7.2 Packaging

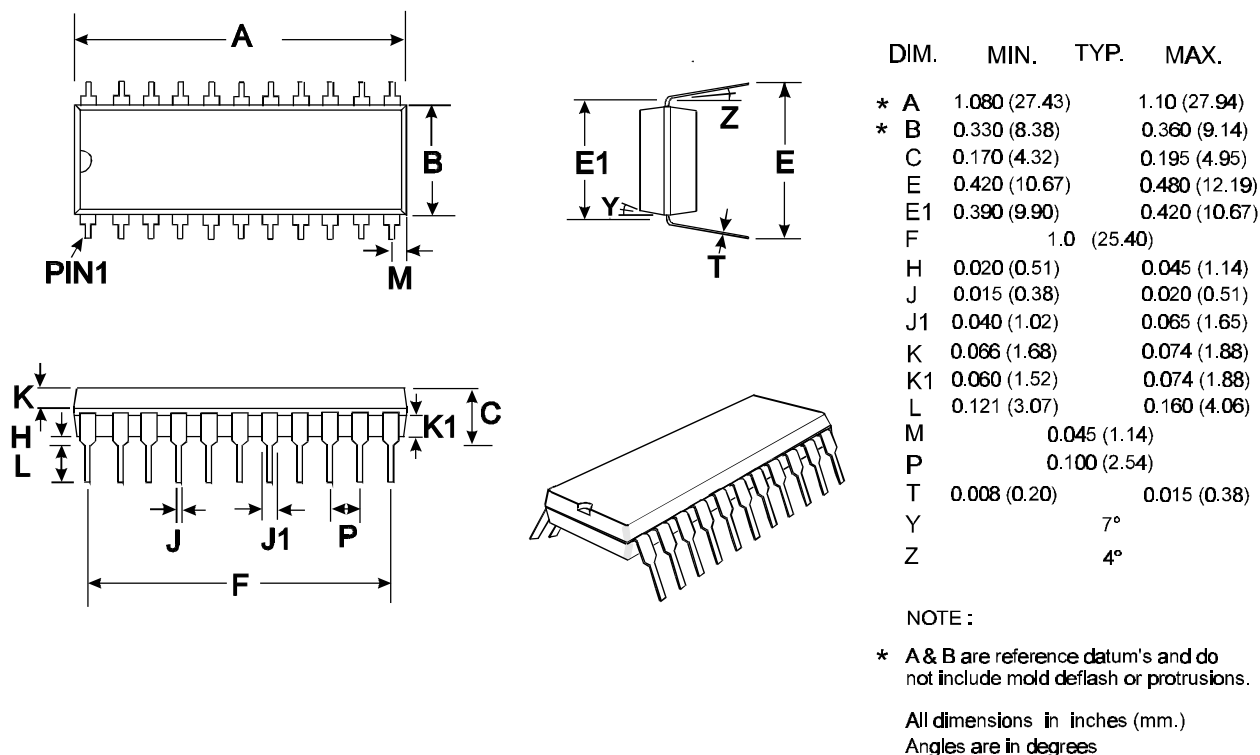


Figure 9 P6 Mechanical Outline: Order as part no. CMX639P6

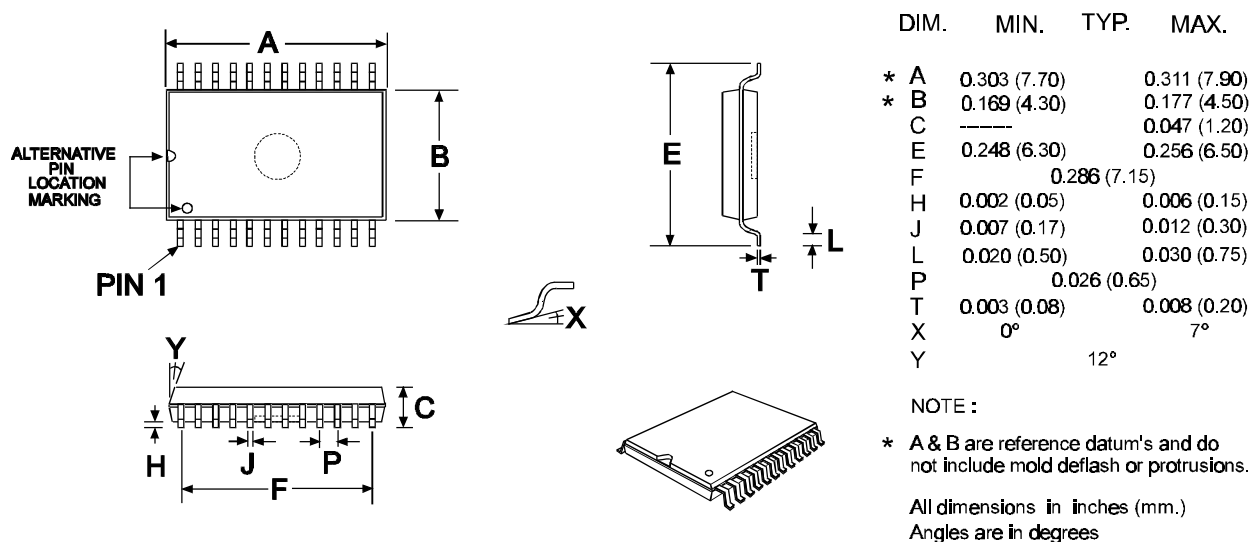


Figure 10 E2 Mechanical Outline: Order as part no. CMX639E2

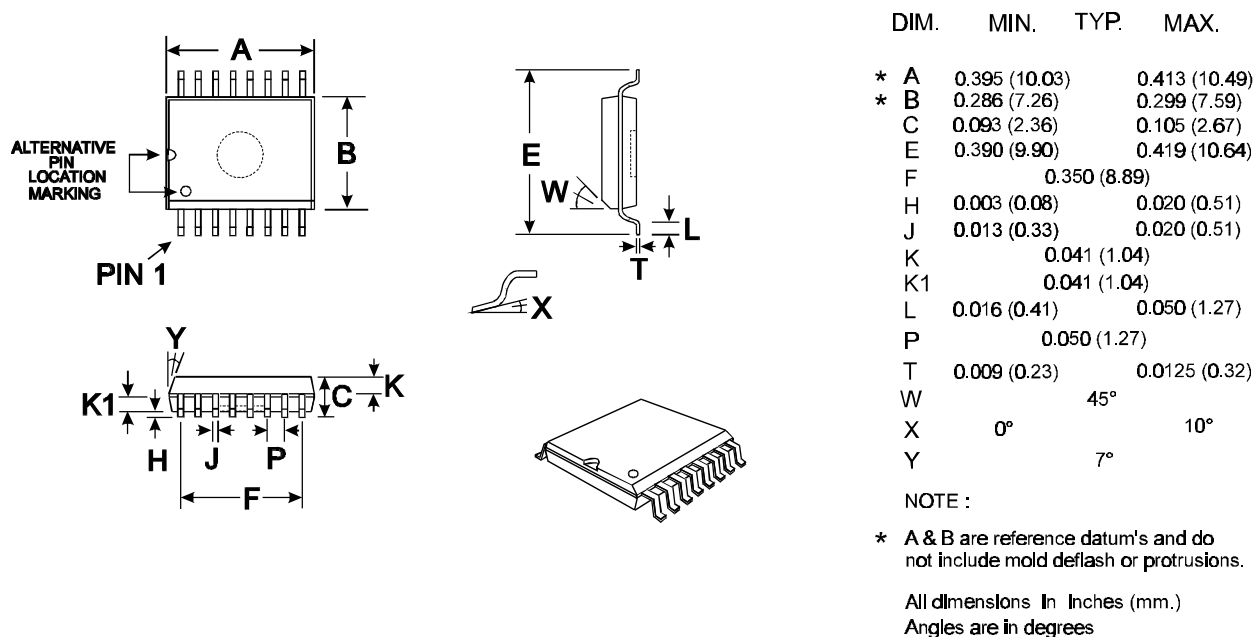


Figure 9 D4 Mechanical Outline: Order as part no. CMX639D4

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.



## CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc (*Consumer Microcircuits Limited (UK)*, *MX-COM, Inc (USA)* and *CML Microcircuits (Singapore) Pte Ltd*) have undergone name changes and, whilst maintaining their separate new names (*CML Microcircuits (UK) Ltd*, *CML Microcircuits (USA) Inc* and *CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.

These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

### CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

Company contact information is as below:



**CML Microcircuits  
(UK) Ltd**  
COMMUNICATION SEMICONDUCTORS

Oval Park, Langford, Maldon,  
Essex, CM9 6WG, England  
Tel: +44 (0)1621 875500  
Fax: +44 (0)1621 875600  
uk.sales@cmlmicro.com  
www.cmlmicro.com



**CML Microcircuits  
(USA) Inc.**  
COMMUNICATION SEMICONDUCTORS

4800 Bethania Station Road,  
Winston-Salem, NC 27105, USA  
Tel: +1 336 744 5050,  
0800 638 5577  
Fax: +1 336 744 5054  
us.sales@cmlmicro.com  
www.cmlmicro.com



**CML Microcircuits  
(Singapore) Pte Ltd**  
COMMUNICATION SEMICONDUCTORS

No 2 Kallang Pudding Road, 09-05/  
06 Mactech Industrial Building,  
Singapore 349307  
Tel: +65 7450426  
Fax: +65 7452917  
sg.sales@cmlmicro.com  
www.cmlmicro.com