HMC282

GaAs MMIC LOW NOISE AMPLIFIER 36 - 40 GHz

FEBRUARY 2001 v01.0700

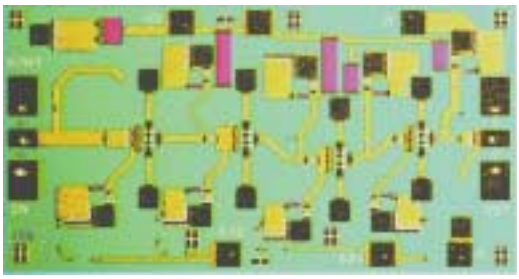
Features

NOISE FIGURE: 3.5 dB

STABLE GAIN vs. TEMPERATURE: 26dB ± 1.2dB

SMALL SIZE: 1.11 mm x 2.07 mm

IDEAL FOR 38 GHz RADIOS, E1 & T1



General Description

The HMC282 chip is a four stage GaAs MMIC Low Noise Amplifier (LNA) which covers the frequency range of 36 to 40 GHz. The chip can easily be integrated into Multi-Chip Modules (MCMs) due to its small (2.30 mm^2) size. The chip utilizes a GaAs PHEMT process offering 26 dB gain from a bias supply of +3.5V @ 90 mA with a noise figure of 3.5 dB. This LNA can be used in millimeterwave point-to-point radios, VSAT, and other SATCOM applications. All data is with the chip in a 50 ohm test fixture connected via ribbon bonds of minimal length. The HMC282 may be used in conjunction with the HMC259 mixer to realize a millimeterwave system receiver.

Guaranteed Performance, *Vdd = +3.5V*, Idd = 90mA, -55 to +85 deg C*

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		36 - 40			37 - 39		GHz
Gain	21	27		21	26		dB
Gain Flatness (Any 1Ghz BW)		± 1			± 1		dB
Noise Figure		3.8	5.8		3.5	5.3	dB
Input Return Loss		7			6		dB
Output Return Loss		5			5		dB
Reverse Isolation	40	46		40	46		dB
Output Power for 1dB Compression (P1dB)	5	9		5	9		dBm
Saturated Output Power (Psat)		12			12		dBm
Output Third Order Intercept (IP3)	18	25		21	27		dBm
Supply Voltage (Vdd)	3.25	3.5	3.75	3.25	3.5	3.75	Vdc
Gate Bias Voltage (Vg1, 2 & Vg3, 4)		-0.45 / -0.3			-0.45 / -0.3		Vdc
Supply Current (Idd) (Vdd = +3.5V, Vg1, 2, 3, 4 = -0.15V Typ.)		90	140		90	140	mA

* Vdd = +3.5V , adjust Vg1, 2 & Vg3, 4 between-2.0 to +0.4V to achieve Idd = 90 mA typical.

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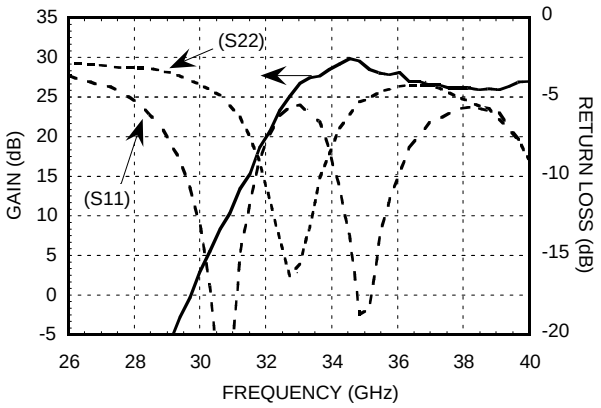
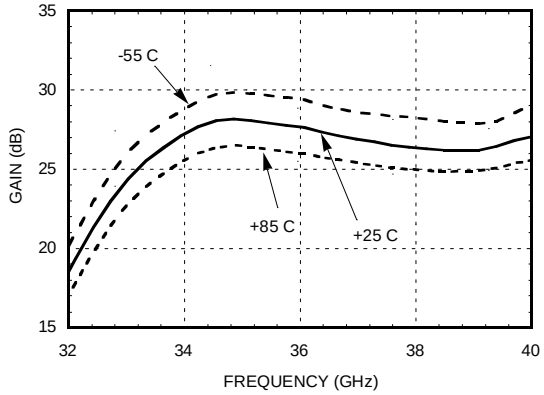
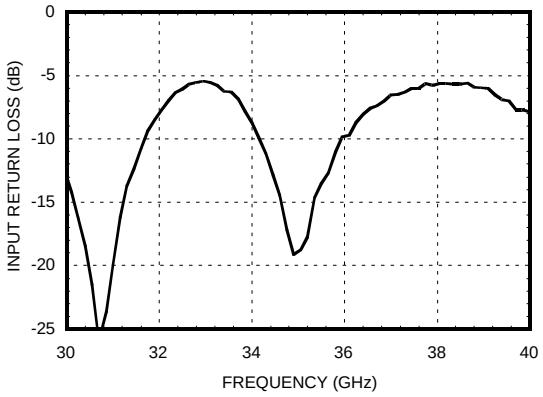
Broadband Gain & Return Loss



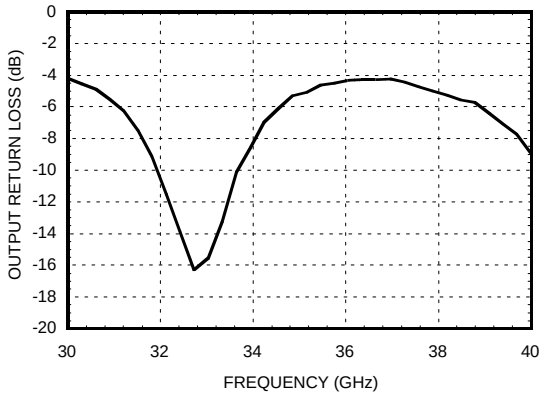
Gain vs. Temperature



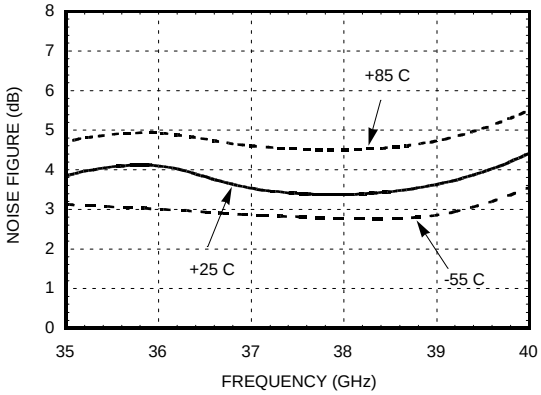
Input Match (S11)



Output Match (S22)

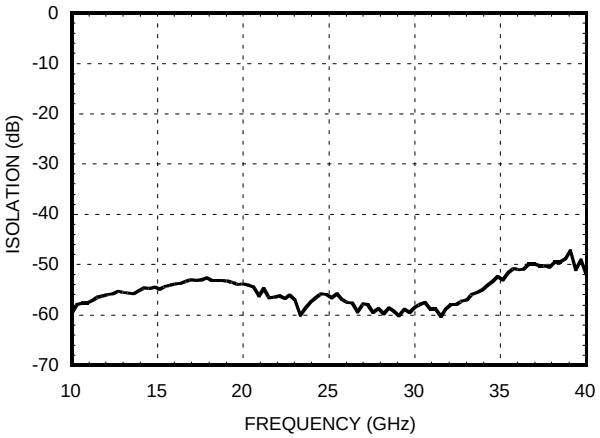


Noise Figure vs. Temperature

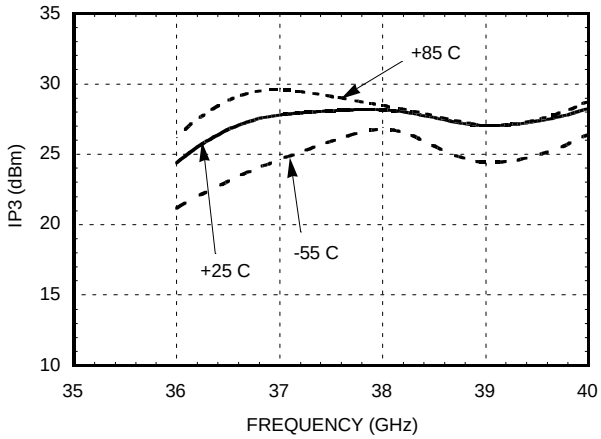


All data is with the chip in a 50 ohm test fixture connected via ribbon bonds of minimal length.

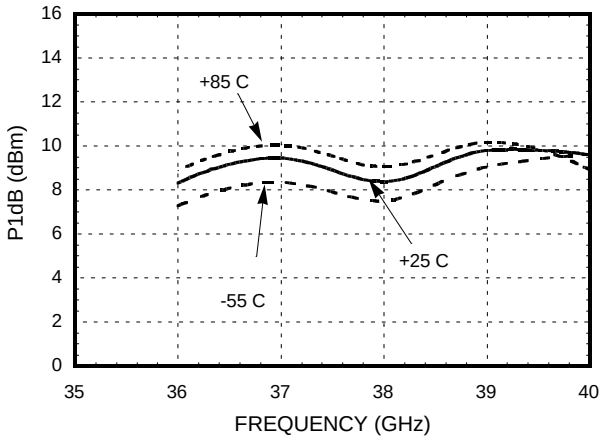
Isolation



IP3 Output @ Vdd = +3.5V



P1dB Output @ Vdd = +3.5V



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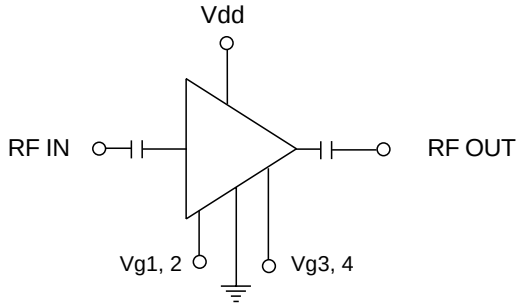
Schematic

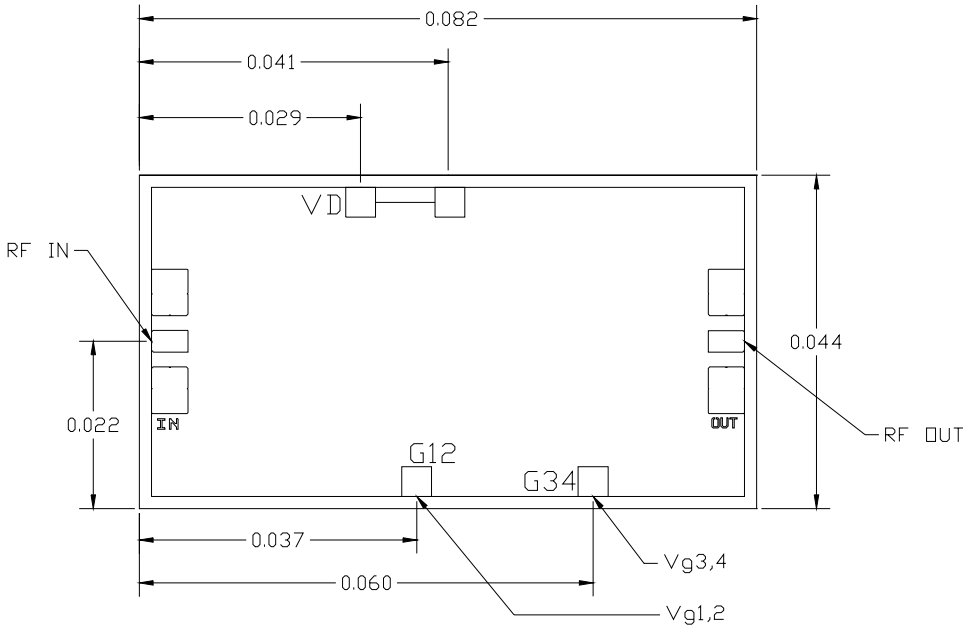


Backside is Ground

Absolute Maximum Ratings

Supply Voltage (Vdd)	+4 Vdc
Supply Current (Idd)	200 mA
Gate Bias Voltage (Vgg)	-2 to +0.4V
DC Gate Current (mA)	4 MA
Input Power (RFin)(Vdd=+3V)	+13 dBm
Channel Temperature (Tc)	175 °C
Thermal Resistance (⊖jc) (Channel Backside)	90 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-55 to +85 °C

Outline



ALL DIMENSION IN MILLIMETERS (INCHES)
ALL TOLERANCES ARE ±0.025 (0.001)
DIE THICKNESS IS 0.100 (0.004) BACKSIDE IS GROUND
BOND PADS ARE 0.100 (0.004) SQUARE
BACKSIDE METALLIZATION : GOLD
BOND PAD METALLIZATION : GOLD

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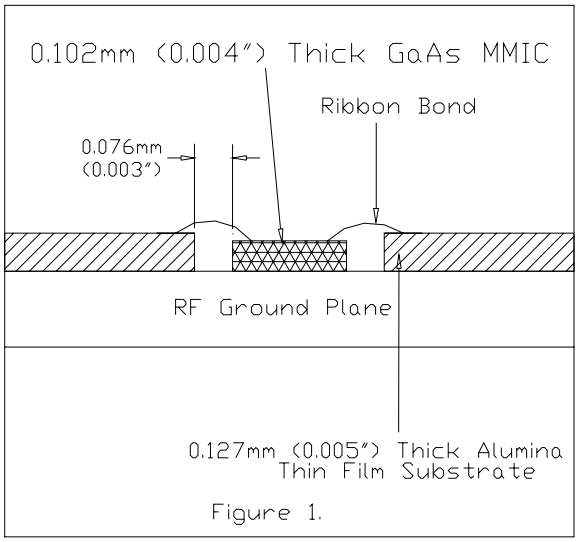

Figure 1.

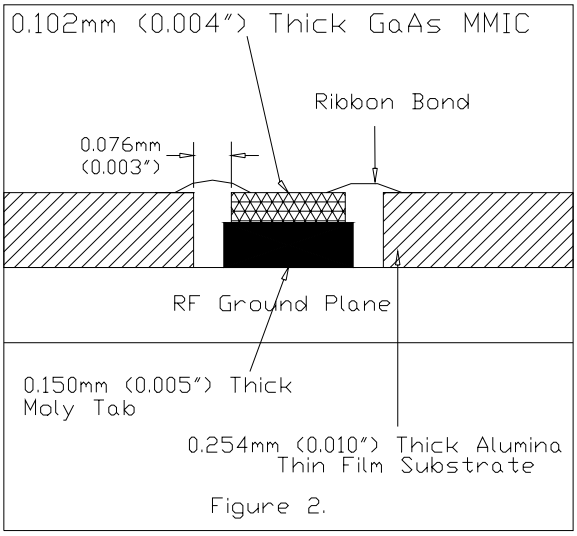

Figure 2.

Mounting & Bonding Techniques for Millimeterwave GaAs MMICs

The die should be attached directly to the ground plane eutectically or with conductive epoxy (see HMC general Handling, Mounting, Bonding Note).

50 Ohm Microstrip transmission lines on 0.127mm (5 mil) thick alumina thin film substrates are recommended for bringing RF to and from the chip (Figure 1). If 0.254mm (10 mil) thick alumina thin film substrates must be used, the die should be raised 0.150mm (6 mils) so that the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.102mm (4 mil) thick die to a 0.150mm (6 mil) thick molybdenum heat spreader (moly-tab) which is then attached to the ground plane (Figure 2).

Microstrip substrates should brought as close to the die as possible
in order to minimize bond length. Typical die-to-substrate spacing is 0.076mm (3 mils). Gold ribbon of 0.076 mm x 0.013 mm (3mil x 0.5 mil) is recommended to minimize inductance on the RF ports. 0.025 mm (1 mil) diameter ball or wedge bonds are acceptable for DC bias connections.

RF bypass capacitor should be used on the Vdd & Vgg inputs. 100 pF single layer capacitors (mounted eutectically or by conductive epoxy) placed no further than 0.762mm (30 Mils) from the chip are recommended.

Handling Precautions

Follow these precautions to avoid permanent damage.
Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.
Static Sensitivity: Follow ESD precautions to protect against ESD strikes (*see page 8 - 2*).
Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.
General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip has fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back-metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. The mounting surface should be clean and flat.

Eutectic Die Attach:
A 80/20 gold tin preform is recommended with a work surface temperature of 255 deg. C and a tool temperature of 265 deg. C. When hot 90/10 nitrogen/hydrogen gas is applied, tool tip temperature should be 290 deg. C.
DO NOT expose the chip to a temperature greater than 320 deg. C for more than 20 seconds. No more than 3 seconds of scrubbing should be required for attachment.

Epoxy Die Attach:
Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position.
Cure epoxy per the manufacturer's schedule.

Wire Bonding

Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire (DC bias) or ribbon bond (RF ports) with 0.076 mm x 0.013 mm (3 mil x 0.5 mil) size is recommended. Thermosonic wirebonding with a nominal stage temperature of 150 deg. C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31 mm (12 mils).