

### 262,144 WORD X 16 BIT DYNAMIC RAM

#### DESCRIPTION

The TC514260BJ/BFT is the new generation dynamic RAM organized 262,144 word by 16 bit. The TC514260BJ/BFT utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514273BJ to be packaged in a standard 40 pin plastic SOJ, and 44/40 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of  $5V \pm 10\%$  tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

#### FEATURES

- 262,144 word by 16 bit organization
- Fast access time and cycle time
- Single power supply of  $5V \pm 10\%$  with a built-in  $V_{BB}$  generator
- Low Power
  - 550mW MAX. Operating (TC514273BJ-70)
  - 468mW MAX. Operating (TC514273BJ-80)
  - 5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write,  $\overline{CAS}$  before  $\overline{RAS}$  refresh,  $\overline{RAS}$ -only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 512refresh cycles/8ms
- Package TC514260BJ : SOJ40-P-400  
TC514260BFT : TSOP44-P-400B

#### KEY PARAMETERS

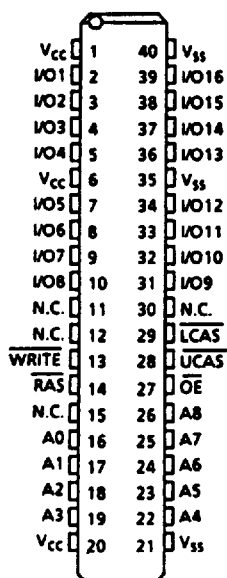
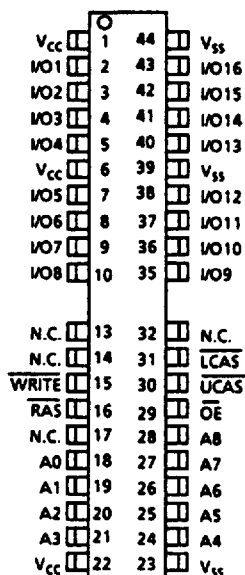
| ITEM                                   | TC514260BJ |       |
|----------------------------------------|------------|-------|
|                                        | -70        | -80   |
| $t_{RAC}$ $\overline{RAS}$ Access Time | 70ns       | 80ns  |
| $t_{AA}$ Column Address Access Time    | 35ns       | 40ns  |
| $t_{CAC}$ $\overline{CAS}$ Access Time | 20ns       | 20ns  |
| $t_{RC}$ Cycle Time                    | 130ns      | 150ns |
| $t_{PC}$ Fast Page Mode Cycle Time     | 45ns       | 50ns  |

## PIN NAME

|                 |                                          |
|-----------------|------------------------------------------|
| A0~A8           | Address Inputs                           |
| RAS             | Row Address Strobe                       |
| UCAS            | Column Address Strobe/Upper Byte Control |
| LCAS            | Column Address Strobe/Lower Byte Control |
| WRITE           | Read/Write Input                         |
| OE              | Output Enable                            |
| I/O1~I/O16      | Write Section/ Data Input/Output         |
| V <sub>CC</sub> | Power (+5V)                              |
| V <sub>SS</sub> | Ground                                   |
| N.C.            | No Connection                            |

## PIN CONNECTION (TOP VIEW)

Plastic SOJ

Plastic TSOP  
(Normal Bend Type)



**RECOMMENDED D.C. OPERATING CONDITION ( $T_a = 0\sim 70^\circ\text{C}$ )**

| SYMBOL   | PARAMETER          | MIN. | TYP | MAX          | UNIT | NOTE |
|----------|--------------------|------|-----|--------------|------|------|
| $V_{CC}$ | Supply Voltage     | 4.5  | 5.0 | 5.5          | V    | 2    |
| $V_{IH}$ | Input High Voltage | 2.4  | -   | $V_{CC}+0.5$ | V    | 2    |
| $V_{IL}$ | Input Low Voltage  | -0.5 | -   | 0.8          | V    | 2    |

\*-2.0V at pulse width  $\leq 20\text{ns}$ **D.C. OPERATING CHARACTERISTICS ( $V_{CC} = 5V \pm 10\%$ ,  $T_a = 0\sim 70^\circ\text{C}$ )**

| SYMBOL     | PARAMETER                                                                                                                                         | MIN.              | MAX | UNIT | NOTE          |
|------------|---------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|-----|------|---------------|
| $I_{CC1}$  | OPERATING CURRENT<br>Average Power Supply Operating Current (RAS, UCAS, LCAS, Address Cycling: $t_{RC}=t_{RC\text{ MIN.}}$ )                      | TC514260BJ/BFT-70 | -   | 100  | mA<br>3, 4, 5 |
|            |                                                                                                                                                   | TC514260BJ/BFT-80 | -   | 85   |               |
| $I_{CC2}$  | STANDBY CURRENT<br>Power Supply Standby Current<br>(RAS=UCAS=LCAS= $V_{IH}$ )                                                                     |                   | 2   | mA   |               |
| $I_{CC3}$  | RAS ONLY REFRESH CURRENT Average Power Supply Current, RAS Only Mode(RAS Cycling, UCAS=LCAS= $V_{IH}$ : $t_{RC}=t_{RC\text{ MIN.}}$ )             | TC514260BJ/BFT-70 | -   | 100  | mA<br>3, 5    |
|            |                                                                                                                                                   | TC514260BJ/BFT-80 | -   | 85   |               |
| $I_{CC4}$  | FAST PAGE MODE CURRENT<br>Average Power Supply Current, Fast Page Mode(RAS= $V_{IL}$ , UCAS, LCAS, Address Cycling: $t_{PC}=t_{PC\text{ MIN.}}$ ) | TC514260BJ/BFT-70 | -   | 70   | mA<br>3, 4, 5 |
|            |                                                                                                                                                   | TC514260BJ/BFT-80 | -   | 60   |               |
| $I_{CC5}$  | STANDBY CURRENT<br>Power Supply Standby Current<br>(RAS=UCAS=LCAS= $V_{CC}-0.2V$ )                                                                |                   | 1   | mA   |               |
| $I_{CC6}$  | CAS BEFORE RAS REFRESH CURRENT<br>Average Power Supply Current, CAS Before RAS Mode (RAS, UCAS, LCAS Cycling: $t_{RC}=t_{PC\text{ MIN.}}$ )       | TC514260BJ/BFT-70 | -   | 100  | mA<br>3, 5    |
|            |                                                                                                                                                   | TC514260BJ/BFT-80 | -   | 85   |               |
| $I_{I(L)}$ | INPUT LEAKAGE CURRENT<br>Input Leakage Current, any input<br>( $0V \leq V_{IN} \leq 6.5V$ , All Other Pins Not Under Test= $0V$ )                 |                   | -10 | 10   | $\mu A$       |
| $I_{O(L)}$ | OUTPUT LEAKAGE CURRENT<br>( $D_{OUT}$ is disabled, $0V \leq V_{OUT} \leq 5.5V$ )                                                                  |                   | -10 | 10   | $\mu A$       |
| $V_{OH}$   | OUTPUT CURRENT<br>Output "H" Level Voltage ( $I_{OUT}=-5\text{mA}$ )                                                                              |                   | 2.4 | -    | V             |
| $V_{OL}$   | OUTPUT CURRENT<br>Output "L" Level Voltage ( $I_{OUT}=4.2\text{mA}$ )                                                                             |                   | -   | 0.4  | V             |

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS ( $V_{CC} = 5V \pm 10\%$ ,  $T_a = 0\sim 70^\circ C$ )(Notes 6,7,8)**

| SYMBOL            | PARAMETER                                         | TC514260BJ/BFT |         |     |         | UNIT | NOTES   |
|-------------------|---------------------------------------------------|----------------|---------|-----|---------|------|---------|
|                   |                                                   | -70            |         | -80 |         |      |         |
|                   |                                                   | MIN            | MAX.    | MIN | MAX     |      |         |
| t <sub>RC</sub>   | Random Read or Write Cycle Time                   | 130            | -       | 150 | -       | ns   |         |
| t <sub>RMW</sub>  | Read-Modify-Write Cycle                           | 185            | -       | 205 | -       | ns   |         |
| t <sub>PC</sub>   | Fast Page Mode Cycle Time                         | 45             | -       | 50  | -       | ns   |         |
| t <sub>PRMW</sub> | Fast Page Mode Read-Modify-Write Cycle Time       | 100            | -       | 105 | -       | ns   |         |
| t <sub>RAC</sub>  | Access Time from RAS                              | -              | 70      | -   | 80      | ns   | 9,14,15 |
| t <sub>CAC</sub>  | Access Time from CAS                              | -              | 20      | -   | 20      | ns   | 9,14    |
| t <sub>AA</sub>   | Access Time from Column Address                   | -              | 35      | -   | 40      | ns   | 9,15    |
| t <sub>CPA</sub>  | Access Time from CAS Precharge                    | -              | 40      | -   | 45      | -    | 9       |
| t <sub>CLZ</sub>  | CAS to Output in Low-Z                            | 0              | -       | 0   | -       | ns   | 9       |
| t <sub>OFF</sub>  | Output Buffer Turn-off Delay                      | 0              | 15      | 0   | 15      | ns   | 10      |
| t <sub>T</sub>    | Transition Time (Rise and Fall)                   | 3              | 50      | 3   | 50      | ns   |         |
| t <sub>RP</sub>   | RAS Presharge Time                                | 50             | -       | 60  | -       | ns   |         |
| t <sub>RAS</sub>  | RAS Pulse Width                                   | 70             | 10,000  | 80  | 10,000  | ns   |         |
| t <sub>RASP</sub> | RAS Pulse Width (Fast Page Mode)                  | 70             | 100,000 | 80  | 100,000 | ns   |         |
| t <sub>RSH</sub>  | RAS Hold Time                                     | 20             | -       | 20  | -       | ns   |         |
| t <sub>RHCP</sub> | RAS Hold Time From CAS Precharge (Fast Page Mode) | 40             | -       | 45  | -       | ns   |         |
| t <sub>CSH</sub>  | CAS Hold Time                                     | 70             | -       | 80  | -       | ns   |         |
| t <sub>CAS</sub>  | CAS Pulse Width                                   | 20             | 10,000  | 20  | 10,000  | ns   |         |
| t <sub>RCD</sub>  | RAS to CAS Delay Time                             | 20             | 50      | 20  | 60      | ns   | 14      |
| t <sub>RAD</sub>  | RAS to Column Address Delay Time                  | 15             | 35      | 15  | 40      | ns   | 15      |
| t <sub>CRP</sub>  | CAS to RAS Precharge Time                         | 5              | -       | 5   |         | ns   |         |
| t <sub>CP</sub>   | CAS Precharge Time                                | 10             | -       | 10  | -       | ns   |         |
| t <sub>ASR</sub>  | Row Address Set-Up Time                           | 0              | -       | 0   | -       | ns   |         |
| t <sub>RAH</sub>  | Row Address Hold Time                             | 10             | -       | 10  | -       | ns   |         |
| t <sub>ASC</sub>  | Column Address Set-Up Time                        | 0              | -       | 0   | -       | ns   |         |
| t <sub>CAH</sub>  | Column Address Hold Time                          | 10             | -       | 15  | -       | ns   |         |
| t <sub>RAL</sub>  | Column Address To RAS Lead Time                   | 35             | -       | 40  | -       | ns   |         |
| t <sub>RCS</sub>  | Read Command Set-Up Time                          | 0              | -       | 0   | -       | ns   |         |
| t <sub>RCH</sub>  | Read Command Hold Time                            | 0              | -       | 0   | -       | ns   | 11      |
| t <sub>RRH</sub>  | Read Command Hold Time referenced to RAS          | 0              | -       | 0   | -       | ns   | 11      |
| t <sub>WCH</sub>  | Write Command Hold Time                           | 15             | -       | 15  | -       | ns   |         |

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C.  
OPERATING CONDITIONS (CONT)**

| SYMBOL            | PARAMETER                                              | TC514260BJ/BFT |     |     |     | UNIT | NOTES |
|-------------------|--------------------------------------------------------|----------------|-----|-----|-----|------|-------|
|                   |                                                        | -70            |     | -80 |     |      |       |
|                   |                                                        | MIN            | MAX | MIN | MAX |      |       |
| t <sub>WP</sub>   | Write Command Pulse Width                              | 15             | -   | 15  | -   | ns   |       |
| t <sub>RWL</sub>  | Write Command to RAS Lead Time                         | 20             | -   | 20  | -   | ns   |       |
| t <sub>CWL</sub>  | Write Command to CAS Lead Time                         | 20             | -   | 20  | -   | ns   |       |
| t <sub>DS</sub>   | Data Set-Up Time                                       | 0              | -   | 0   | -   | ns   | 12    |
| t <sub>DH</sub>   | Data Hold Time                                         | 15             | -   | 15  | -   | ns   | 12    |
| t <sub>REF</sub>  | Refresh Period                                         | -              | 8   | -   | 8   | ns   |       |
| t <sub>WCS</sub>  | Write Command Set-Up Time                              | 0              | -   | 0   | -   | ns   | 13    |
| t <sub>CWD</sub>  | CAS to WRITE Delay Time                                | 50             | -   | 50  | -   | ns   | 13    |
| t <sub>RWD</sub>  | RAS to WRITE Delay Time                                | 100            | -   | 110 | -   | ns   | 13    |
| t <sub>AWD</sub>  | Column Address to WE Delay Time                        | 65             | -   | 70  | -   | ns   | 13    |
| t <sub>CPWD</sub> | CAS Precharge to WRITE Delay Time                      | 70             | -   | 75  | -   | ns   | 13    |
| t <sub>CSR</sub>  | CAS Set-Up Time (CAS before RAS Cycle)                 | 5              | -   | 5   | -   | ns   |       |
| t <sub>CHR</sub>  | CAS Hold Time (CAS before RAS Cycle)                   | 15             | -   | 15  | -   | ns   |       |
| t <sub>RPC</sub>  | RAS to CAS Precharge Time                              | 5              | -   | 5   | -   | ns   |       |
| t <sub>CPT</sub>  | CAS Precharge Time (CAS before RAS Counter Test Cycle) | 30             | -   | 30  | -   | ns   |       |
| t <sub>ROH</sub>  | RAS Hold Time referenced to OE                         | 10             | -   | 10  |     | ns   |       |
| t <sub>OEA</sub>  | OE Access Time                                         | -              | 20  | 0   | 20  | ns   | 9     |
| t <sub>OED</sub>  | OE to Data Delay                                       | 20             | -   | 20  | -   | ns   |       |
| t <sub>OEZ</sub>  | Output buffer turn off Delay Time from OE              | 0              | 20  | 0   | 20  | ns   | 10    |
| t <sub>OEH</sub>  | OE Command Hold Time                                   | 20             | -   | 20  | -   | ns   |       |
| t <sub>ODS</sub>  | Output Disable Set-Up Time                             | 0              | -   | 0   | -   | ns   |       |

**CAPACITANCE ( $V_{CC} = 5V \pm 10\%$ ,  $f = 1MHz$ ,  $T_a = 0 \sim 70^\circ C$ )**

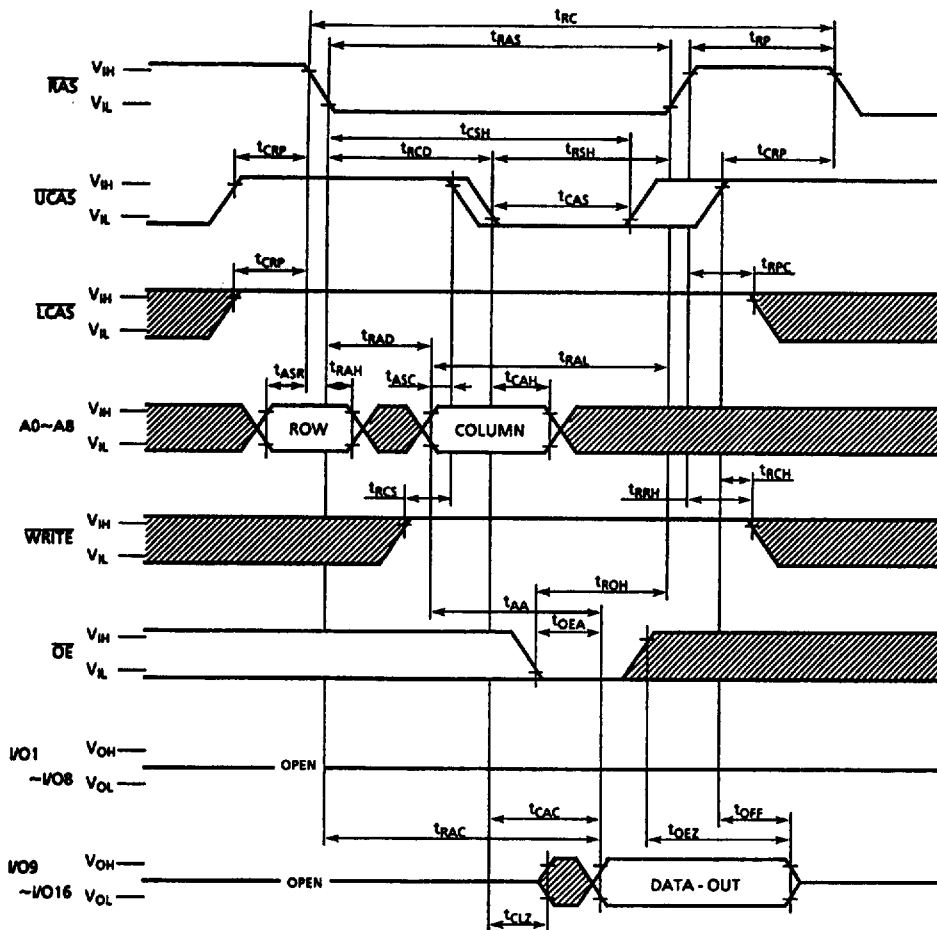
| SYMBOL   | PARAMETER                                | MIN | MAX | UNIT |
|----------|------------------------------------------|-----|-----|------|
| $C_{I1}$ | Input Capacitance (A0~A8)                | -   | 5   | pF   |
| $C_{I2}$ | Input Capacitance (RAS, UCAS, LCAS, OE)) | -   | 7   | pF   |
| $C_O$    | Input Capacitance(I/O1~I/O16)            | -   | 7   | pF   |

## NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to  $V_{SS}$ .
3.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ ,  $I_{CC6}$  depend on cycle rate.
4.  $I_{CC1}$ ,  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
5. Address can be changed one or less while  $\overline{RAS}=V_{IL}$ . In case of  $I_{CC4}$ , it can be changed once or less during a fast page mode cycle ( $t_{PC}$ ).
6. An initial pause of 200 $\mu$ s is required after power-up followed by 8  $\overline{RAS}$  only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{CAS}$  before  $\overline{RAS}$  refresh cycles instead of 8  $\overline{RAS}$  only refresh cycles are required.
7. AC measurements assume  $t_f=5$ ns.
8.  $V_{IH}$  (min.) and  $V_{IL}$  (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10.  $t_{OFF}$  (max.) and  $t_{OEZ}$  (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
12. These parameters are referenced to  $\overline{UCAS}$ ,  $\overline{LCAS}$  leading edge in early write cycles and to  $\overline{WRITE}$ , leading edge in Read-Modify-Write cycles.
13.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$ ,  $t_{AWD} \geq t_{AWD}(\text{min.})$  and  $t_{CPWD} \geq t_{CPWD}(\text{min.})$ , (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell; If neither of the above sets of condition is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the  $t_{RCD}(\text{max.})$  limit insures that  $t_{RAC}$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$ .
15. Operation within the  $t_{RAD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only: If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled by  $t_{AA}$ .



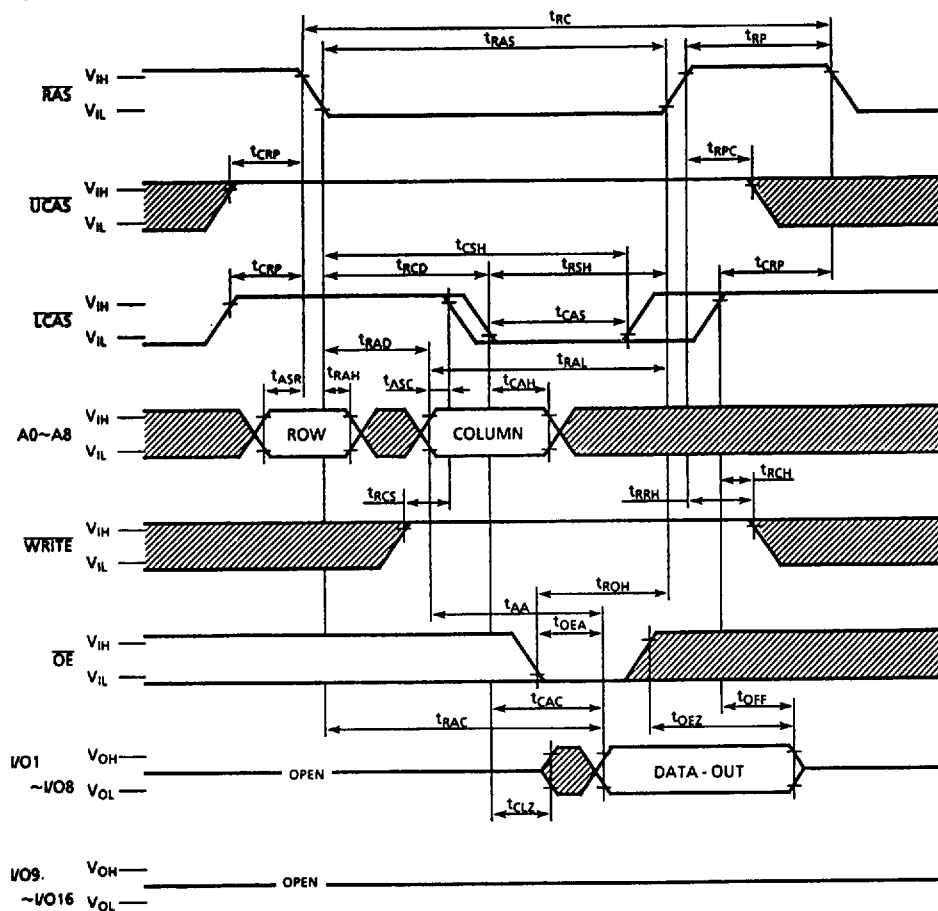
## UPPER BYTE READ CYCLE



Note:  $D_{IN}$  (I/O1~I/O8) = Don't Care  
 $D_{IN}$  (I/O9~I/O16) = OPEN

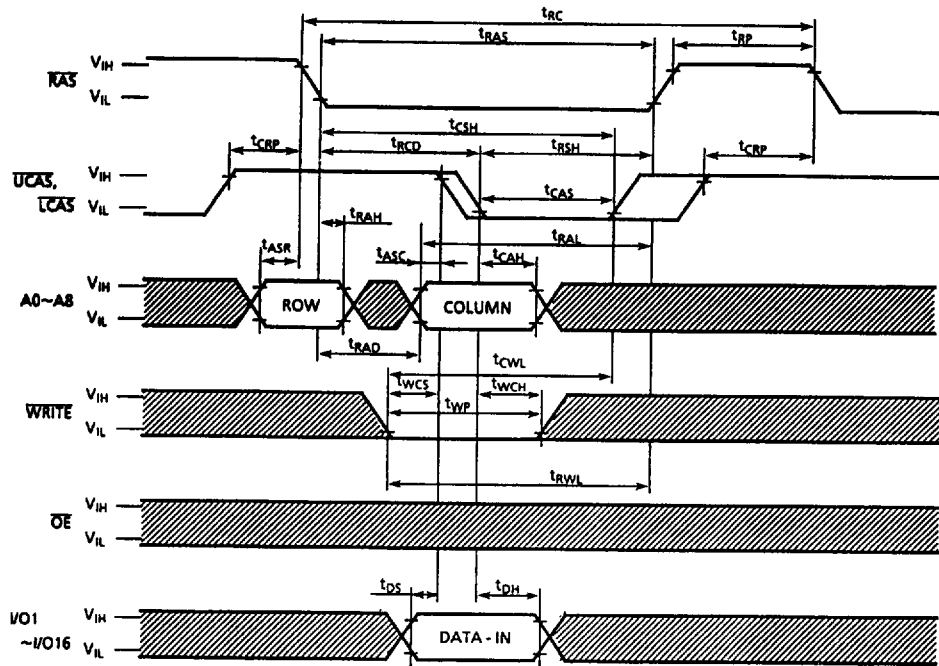
■ : "H" or "L"

# LOWER BYTE READ CYCLE



Note:  $D_{IN}(I/O1 \sim I/O8) = \text{OPEN}$   
 $D_{IN}(I/O9 \sim I/O16) = \text{Don't Care}$

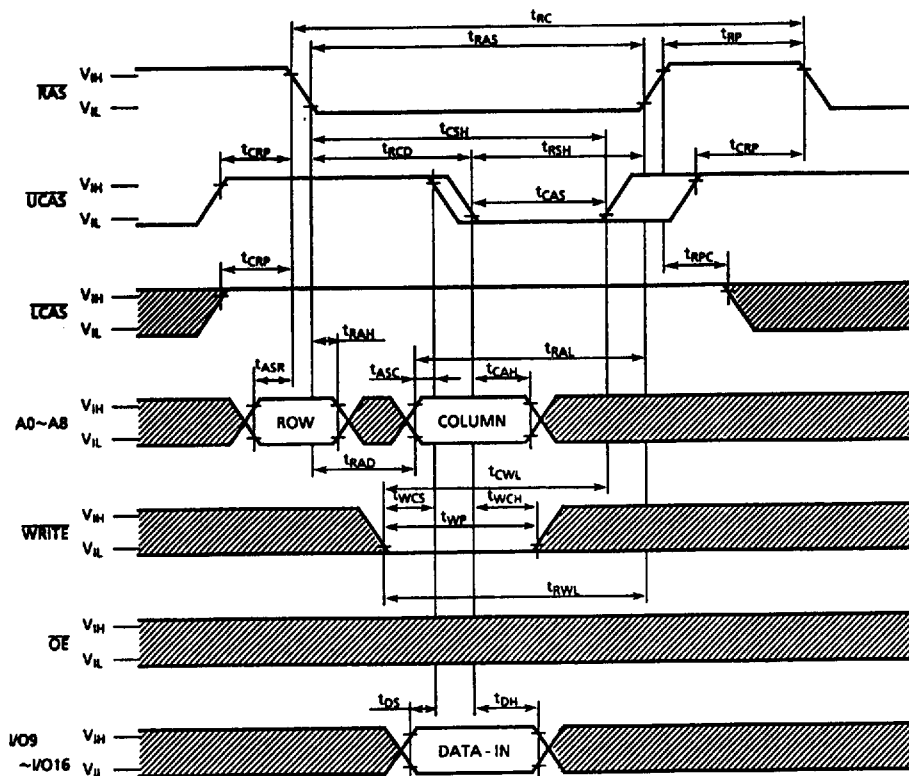
## WRITE CYCLE (EARLY WRITE)



■ : "H" or "L"

Note:  $D_{OUT}$  = OPEN

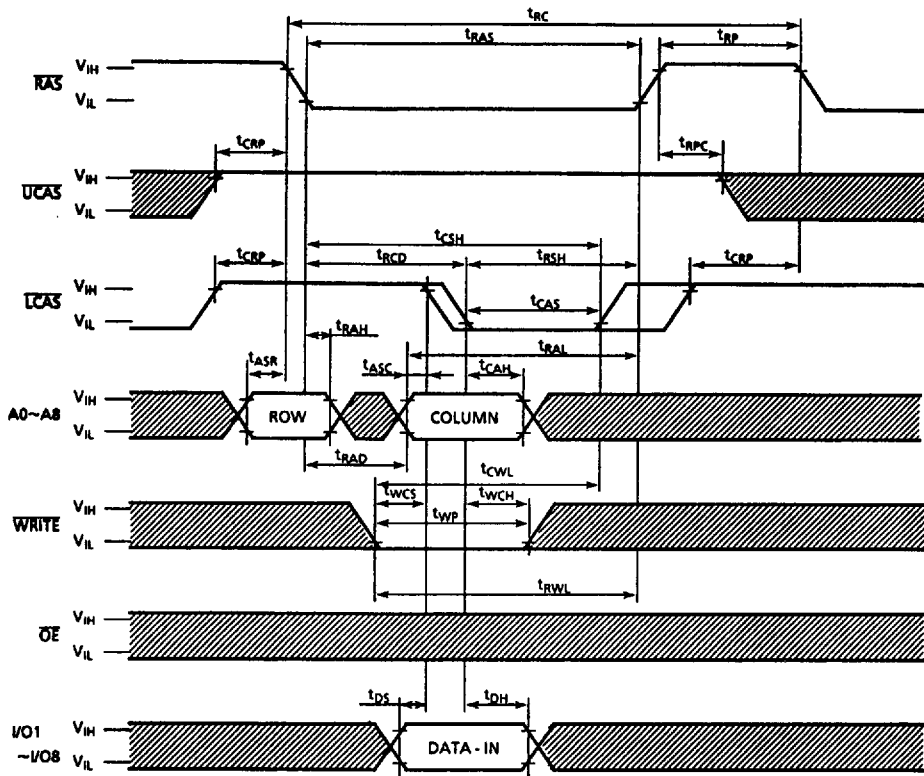
## UPPER BYTE WRITE CYCLE (EARLY WRITE)



■ : "H" or "L"

Note:  $D_{IN}$  (I/O1~I/O8) = Don't Care  
 $D_{OUT}$  = OPEN

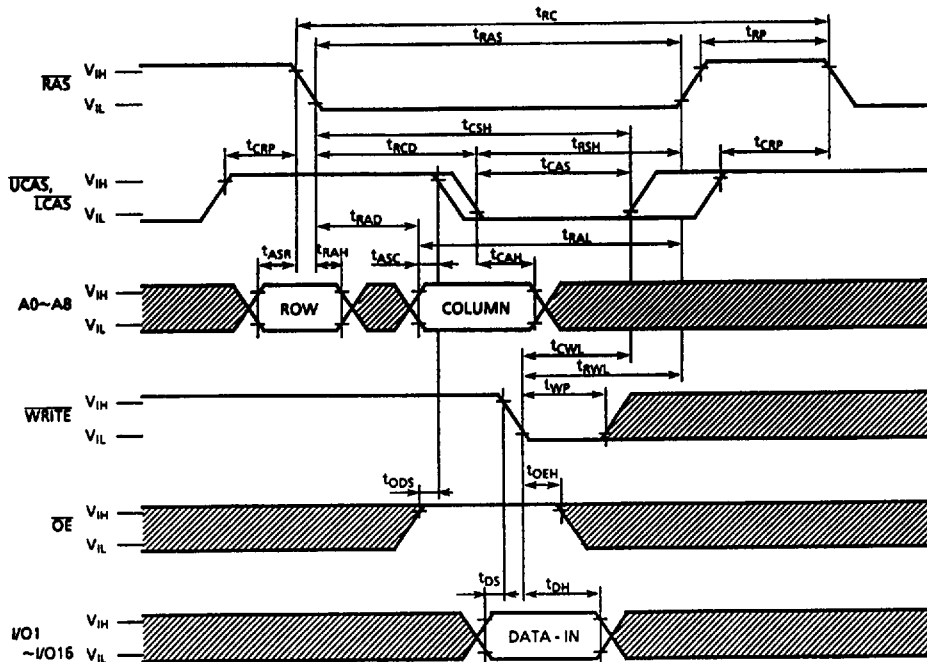
## LOWER BYTE WRITE CYCLE (EARLY WRITE)



■ : "H" or "L"

Note:  $D_{IN}$  (I/O9~I/O16) = Don't Care  
 $D_{OUT}$  = OPEN

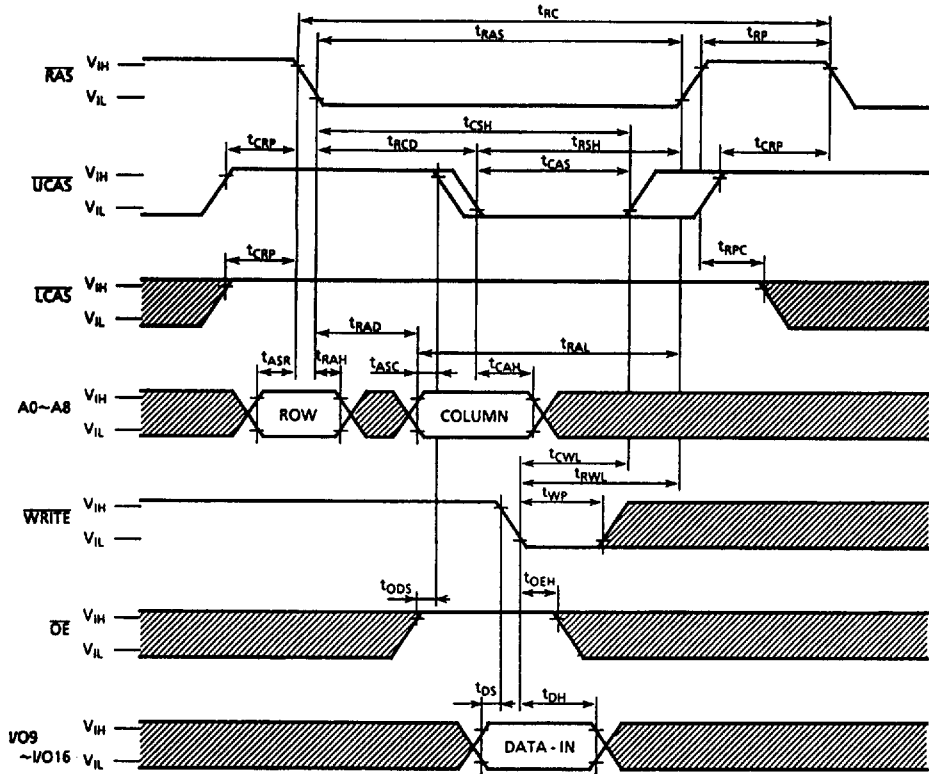
# WRITE CYCLE (OE CONTROLLED WRITE)



Note: D<sub>OUT</sub> = OPEN

■ : "H" or "L"

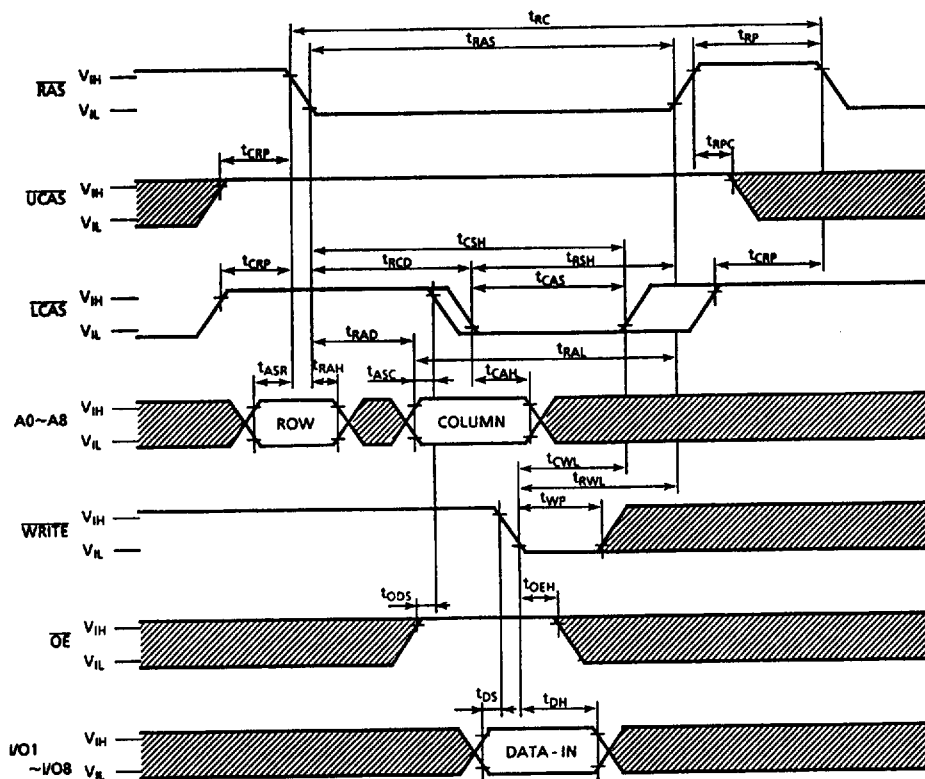
## UPPER BYTE WRITE CYCLE (OE CONTROLLED WRITE)



Note:  $D_{IN}$  (I/O1~I/O8) = Don't Care  
 $D_{OUT}$  = OPEN

▨ : "H" or "L"

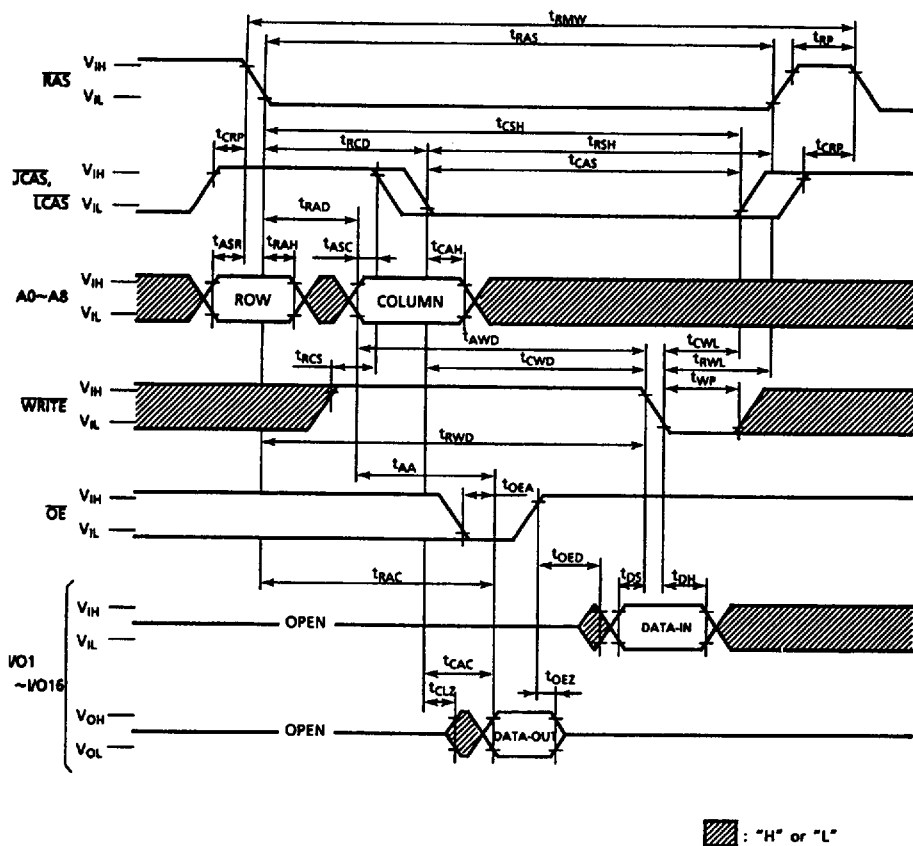
# LOWER BYTE WRITE CYCLE (OE CONTROLLED WRITE)



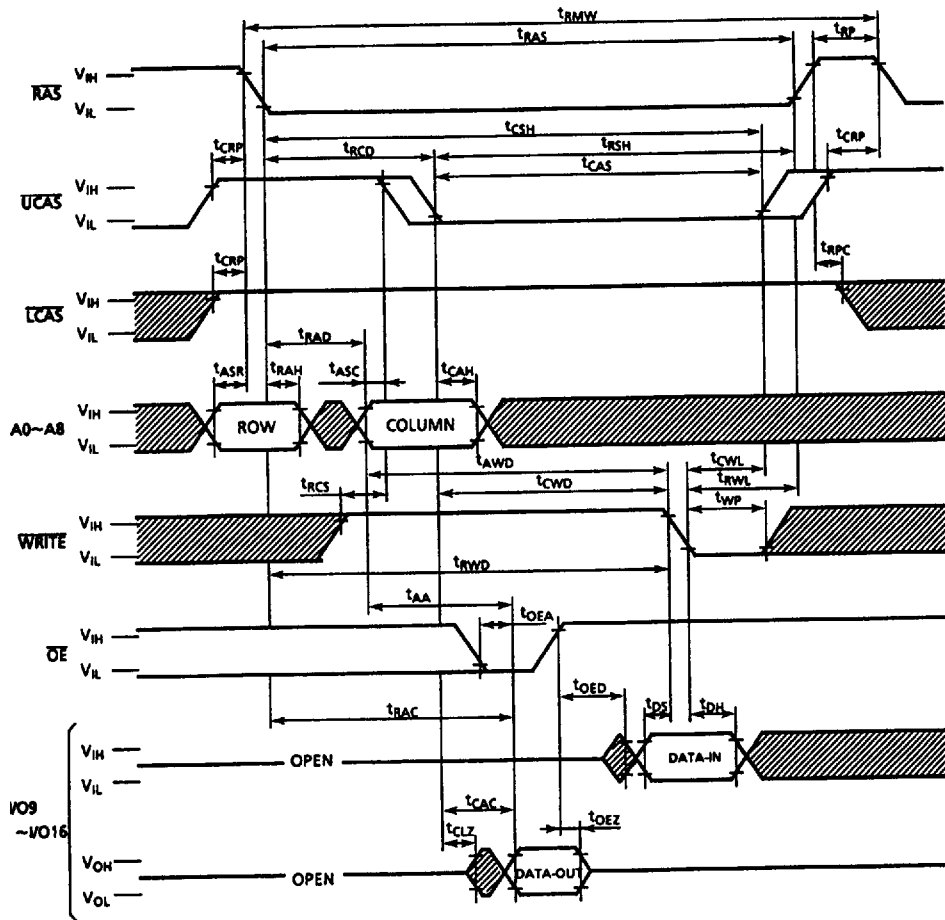
Note:  $D_{IN}$  (I/O9~I/O16) = Don't Care  
 $D_{OUT}$  = OPEN

■ : "H" or "L"

## READ-MODIFY-WRITE CYCLE



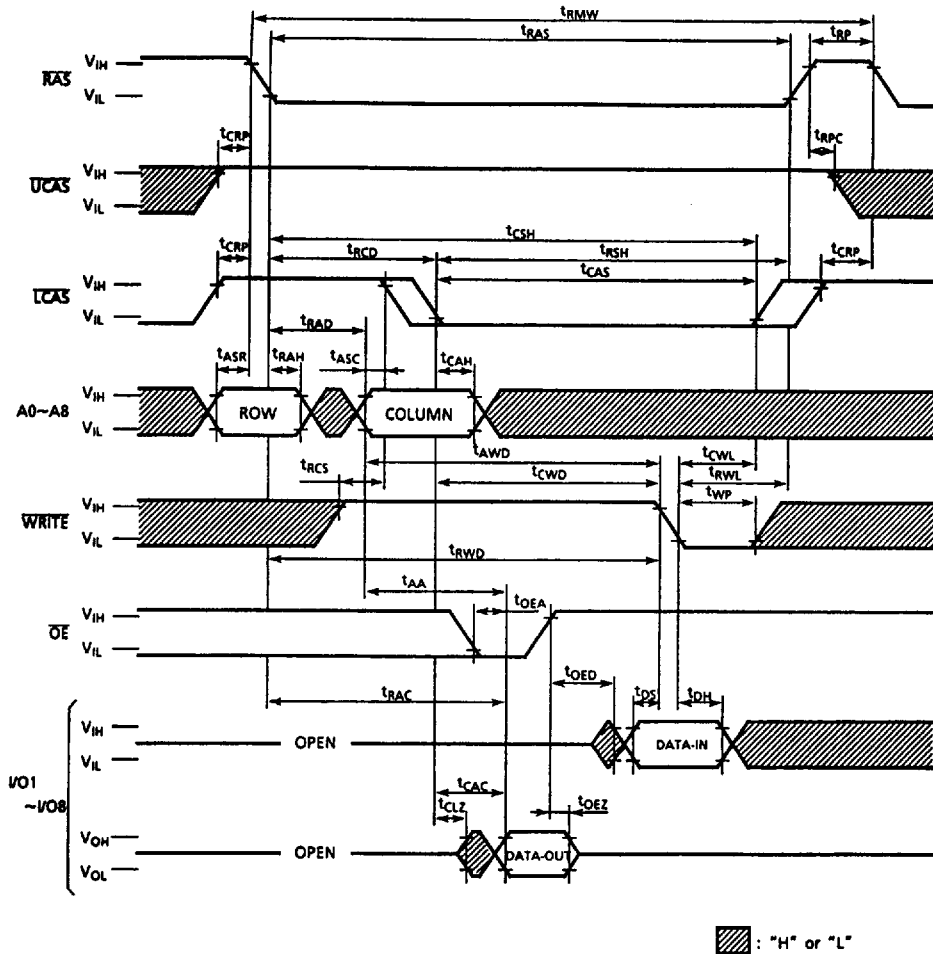
# UPPER BYTE READ-MODIFY-WRITE CYCLE



■ : "H" or "L"

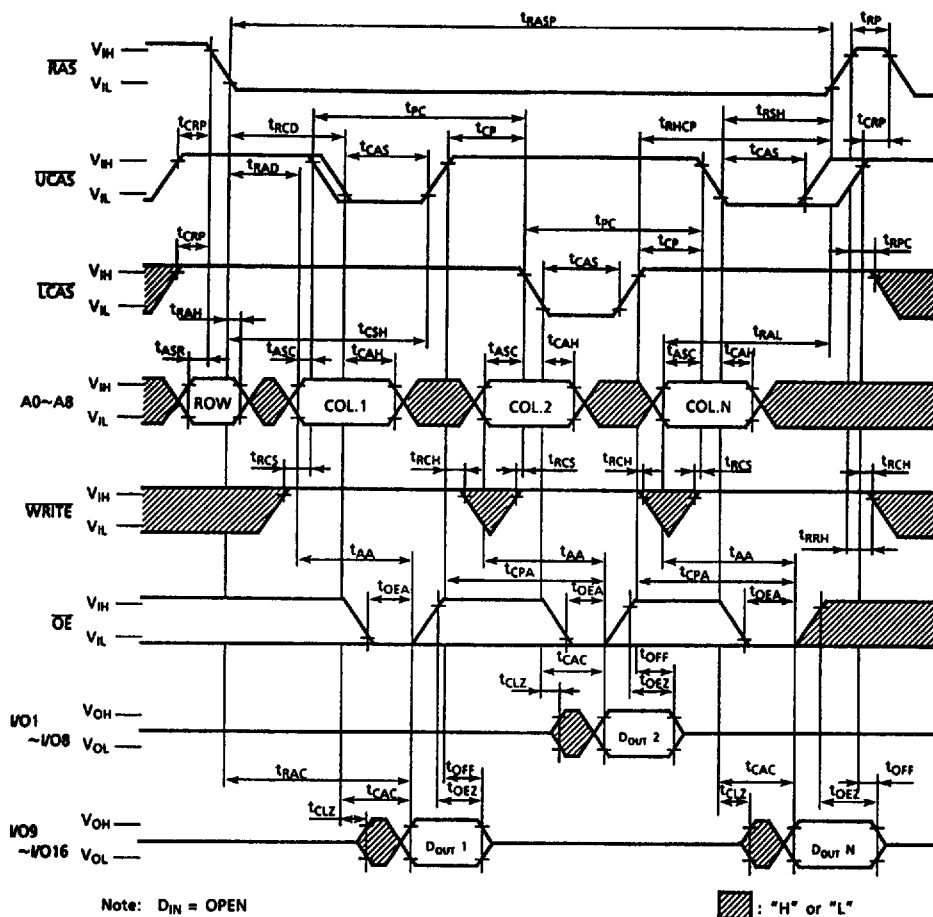
Note:  $D_{IN}(I/O1 \sim I/O8)$  = Don't Care  
 $D_{OUT}(I/O1 \sim I/O8)$  = OPEN

## LOWER BYTE READ-MODIFY-WRITE CYCLE





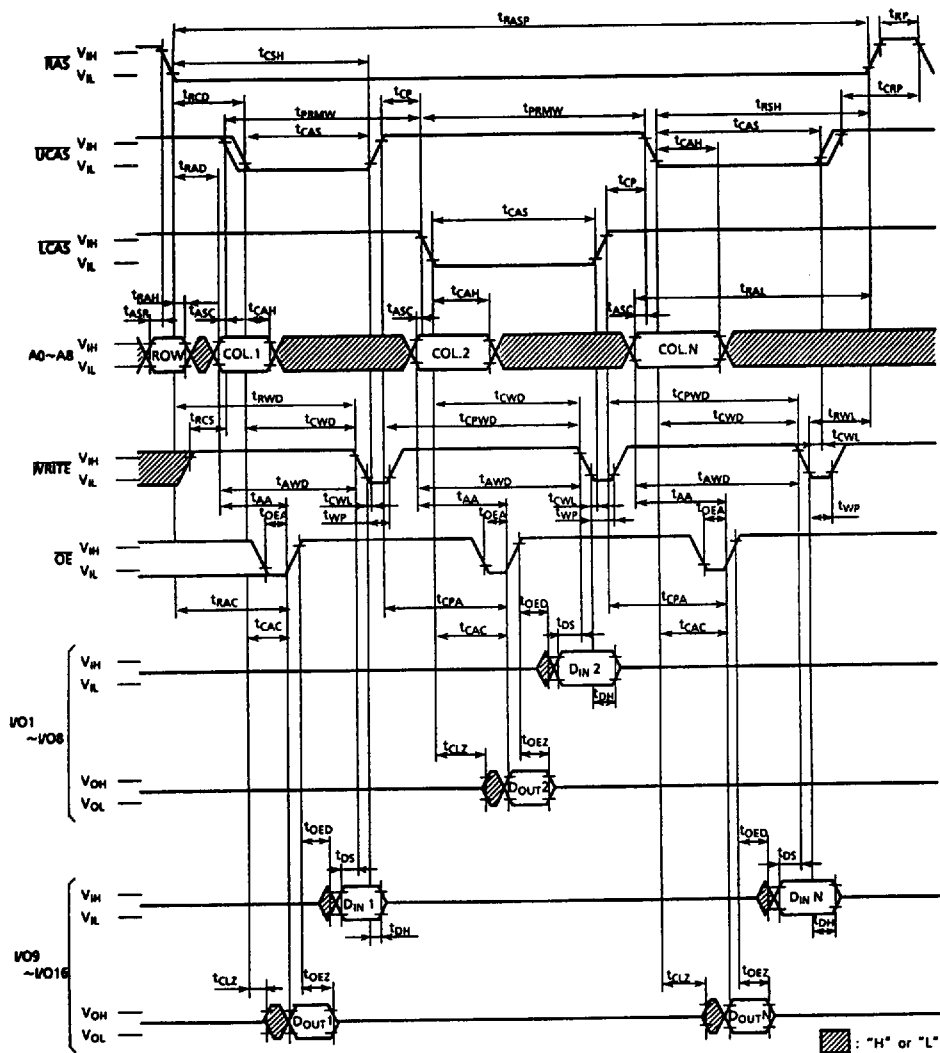
### FAST PAGE MODE BYTE READ CYCLE



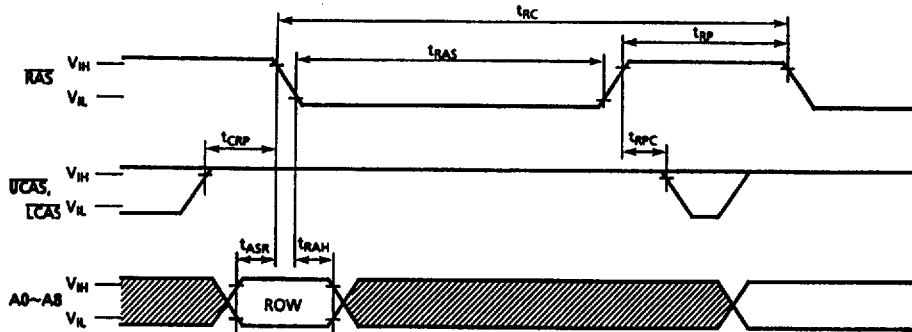




# FAST PAGE MODE BYTE READ-MODIFY-WRITE CYCLE



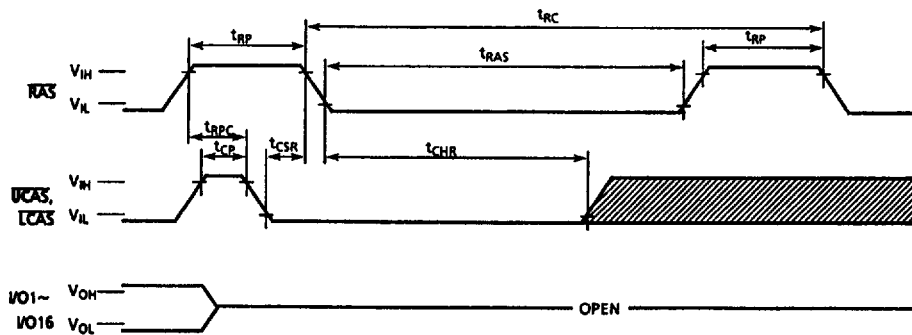
## RAS ONLY REFRESH CYCLE



Note: WRITE, OE = "H" or "L"  
 DIN = Don't Care  
 DOUT = OPEN

▨ : "H" or "L"

## CAS BEFORE RAS REFRESH CYCLE

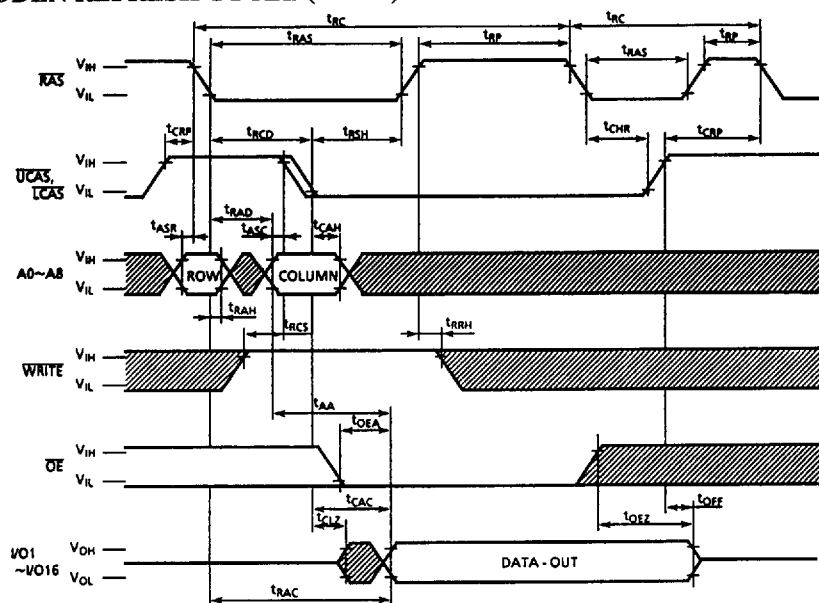


Note: WRITE, OE, A0~A8 = "H" or "L"  
 DIN = Don't Care

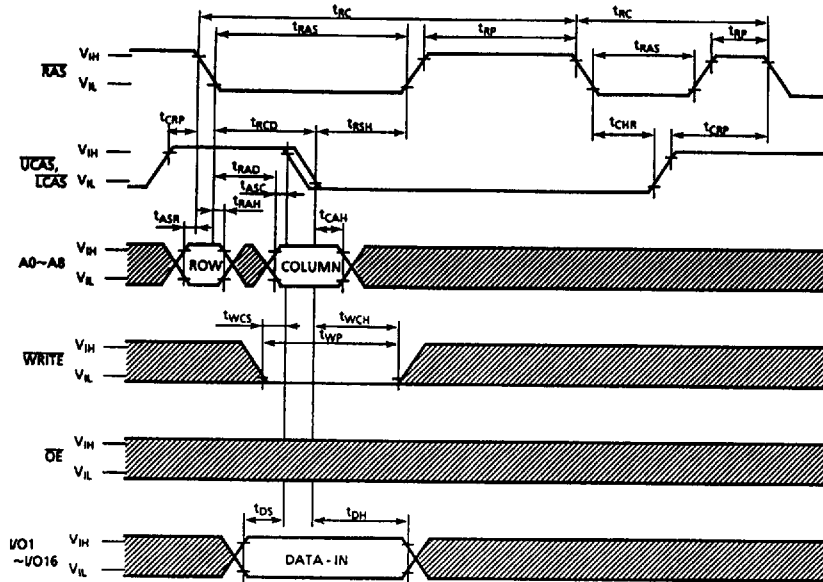
CAS before RAS refresh is performed when either UCAS or LCAS meets this timing.

▨ : "H" or "L"

## HIDDEN REFRESH CYCLE (READ)

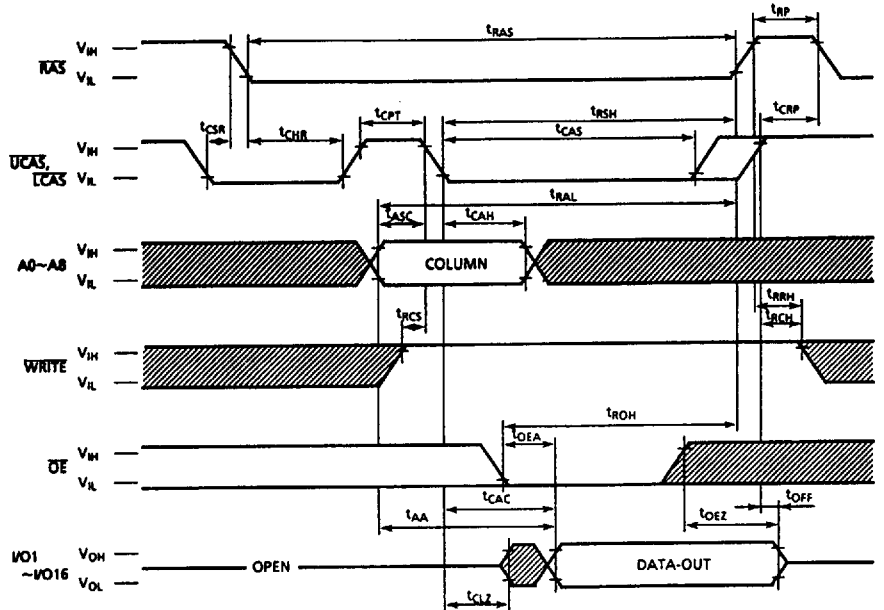
Note:  $D_{IN} = \text{OPEN}$ 

: "H" or "L"

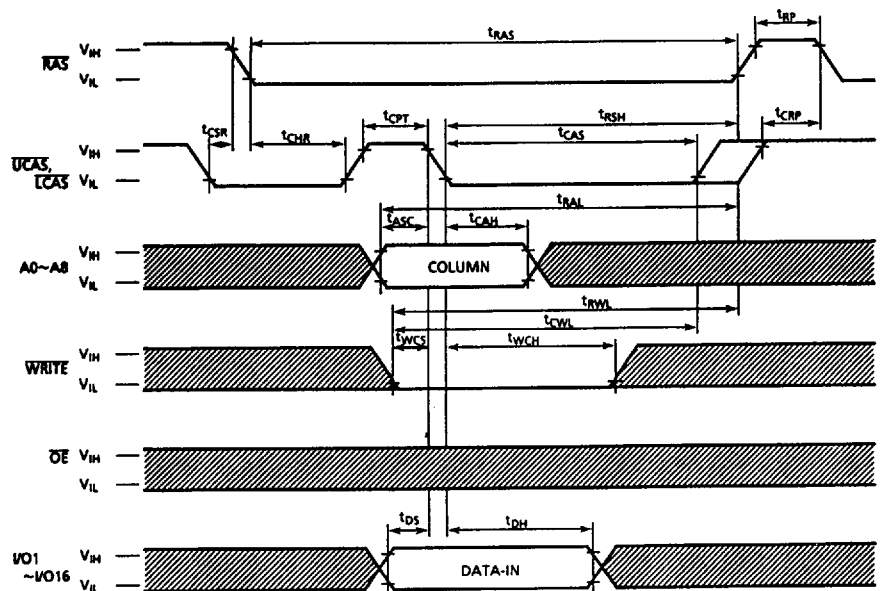
**HIDDEN REFRESH CYCLE (WRITE)**Note:  $D_{OUT} = OPEN$ 

: "H" or "L"

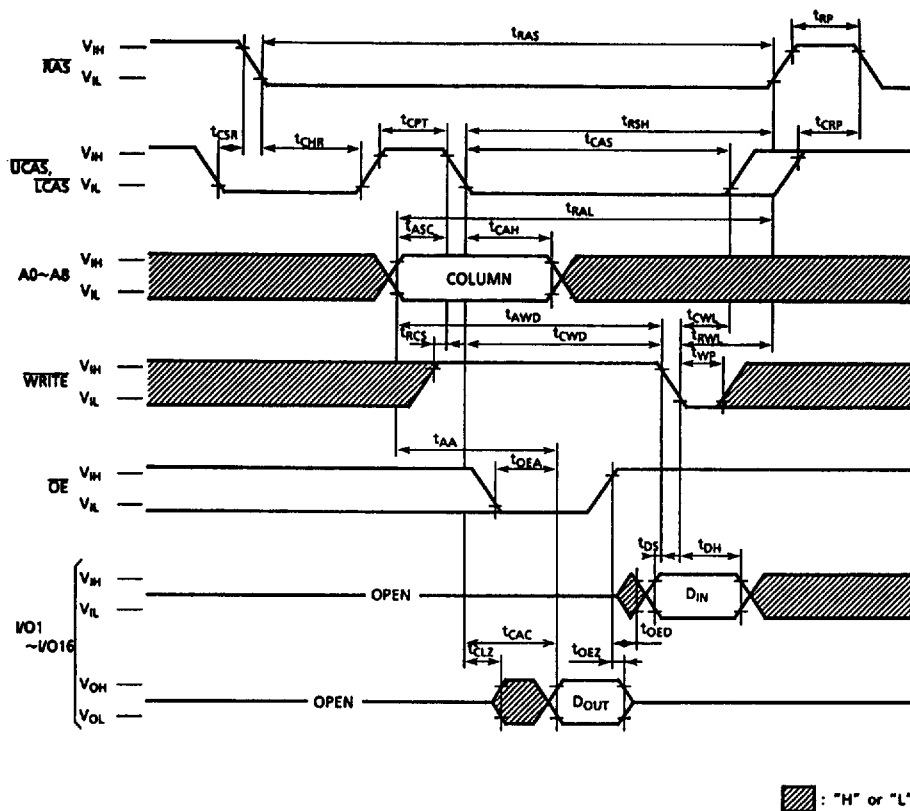
## CAS BEFORE RAS REFRESH COUNTER TEST READ CYCLE



## CAS BEFORE RAS REFRESH COUNTER TEST WRITE CYCLE



## CAS BEFORE RAS REFRESH COUNTER TEST READ-MODIFY-WRITE CYCLE



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