

# COMPOUND FIELD EFFECT POWER TRANSISTOR

# $\mu$ PA1560

### N-CHANNEL POWER MOS FET ARRAY

### SWITCHING

### INDUSTRIAL USE

#### DESCRIPTION

The  $\mu$ PA1560 is N-Channel Power MOS FET Array that built in 4 circuits designed for solenoid, motor and lamp driver.

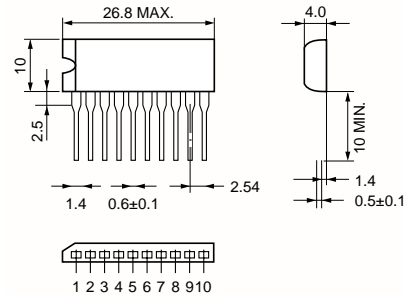
#### FEATURES

- Full mold package with 4 circuits
- 4 V driving is possible
- Low on-state resistance  
 $R_{DS(on)1} = 165 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 1.5 \text{ A)}$   
 $R_{DS(on)2} = 200 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4 \text{ V, } I_D = 1.5 \text{ A)}$
- Low input capacitance  
 $C_{iss} = 600 \text{ pF TYP.}$

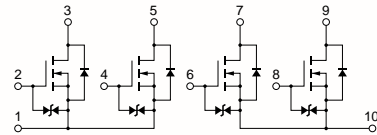
#### ORDERING INFORMATION

| PART NUMBER   | PACKAGE    |
|---------------|------------|
| $\mu$ PA1560H | 10-pin SIP |

#### PACKAGE DRAWING (Unit : mm)



#### EQUIVALENT CIRCUIT



ELECTRODE CONNECTION  
 2, 4, 6, 8 : Gate  
 3, 5, 7, 9 : Drain  
 1, 10 : Source

#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

|  |                |              |                  |
|--|----------------|--------------|------------------|
| Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )   | $V_{DSS}$      | 120          | V                |
| Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )    | $V_{GSS(AC)}$  | $\pm 20$     | V                |
| Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )    | $V_{GSS(DC)}$  | + 20, -10    | V                |
| Drain Current (DC)                                   | $I_{D(DC)}$    | $\pm 3.0$    | A                |
| Drain Current (pulse) <sup>Note1</sup>               | $I_{D(pulse)}$ | $\pm 12$     | A                |
| Total Power Dissipation ( $T_C = 25^\circ\text{C}$ ) | $P_{T1}$       | 28           | W                |
| Total Power Dissipation ( $T_A = 25^\circ\text{C}$ ) | $P_{T2}$       | 3.7          | W                |
| Channel Temperature                                  | $T_{ch}$       | 150          | $^\circ\text{C}$ |
| Storage Temperature                                  | $T_{stg}$      | -55 to + 150 | $^\circ\text{C}$ |
| Single Avalanche Current <sup>Note2</sup>            | $I_{AS}$       | 3.0          | A                |
| Single Avalanche Energy <sup>Note2</sup>             | $E_{AS}$       | 0.9          | mJ               |

**Notes 1.**  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1 \%$

**2.** Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = 60 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

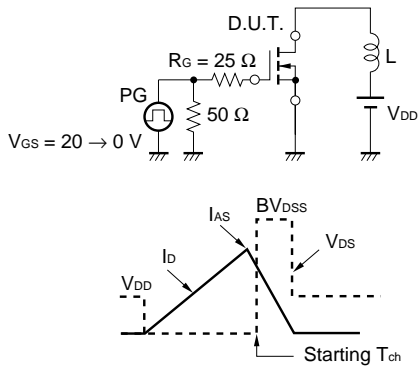
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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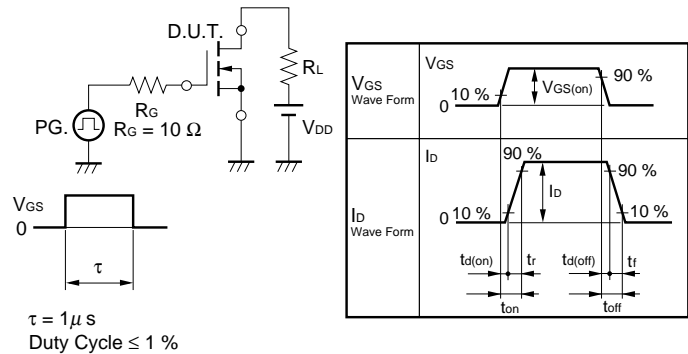
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

| CHARACTERISTICS                     | SYMBOL               | TEST CONDITIONS                                 | MIN. | TYP. | MAX. | UNIT |
|-------------------------------------|----------------------|---|------|------|------|------|
| Drain to Source On-state Resistance | R <sub>DS(on)1</sub> | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.5 A  |      | 130  | 165  | mΩ   |
|                                     | R <sub>DS(on)2</sub> | V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 1.5 A |      | 145  | 200  | mΩ   |
| Gate to Source Cut-off Voltage      | V <sub>GS(off)</sub> | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1.0 mA | 1.0  | 1.8  | 2.5  | V    |
| Forward Transfer Admittance         | y <sub>fs</sub>      | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1.5 A  | 2    | 4.5  |      | S    |
| Drain Leakage Current               | I <sub>DSS</sub>     | V <sub>DS</sub> = 120 V, V <sub>GS</sub> = 0 V  |      |      | 10   | μA   |
| Gate to Source Leakage Current      | I <sub>GSS</sub>     | V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V  |      |      | ±10  | μA   |
| Input Capacitance                   | C <sub>iss</sub>     | V <sub>DS</sub> = 10 V                          |      | 600  |      | pF   |
| Output Capacitance                  | C <sub>oss</sub>     | V <sub>GS</sub> = 0 V                           |      | 160  |      | pF   |
| Reverse Transfer Capacitance        | C <sub>rss</sub>     | f = 1.0 MHz                                     |      | 70   |      | pF   |
| Turn-on Delay Time                  | t <sub>d(on)</sub>   | I <sub>D</sub> = 1.5 A                          |      | 35   |      | ns   |
| Rise Time                           | t <sub>r</sub>       | V <sub>GS(on)</sub> = 10 V                      |      | 80   |      | ns   |
| Turn-off Delay Time                 | t <sub>d(off)</sub>  | V <sub>DD</sub> = 60 V                          |      | 700  |      | ns   |
| Fall Time                           | t <sub>f</sub>       | R <sub>L</sub> = 30 Ω                           |      | 250  |      | ns   |
| Total Gate Charge                   | Q <sub>G</sub>       | I <sub>D</sub> = 3.0 A                          |      | 28   |      | nC   |
| Gate to Source Charge               | Q <sub>GS</sub>      | V <sub>DD</sub> = 96 V                          |      | 2.5  |      | nC   |
| Gate to Drain Charge                | Q <sub>GD</sub>      | V <sub>GS</sub> = 10 V                          |      | 9    |      | nC   |
| Body Diode Forward Voltage          | V <sub>F(S-D)</sub>  | I <sub>F</sub> = 3.0 A, V <sub>GS</sub> = 0 V   |      | 0.9  |      | V    |
| Reverse Recovery Time               | t <sub>rr</sub>      | I <sub>F</sub> = 3.0 A, V <sub>GS</sub> = 0 V   |      | 160  |      | ns   |
| Reverse Recovery Charge             | Q <sub>rr</sub>      | di/dt = 50 A/μs                                 |      | 280  |      | nC   |

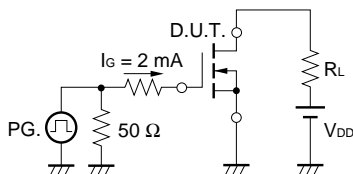
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**



**TEST CIRCUIT 3 GATE CHARGE**



[MEMO]

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