Ordering number : EN5950

CMOS IC

LC75754M

1/3 Duty VFD Driver

Overview

The LC75754M is a 1/3 duty VFD driver that can be used for electronic tuning frequency display and other applications under the control of a microcontroller. This product can directly drive VFDs with up to 72 segments.

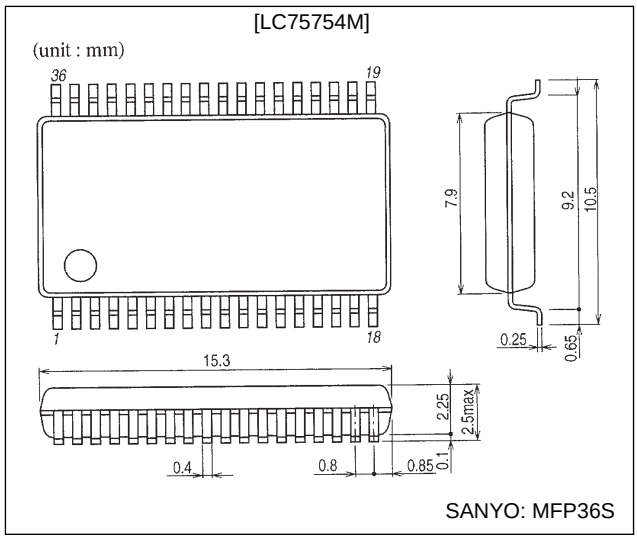
Features

- 72 segment outputs.
- Noise reduction circuits are built into the output drivers.
- Serial data input supports CCB format communication with the system controller.
- Dimmer can be controlled by serial data input.
- High generality since display data is displayed without the intervention of a decoder.
- All segments can be turned off with the $\overline{\text{BLK}}$ pin.

Package Dimensions

unit: mm

3129-MFP36S



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	–0.3 to +6.5	V
	V_{FL} max	V_{FL}	–0.3 to +21.0	V
Input voltage	$V_{IN}1$	DI, CL, CE, $\overline{\text{BLK}}$	–0.3 to +6.5	V
	$V_{IN}2$	OSCI	–0.3 to V_{DD} +0.3	V
Output voltage	$V_{OUT}1$	S1 to S24, G1 to G3	–0.3 to V_{FL} +0.3	V
	$V_{OUT}2$	OSCO	–0.3 to V_{DD} +0.3	V
Output current	$I_{OUT}1$	S1 to S24	6	mA
	$I_{OUT}2$	G1 to G3	60	mA
Allowable power dissipation	Pd max	Ta = 85°C	300	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–50 to +150	°C

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

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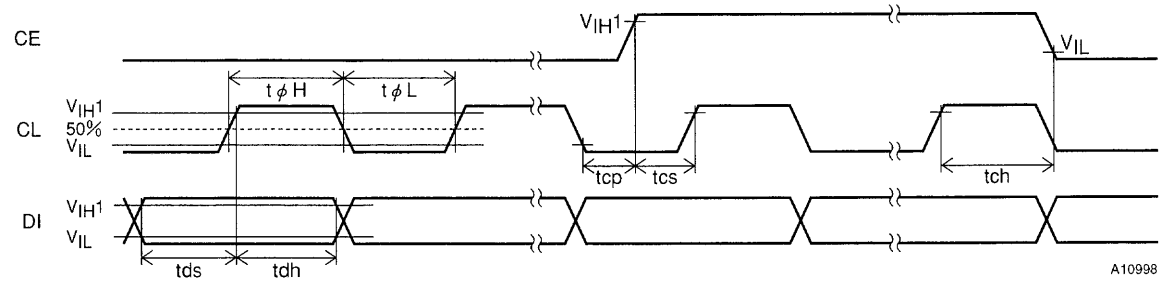
Allowable Operating Ranges at Ta = –40 to +85°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	4.5	5.0	5.5	V
	V_{FL}	V_{FL}	8	12	18	V
Input high-level voltage	$V_{IH}1$	DI, CL, CE, $\overline{BLK}$	0.8 V_{DD}		5.5	V
	$V_{IH}2$	OSCI	0.8 V_{DD}		V_{DD}	V
Input low-level voltage	V_{IL}	DI, CL, CE, $\overline{BLK}$, OSCI	0		0.2 V_{DD}	V
Guaranteed oscillator range	f_{OSC}	OSCI, OSCO	0.9	2.4	3.7	MHz
Recommended external resistance	R_{OSC}	OSCI, OSCO	2.2	12	47	KΩ
Recommended external capacitance	C_{OSC}	OSCI, OSCO	15	33	100	pF
Low level clock pulse width	$t_{øL}$	CL : Figure 1	160			ns
High level clock pulse width	$t_{øH}$	CL : Figure 1	160			ns
Data setup time	t_{ds}	DI, CL : Figure 1	160			ns
Data hold time	t_{dh}	DI, CL : Figure 1	160			ns
CE wait time	t_{cp}	CE, CL : Figure 1	160			ns
CE setup time	t_{cs}	CE, CL : Figure 1	160			ns
CE hold time	t_{ch}	CE, CL : Figure 1	160			ns
$\overline{BLK}$ switching time	t_c	$\overline{BLK}$, CE : Figure 3	10			µs

Electrical Characteristics in the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level current	$I_{IH}1$	DI, CL, CE, $\overline{BLK}$: V_{IN} = 5.5V			5	µA
	$I_{IH}2$	OSCI : V_{IN} = V_{DD}			5	µA
Input low-level current	I_{IL}	DI, CL, CE, $\overline{BLK}$, OSCI : V_{IN} = 0 V	–5			µA
Output high-level voltage	$V_{OH}1$	S1 to S24 : I_O = –2 mA	V_{FL} – 0.6			V
	$V_{OH}2$	G1 to G3 : I_O = –50 mA	V_{FL} – 1.3			V
	$V_{OH}3$	OSCO : I_O = –0.5 mA	V_{DD} – 2.0			V
Output low-level voltage	$V_{OL}1$	S1 to S24, G1 to G3 : I_O = 50 µA			0.5	V
	$V_{OL}2$	OSCO : I_O = 0.5 mA			2.0	V
Oscillator frequency	f_{OSC}	R_{OSC} = 12kΩ, C_{OSC} = 33 pF		2.4		MHz
Hysteresis voltage	V_H	DI, CL, CE, $\overline{BLK}$		0.1 V_{DD}		V
Current drain	I_{DD}	Output open : f_{OSC} = 2.4MHz			10	mA

- When CL is stopped at the low level



- When CL is stopped at the high level

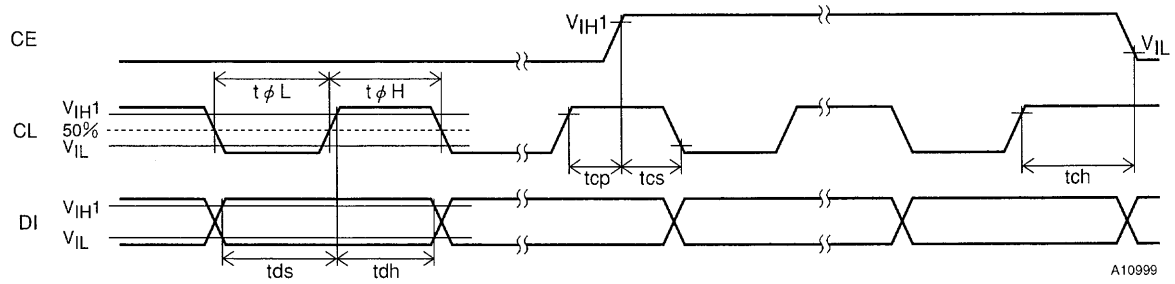
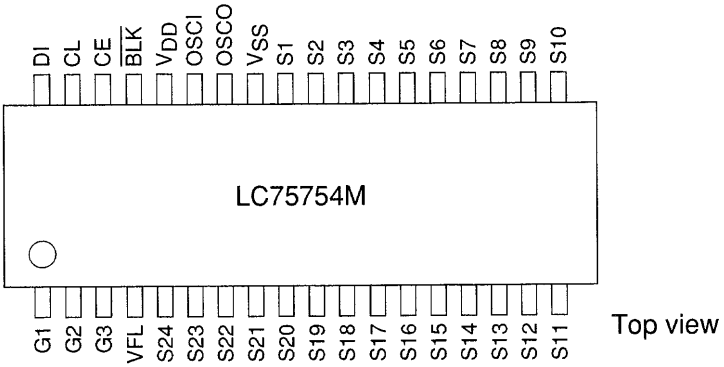
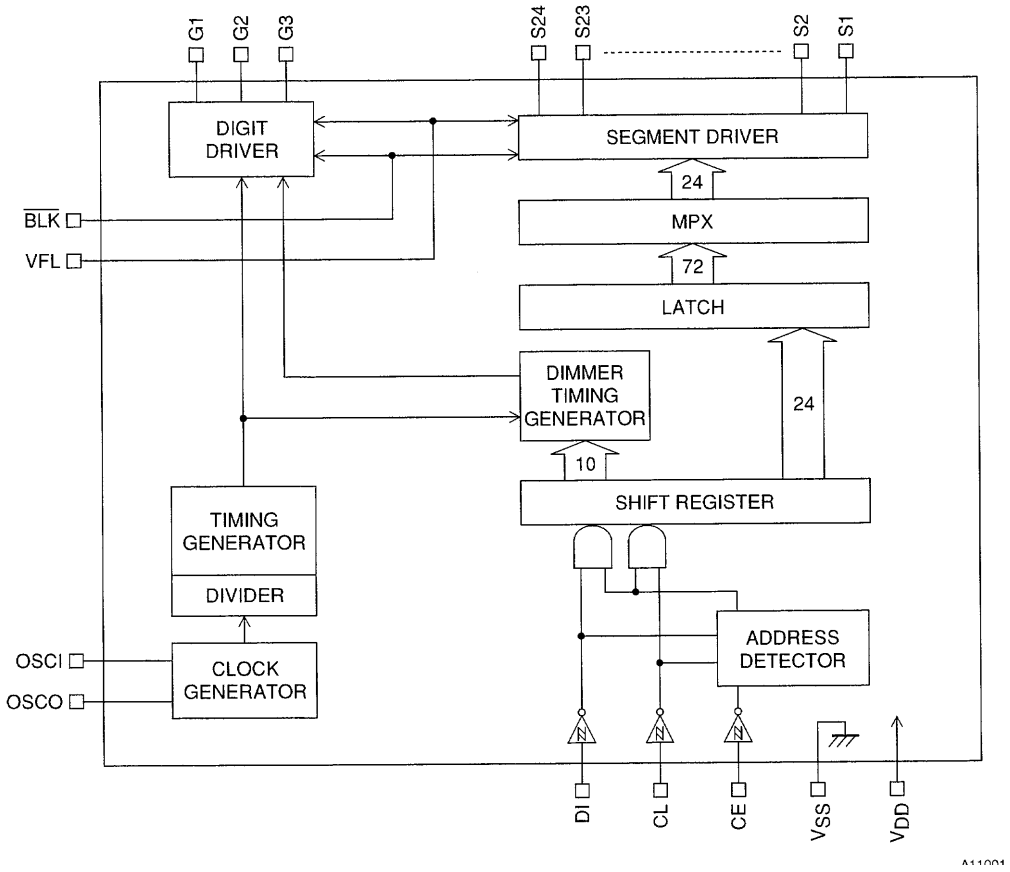


Figure 1

Pin Assignment



Block Diagram

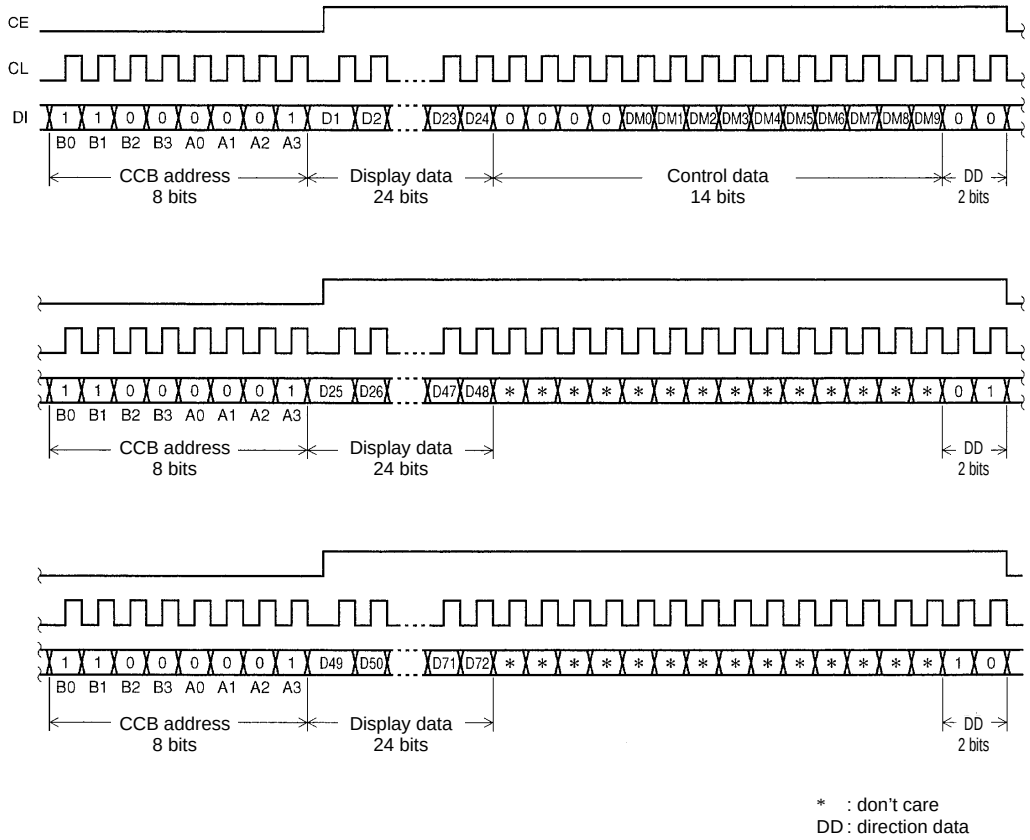


Pin Functions

Pin No.	Pin	Function	I/O	Handling when unused
4	V_{FL}	Driver block power supply. A voltage of between 8.0 and 18.0 V must be supplied.	—	—
32	V_{DD}	Logic block power supply. A voltage of between 4.5 and 5.5 V must be supplied.	—	—
29	V_{SS}	Power supply. Must be connected to the system ground.	—	—
31	OSCI	Oscillator connection. An oscillator circuit is formed by connecting an external resistor and	I	GND
30	OSCO	capacitor to these pins.	O	OPEN
33	$\overline{BLK}$	Display off control input. $\overline{BLK}$ = L (V_{SS}) .....Display off (S1 to S24, G1 to G3 = L) $\overline{BLK}$ = H (V_{DD}) .....Display on Note that serial data can be transferred while the display is turned off.	I	GND
35	CL	Serial data transfer inputs. These pins must be connected to the system microcontroller. CL : Synchronization clock DI : Transfer data CE : Chip enable	I	GND
36	DI			
34	CE			
1 to 3	G1 to G3	Digit outputs. The frame frequency fo is (f_{OSC}/6144)Hz.	O	OPEN
28 to 5	S1 to S24	Segment outputs for displaying the display data transferred by serial data input	O	OPEN

Serial Data Transfer Format

• When CL is stopped at the low level



• When CL is stopped at the high level

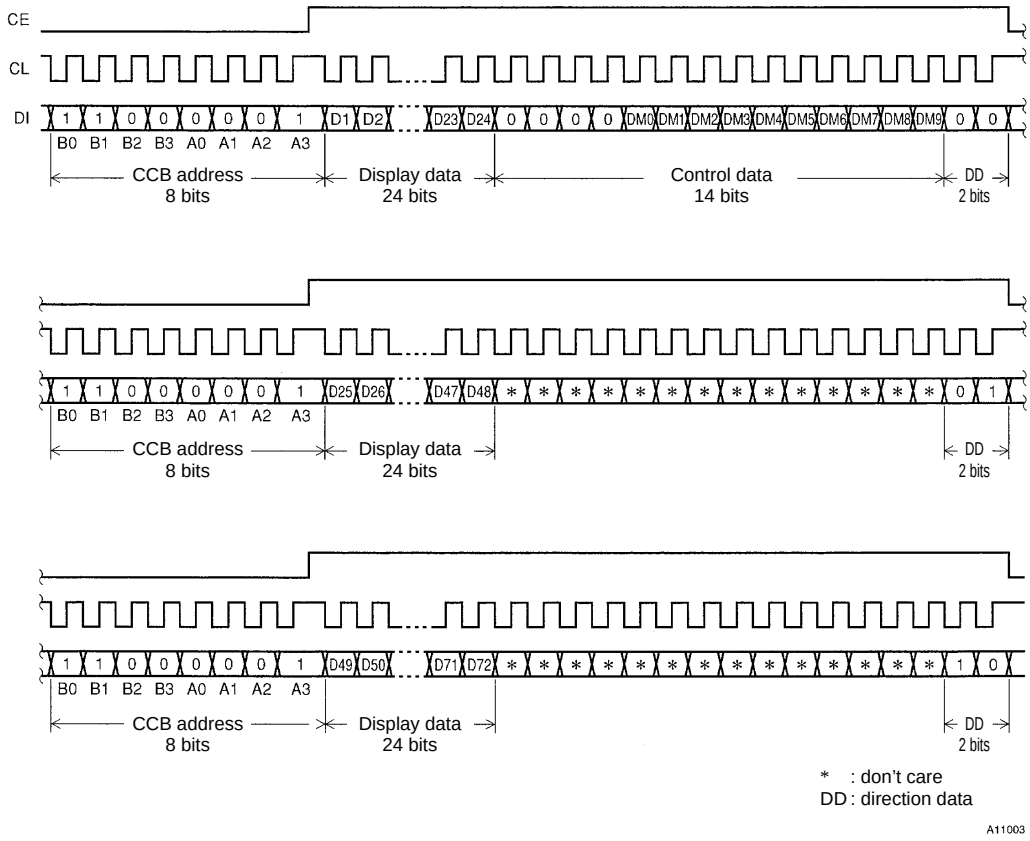


Figure 2

CCB address : Transfer 11000001B(83_H) as shown in Figure 2

DM0 to DM9 : Dimmer data

This data controls the duty of the G1 to G3 digit output pins, and consists of 10 bits with DM0 being the LSB. Note that the intensity of the display can be adjusted by controlling the duty of the G1 to G3 digit output pins.

The relationship between the dimmer data and the dimmer value is as follows.

DM9	DM8	DM7	DM6	DM5	DM4	DM3	DM2	DM1	DM0	Dimmer value (t4/t3)
0	0	0	0	0	0	0	0	0	0	0/1024
0	0	0	0	0	0	0	0	0	1	1/1024
0	0	0	0	0	0	0	0	1	0	2/1024
⋮										⋮
1	1	1	1	1	1	1	1	0	0	1020/1024
1	1	1	1	1	1	1	1	0	1	1021/1024
1	1	1	1	1	1	1	1	1	0	1022/1024
1	1	1	1	1	1	1	1	1	1	Not used

t3, t4 : See Figure 4.

D1 to D24 : Display data for the G1 digit output pin.

Dn (n = 1 to 24) = 1 : On

Dn (n = 1 to 24) = 0 : Off

D25 to D48 : Display data for the G2 digit output pin.

Dn (n = 25 to 48) = 1 : On

Dn (n = 25 to 48) = 0 : Off

D49 to D72 : Display data for the G3 digit output pin.

Dn (n = 49 to 72) = 1 : On

Dn (n = 49 to 72) = 0 : Off

Correspondence between Display Data (D1 to D72) and Segment Output Pins

Segment output pins	G1	G2	G3
S1	D1	D25	D49
S2	D2	D26	D50
S3	D3	D27	D51
S4	D4	D28	D52
S5	D5	D29	D53
S6	D6	D30	D54
S7	D7	D31	D55
S8	D8	D32	D56
S9	D9	D33	D57
S10	D10	D34	D58
S11	D11	D35	D59
S12	D12	D36	D60

Segment output pins	G1	G2	G3
S13	D13	D37	D61
S14	D14	D38	D62
S15	D15	D39	D63
S16	D16	D40	D64
S17	D17	D41	D65
S18	D18	D42	D66
S19	D19	D43	D67
S20	D20	D44	D68
S21	D21	D45	D69
S22	D22	D46	D70
S23	D23	D47	D71
S24	D24	D48	D72

Example : Segment output pin S11 is controlled as follows :

Display data			Segment output pin S11 state
D11	D35	D59	
0	0	0	The segments corresponding to the G1, G2, and G3 digit output pins are off
0	0	1	The segments corresponding to the G3 digit output pin are on
0	1	0	The segments corresponding to the G2 digit output pin are on
0	1	1	The segments corresponding to the G2 and G3 digit output pins are on
1	0	0	The segments corresponding to the G1 digit output pin are on
1	0	1	The segments corresponding to the G1 and G3 digit output pins are on
1	1	0	The segments corresponding to the G1 and G2 digit output pins are on
1	1	1	The segments corresponding to the G1, G2, and G3 digit output pins are on

$\overline{\text{BLK}}$ and the Display Control

Since the IC internal data (D1 to D72 and the control data) is undefined when power is first applied, the display is off (S1 to S24, G1 to G3 = low) by setting the $\overline{\text{BLK}}$ pin low at the same time as power is applied. Then, meaningless display at power on can be prevented by transferring all 144 bits of serial data from the controller and setting $\overline{\text{BLK}}$ pin high after the transfer completes while the display is off. (See figure 3.)

Power Supply Sequence

The following sequences must be observed when power is turned on and off. (See Figure 3.)

- Power on : Logic block power supply (V_{DD}) on $\rightarrow$ Driver block power supply (V_{FL}) on
- Power off : Driver block power supply (V_{FL}) off $\rightarrow$ Logic block power supply (V_{DD}) off

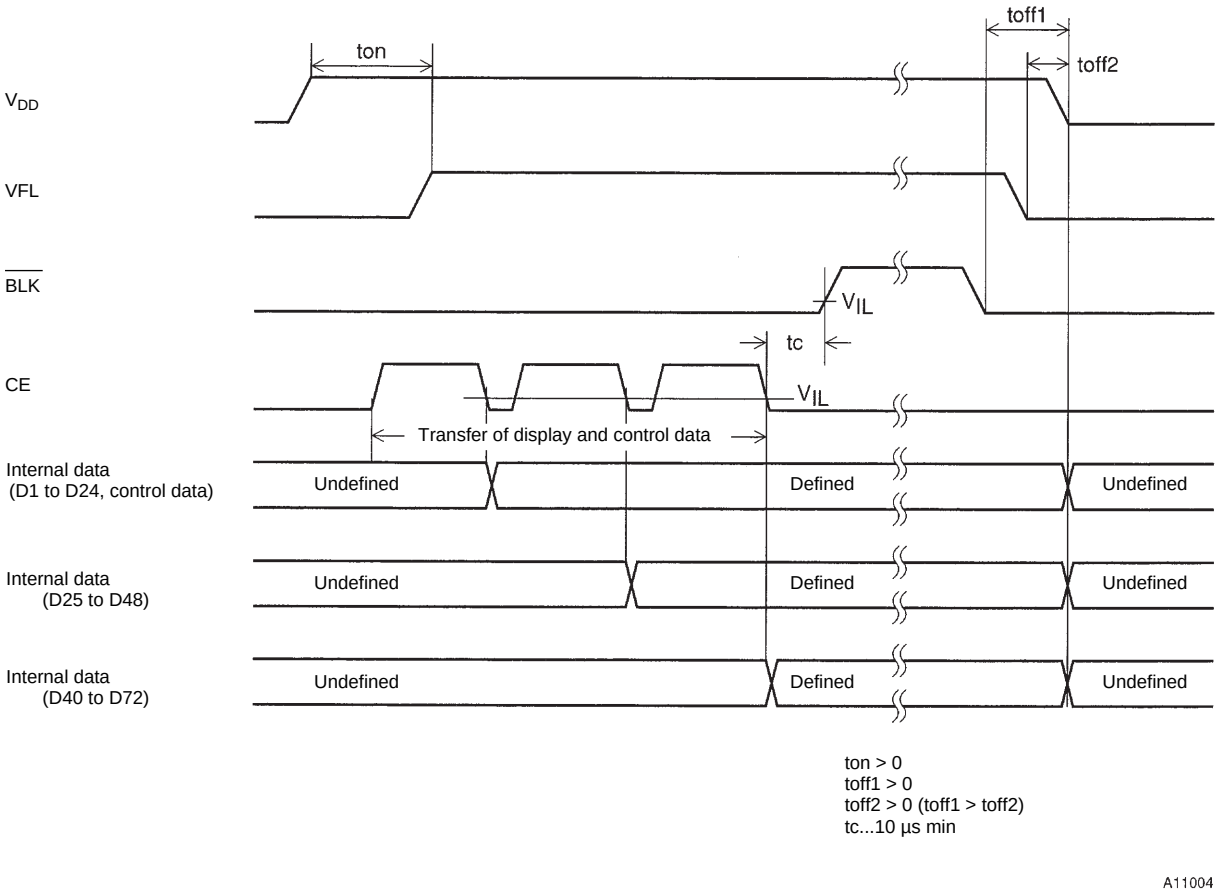
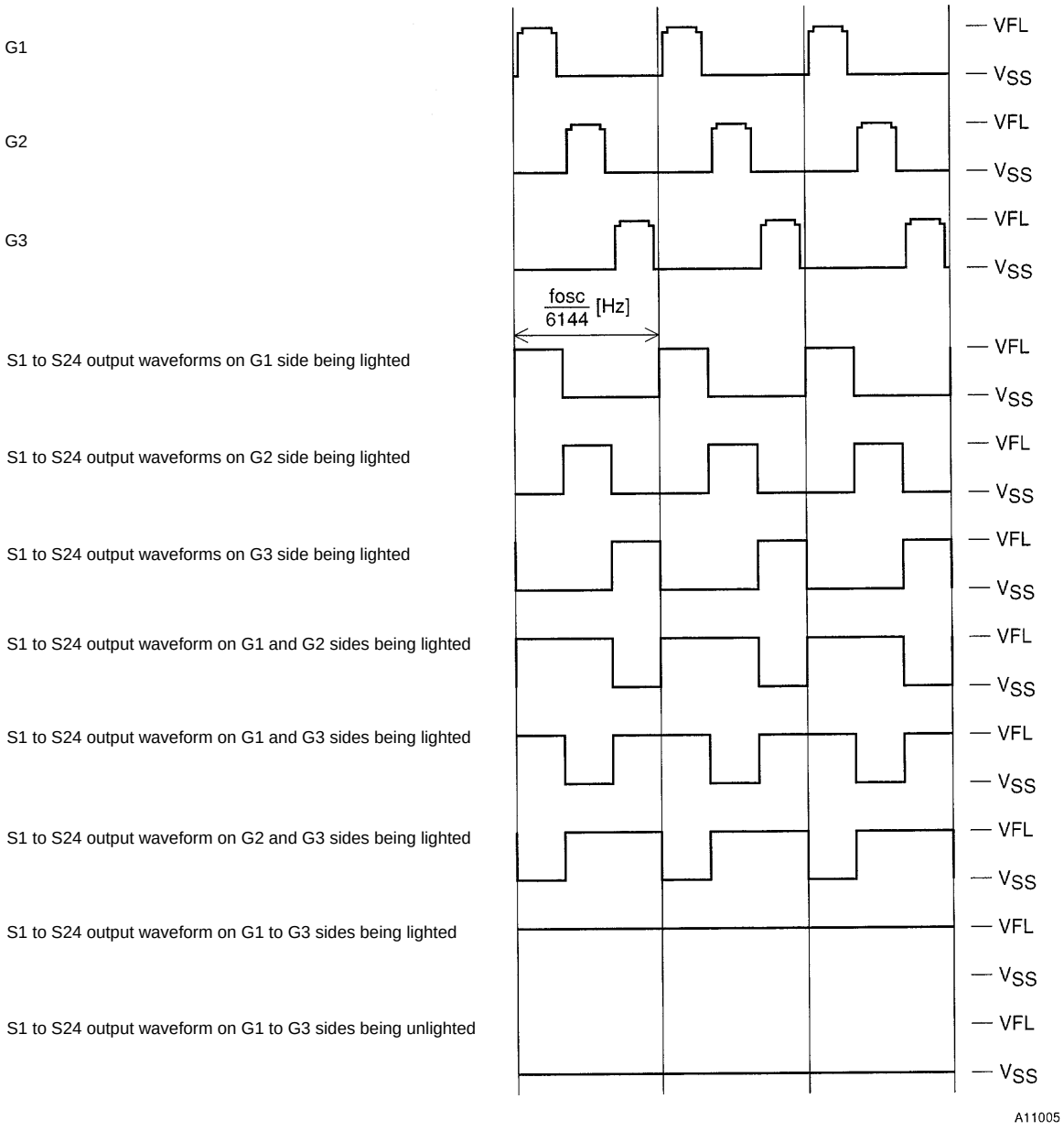


Figure 3

Output Waveforms (S1 to S24)



Relationship between Segment and Digit outputs

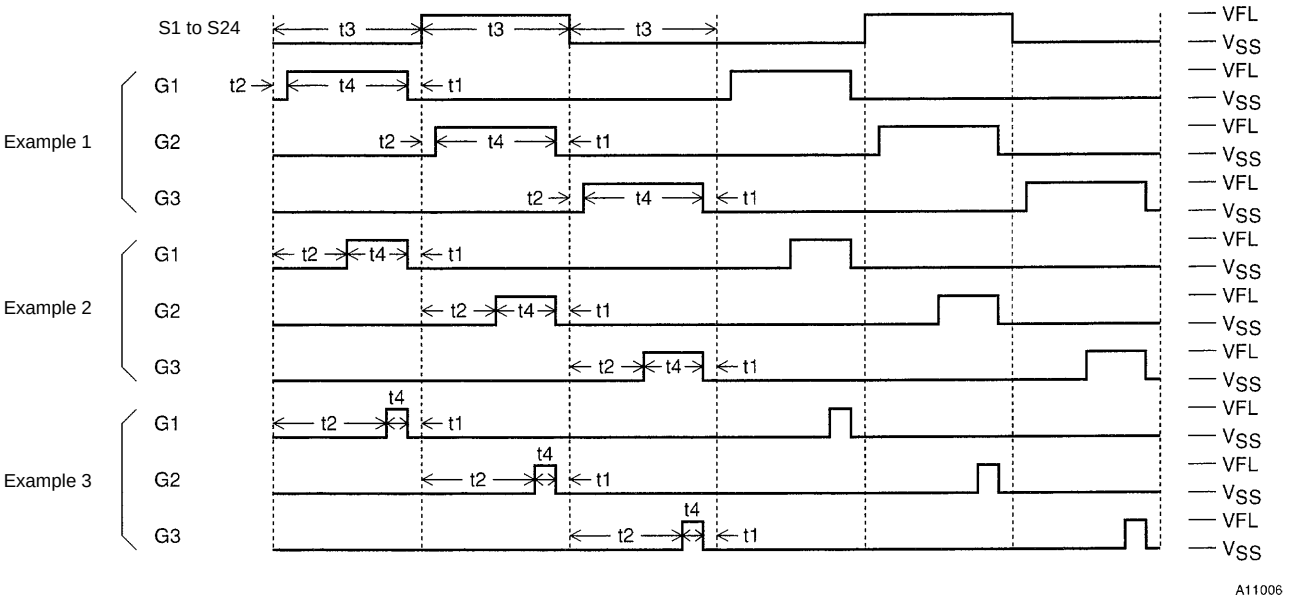


Figure 4

- Consider the examples shown in Figure 4, where display data is set up so that the segment outputs S1 to S24 output V_{SS} level on the G1 and G3 digit output timing and V_{FL} level on the G2 digit output timing. (Here, the G2 side being lighted) The relationship between the time t3 and the oscillator frequency f_{OSC} is $t3 = 2048/f_{OSC}$.
- The digit output G1 to G3 waveforms in Example 1 are output when the dimmer data (DM0 to DM9) are set to 3FEH. The relationship between the time t1 and the oscillator frequency f_{OSC} is $t1=2/f_{OSC}$. Note that the time t1 and the time t2 are the same period in Example 1.
- The digit output G1 to G3 waveforms in Example 2 are those when the dimmer data (DM0 to DM9) are set to a smaller value. Although the time t1 does not change, the time t2 becomes longer.
  When the dimmer data (DM0 to DM9) are set to $1FF_H$ and the oscillator frequency fosc is 2.4 [MHz], then the time t2 is :

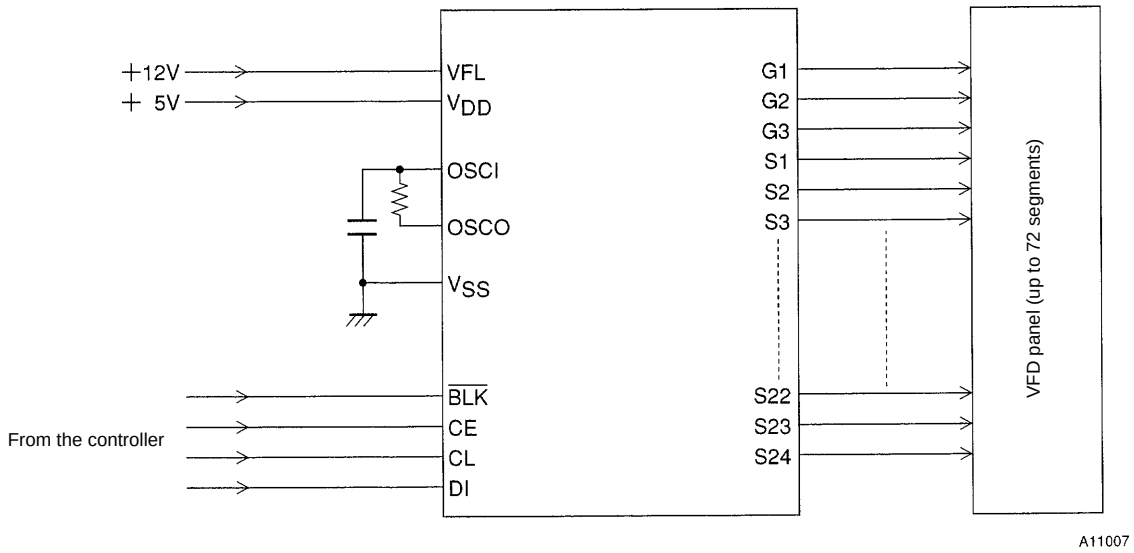
$$t2 = t3 - t1 \times (1FF_H + 1)$$

$$= \frac{1024}{f_{OSC}}$$

$$= 0.43[ms]$$

- When the dimmer data (DM0 to DM9) are set to an even smaller value, the time t2 becomes even longer, as in example 3. Note that the time t1 does not change here, either.

Sample Application Circuit



Notes on the Segment and Digit Waveforms

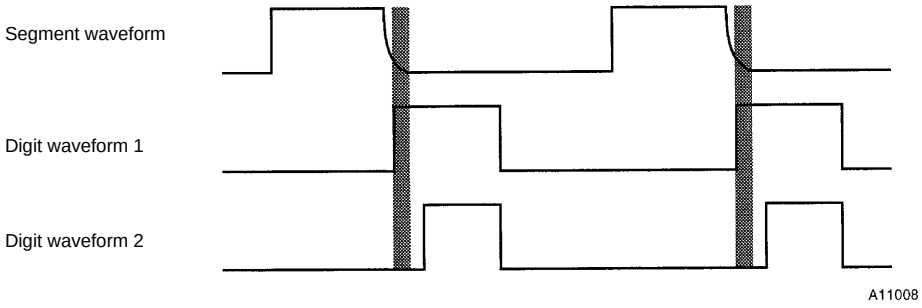


Figure 5

The segment waveform is distorted by the VFD panel used and the wiring, and furthermore, in the case of being used with essentially no dimming as in the digit waveform 1, as shown in Figure 5, the VFD panel glow dimly. By carefully considering the segment waveform, it can be seen that this problem can be resolved by applying an adequate amount of dimming, as shown in digit waveform 2.

Notes on Transferring Display Data from the Controller

Since display data is transferred in three operations as shown in Figure 2, we recommend that all display data be transferred within 30 [ms] to prevent degradation of the visual quality of the displayed image.