CMOS LSI

LC8903, 8903Q

## Digital Audio Interface Receiver

Overview

The LC8903 and LC8903Q are receiver LSIs for applications in which data is transmitted between digital audio equipment in the EIAJ format. These LSIs synchronize with the input signal and demodulate that signal to a regular format signal.

Features

• Built-in PLL circuit synchronizes with the input EIAJ format signal.

• Microprocessor interface receives mode settings and outputs fs codes, copy information, and category codes.

• Supports both 384 fs and 512 fs system clocks (selectable) and provides 256 fs, 128 fs, BCLK and LRCK clock outputs.

• Can operate in either digital source mode or analog source mode.

• Validity flag output

• User bit CD subcode interface

• DIP42S and QIP44M packages

• Silicon gate CMOS process, single 5 V power supply

Package Dimensions

unit: mm
3025B-DIP42S

[LC8903]

SANYO: DIP42S

unit: mm
**3148-QFP44MA**

[LC8903Q]

SANYO: QIP44MA

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Application Usage Overview Diagram

When both digital source mode and analog source mode are used

Digital source mode: EIAJ CP-1201 format data reception mode
Analog source mode: Analog data is received and converted to digital for signal processing.
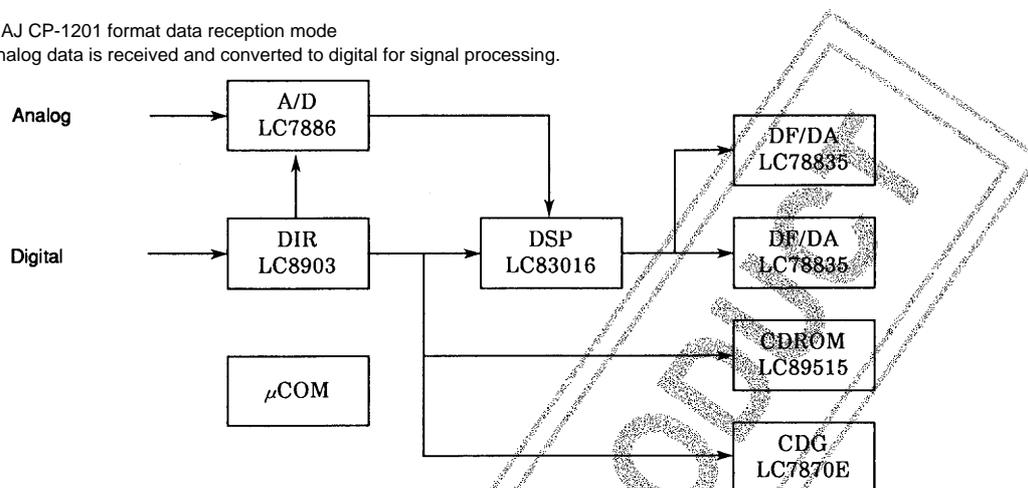
This figure shows an example of a structure using the LC8903/Q. In analog source mode the only function of the LC8903/Q is to provide control clocks.

Pin Assignments

DIP42S

DIN1	1		42	DVDD
DIN2	2		41	CL
DIN3	3		40	CE
DIN4	4		39	DI
DGND	5		38	DO
DIN5	6		37	EMPHA
DOUT1	7		36	LRCK
V/DOUT2	8		35	DATAOUT
RC1	9		34	BCLK
RC2	10		33	SUB2
CLKMD	11		32	SUB1
CLK	12		31	ERROR
TEST1	13		30	CLKOUT2
TEST2	14		29	CLKOUT1
XMODE	15		28	XOUT
AVDD	16		27	XIN
R	17		26	DVDD
AGND	18		25	SBCK
VIN	19		24	SFSY
VCO	20		23	PW
DGND	21		22	SBSY

LC8903

Top view

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QIP44M

LC8903Q

Top view

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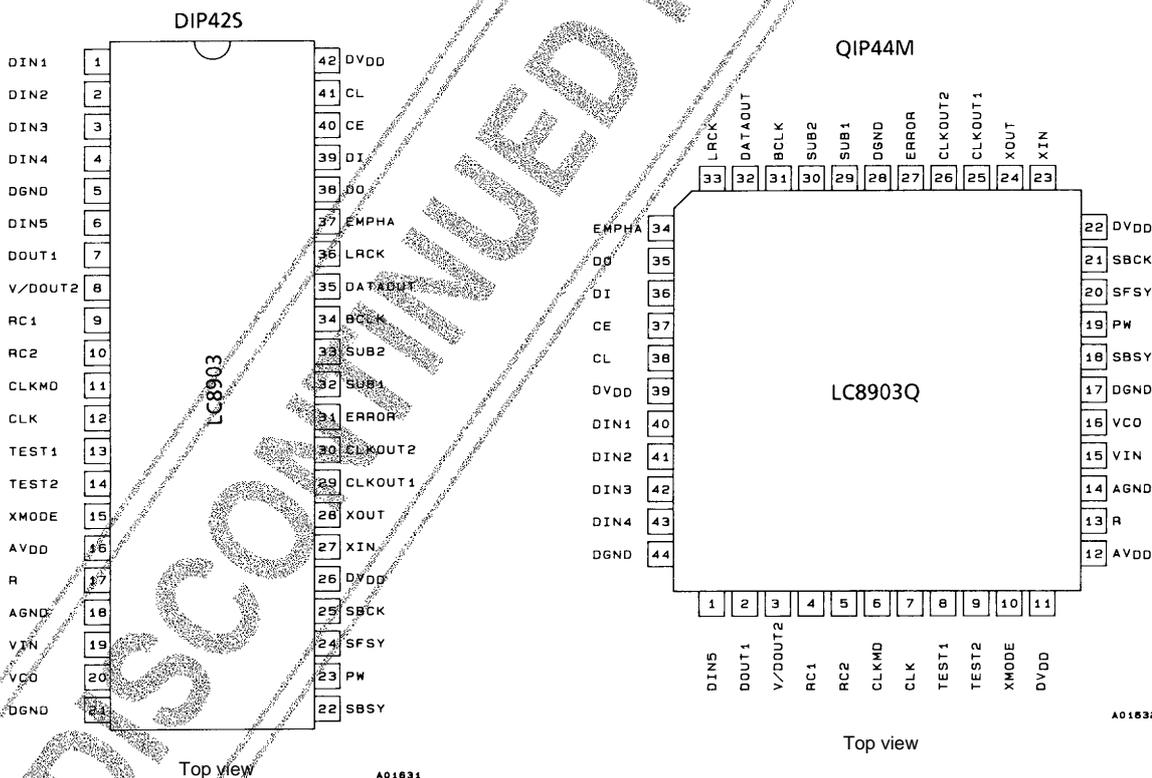
Specifications
Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		−0.3 to +7.0	V
Maximum I/O voltages	$V_I \cdot V_O$ max		−0.3 to V_{DD} + 0.3	V
Operating temperature	Topr		−30 to +75	°C
Storage temperature	Tstg		−55 to +125	°C

Allowable Operating Ranges

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Operating temperature	Topg		−30		+75	°C

DC Characteristics at Ta = –30 to +75°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high level voltage	$V_{IH}1$	*1	2.2		V_{DD} + 0.3	V
Input low level voltage	$V_{IL}1$	*1	−0.3		+0.8	V
Input high level voltage	$V_{IH}2$	*2	0.7 V_{DD}		V_{DD} + 0.3	V
Input low level voltage	$V_{IL}2$	*2	−0.3		0.3 V_{DD}	V
Input high level voltage	$V_{IH}3$	*3	0.8 V_{DD}		V_{DD} + 0.3	V
Input low level voltage	$V_{IL}3$	*3	−0.3		0.2 V_{DD}	V
Output high level voltage	V_{OH}	I_{OH} = −1 μA	V_{DD} − 0.05			V
Output low level voltage	V_{OL}	I_{OL} = 1 μA			V_{SS} + 0.05	V
Current drain	I_{DD}	V_{DD} = 5.0 V, Ta = 25°C, input data fs = 48 kHz	10	20	30	mA
Input amplitude	V_{PP}	*4	0.4		V_{DD} + 0.3	V

Note: 1. Input pins other than DIN1, DIN2, DIN3, DIN4, RC1 and XMODE. TTL compatible.
2. XIN pin. CMOS compatible.
3. The XMODE and RC1 pins. CMOS Schmitt inputs.
4. The condition prior to the capacitors on the DIN1, DIN2, DIN3 and DIN4 input pins.

AC Characteristics at Ta = –30 to +75°C, V_{DD} = 4.5 to 5.5 V

| Parameter	Symbol	Conditions	min	typ	max	Unit
Output pulse width	t_{WBO}	fs = 48 kHz, with a 30 pF load capacitance	160			ns
Output setup time	t_{DSO}		80			ns
Output data hold time	t_{DHO}		80			ns
Output delay (high)	t_{bdH}		−10	0	+10	ns
Output delay (low)	t_{bdL}		−10	0	+10	ns
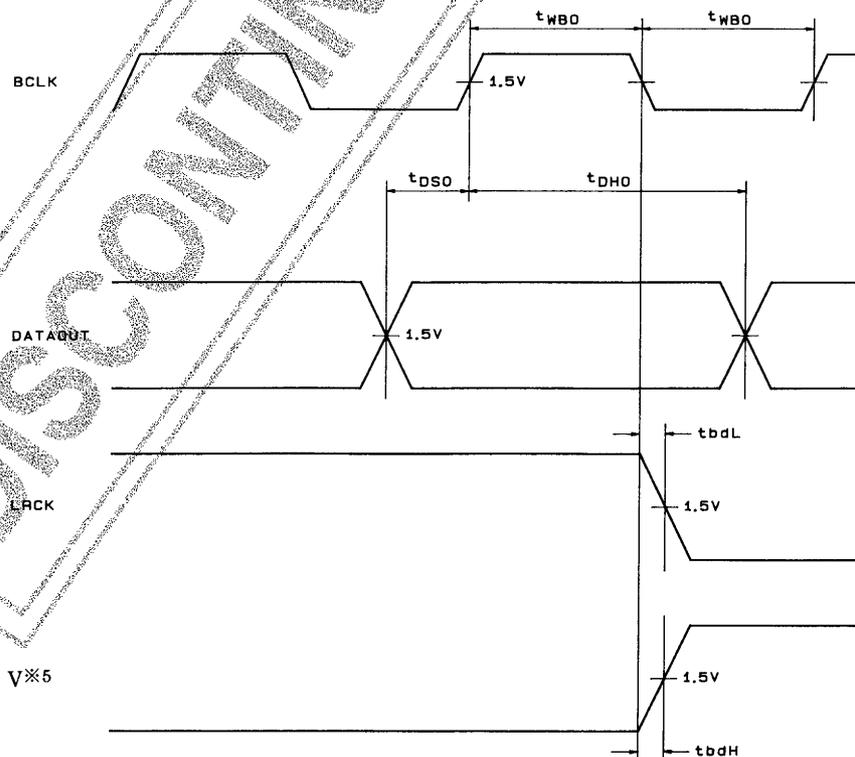
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Note: 5. When validity is output from the V/DOUT2 pin.

Microprocessor Interface Block AC Characteristics at Ta = –30 to +75°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
CL low level pulse width	TWL		100			ns
CL high level pulse width	TWH		100			ns
Data setup time	TDS		50			ns
Data hold time	TDH		50			ns
CL rise time	Tr	CL, CE, DI			30	ns
CL fall time	Tf	CL, CE, DI			30	ns
CE delay time	TD1		1.0			μs
CL delay time	TD2		50			ns
Data delay time	TD3	With a 30 pF load capacitance			25	ns
CL, data delay time	TD4	With a 30 pF load capacitance			50	ns
CL delay time	TD5		100			ns
CL, CE delay time	TD6		1.0			μs
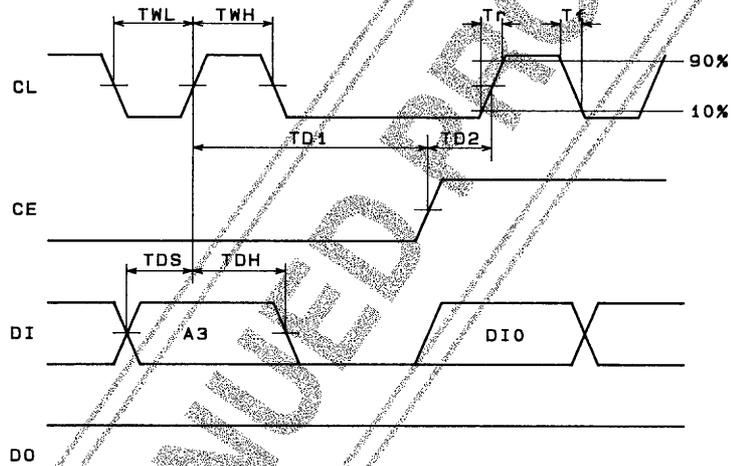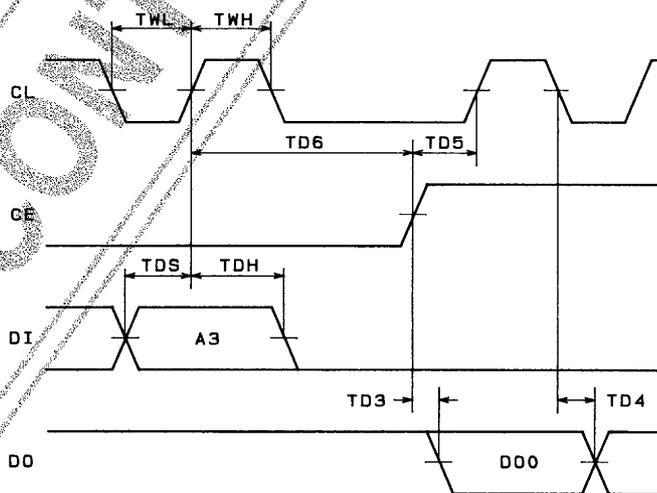
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CD Subcode Interface AC Characteristics at Ta = –30 to +75°C, V_DD = 4.5 to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
SBSY block frequency	tB		12.0	13.3	14.7	ms
SBSY pulse width	tBW	*6	110			μs
SFSY frame frequency	tF	*7	90	136	165	μs
SFSY high level pulse width	tFHW		4			μs
SFSY low level pulse width	tFLW		1.5			μs
SBCK high level pulse width	tCHW	*8	2.0	4.0	5.0	μs
SBCK low level pulse width	tCLW	*8	2.0	4.0	5.0	μs
SBCK rise time	trC				30	ns
SBCK fall time	tfC				30	ns
SBCK delay time	tCD	*8	10	20	30	μs
P data access	tPAC			3	10	μs
Data hold time	tHD		0			μs

Note: Assumes that the load capacitance on each output pin is 30 pF.
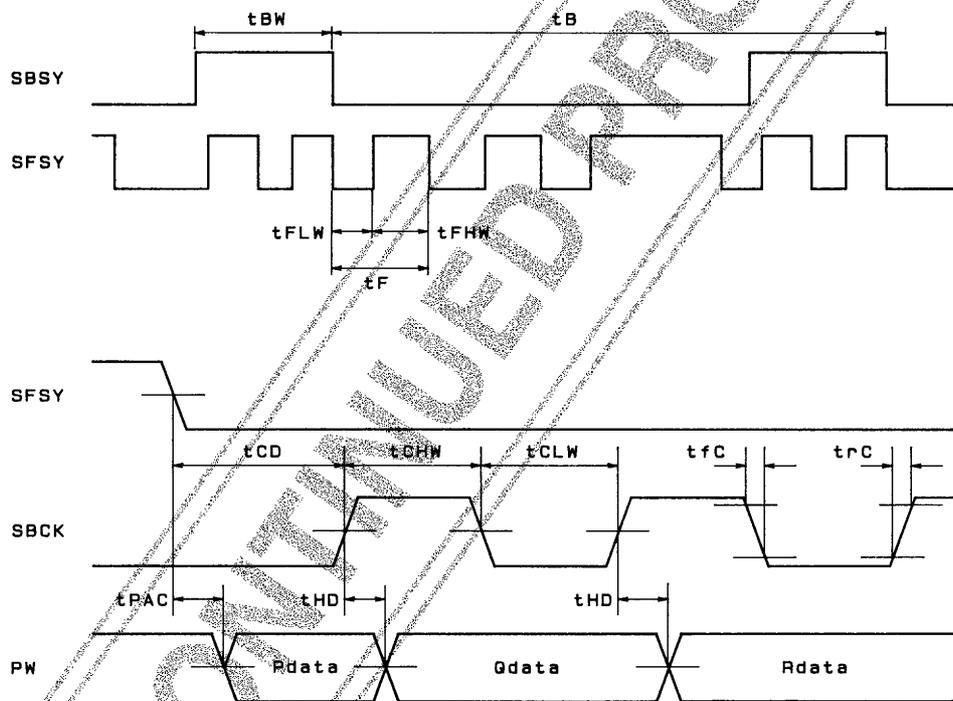
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The LC8903 and LC8903Q use the subcode synchronization word and the start bit in the user bits for subcode interface system timing extraction. Therefore, SBSY and SFSY change depending on that timing. Keep the following notes on user bit transfer in mind when using the values of tBW, tF, tCHW, tCLW and tCD within the specifications described above. Basically, user bit transfers must follow the table shown here.

	1	2	3	4	5	6	7	8	9	10	11	12	
S0	0	0	0	0	0	0	0	0	0	0	0	0	Subcode sync word*6, 7
S1	0	0	0	0	0	0	0	0	0	0	0	0	
S2	1	Q2	R2	S2	T2	U2	V2	W2	0	0	0	0	
S3	1	Q3	R3	S3	T3	U3	V3	W3	0	0	0	0	
:	:	:	:	:	:	:	:	:	:	:	:	:	
:	:	:	:	:	:	:	:	:	:	:	:	:	
S97	1	Q97	R97	S97	T97	U97	V97	W97	0	0	0	0	
S0	0	0	0	0	0	0	0	0	0	0	0	0	Subcode sync word*6, 7
S1	0	0	0	0	0	0	0	0	0	0	0	0	
S2	1	Q2	R2	S2	T2	U2	V2	W2	0	0	0	0	Word length*7, 8
:	:	:	:	:	:	:	:	:					

Note: 6. Subcode synchronization is taken as a block synchronization section (the start of a block) when a minimum of 22 consecutive data bits are zero.
7. The frame sync signal S0 period is 90.7 μs. The S1 period also has a minimum value of 90.7 μs (when there are 22 consecutive zero data bits), depending on the subcode sync word period.
8. When the shortest user data word length is used, the SBCK signal delay (tHD) and pulse widths (tCHW and tCLW) must be set below their typical values.

Pin Functions

Pin No.		Symbol	I/O	Function
QIP	DIP			
1	6	DIN5	I	Data input. There is no built-in amplifier on this pin.
2	7	DOUT1	O	EIAJ data through output
3	8	V/DOUT2	O	Validity flag output Alternatively, the microprocessor interface can set this pin to output the EIAJ input data unchanged.
4	9	RC1	I	RC oscillator input This circuit generates a clock used to detect incorrect PLL locking and to reset the PLL system.
5	10	RC2	O	RC oscillator output This pin outputs a clock with a frequency of about 40 kHz when the component values specified in the sample application circuit are used.
6	11	CLKMD	I	CLKOUT2 output clock switching: Low = 256 fs, high = 128 fs
7	12	CLK	I	Clock mode switching: Low = 384 fs, high = 512 fs
8	13	TEST1	I	Test pin (Should be tied low in normal operation.)
9	14	TEST2	I	
10	15	XMODE	I	Used to start system operation after power is applied.
11	—	DV_{DD}		Digital power supply
12	16	AV_{DD}		Analog power supply
13	17	R	I	VCO oscillator band adjustment
14	18	AGND		Analog ground
15	19	VIN	I	VCO free-running setting
16	20	VCO	O	PLL low-pass filter
17	21	DGND		Digital system ground
18	22	SBSY	O	Subcode interface block sync signal
19	23	PW	O	Subcode interface data output
20	24	SFSY	O	Subcode interface frame sync signal
21	25	SBCK	I	Subcode interface bit clock input
22	26	DV_{DD}		Digital power supply
23	27	XIN	I	Crystal oscillator input
24	28	XOUT	O	Crystal oscillator output
25	29	CLK OUT1	O	Crystal oscillator and VCO clock output
26	30	CLK OUT2	O	256 fs and 128 fs clock output
27	31	ERROR	O	Error mute signal output
28	—	DGND		Digital ground
29	32	SUB1	O	Sampling frequency output
30	33	SUB2	O	
31	34	BCLK	O	Bit clock output
32	35	DATA OUT	O	Audio data output
33	36	LRCK	O	Left/right clock output
34	37	EMPHA	O	High = emphasis on, low = emphasis off. Outputs a low level in analog mode.
35	38	DO	O	Microprocessor interface output
36	39	DI	I	Microprocessor interface input
37	40	CE	I	Microprocessor interface chip enable input
38	41	CL	I	Microprocessor interface clock input
39	42	DV_{DD}		Digital power supply
40	1	DIN1	I	Data inputs with built-in amplifiers
41	2	DIN2	I	
42	3	DIN3	I	
43	4	DIN4	I	
44	5	DGND		Digital ground

Block Diagram
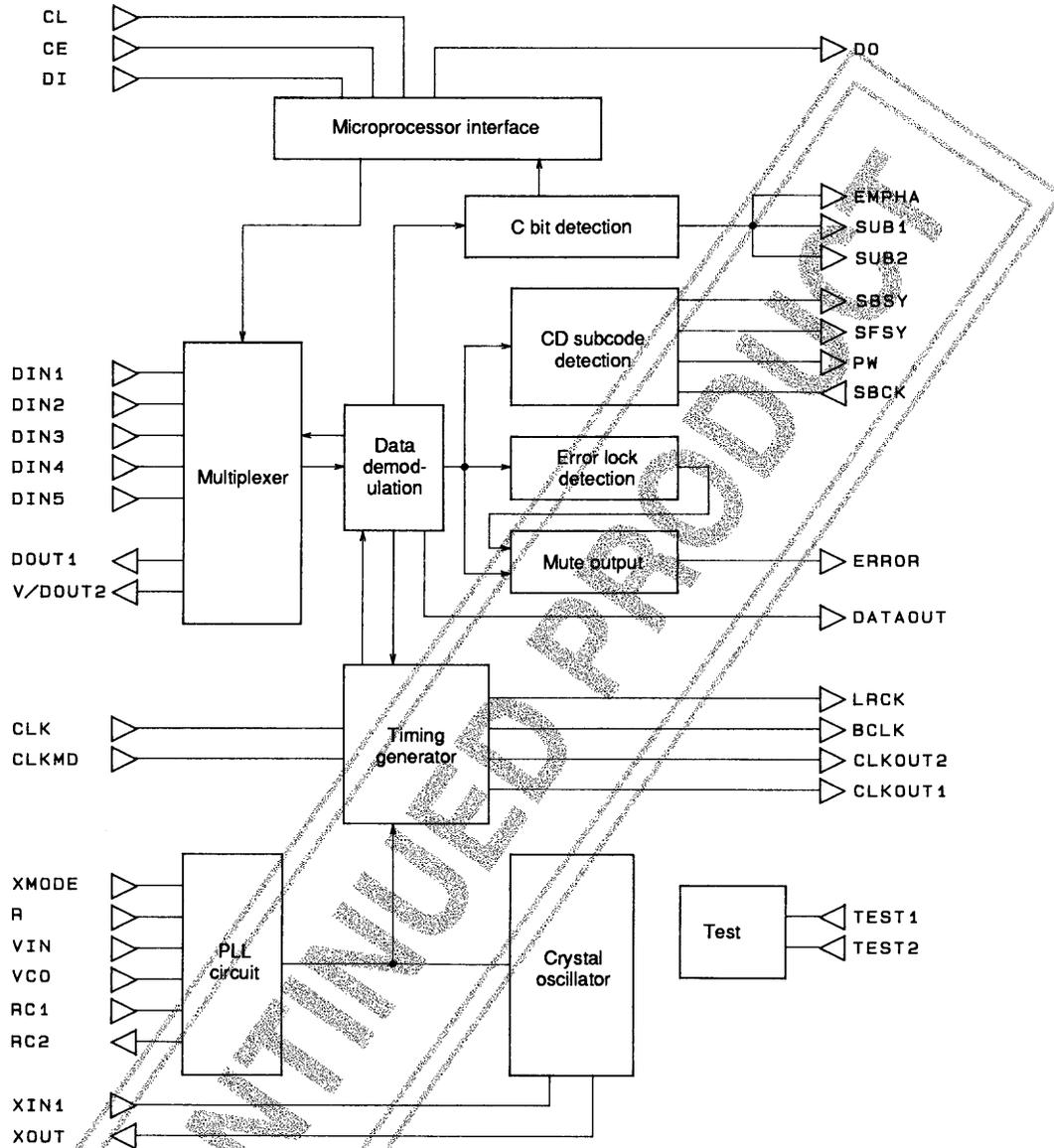
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Clock Modes

The LC8903/Q CLKOUT1 and CLKOUT2 output clock modes are selected by the CLK and CLKMD pins according to the table.

| CLK	CLK OUT1
L	384 fs clock output
H	512 fs clock output

CLK MD	CLK OUT2
L	256 fs clock output*
H	128 fs clock output

Note: * When the CLK pin is low, the 256 fs clock duty has a high to low ratio of 2:1.

Microprocessor Interface

The microprocessor interface is used for specifying the data input pin, for setting the output data format, and for specifying subcode output, system stop, and analog source mode. The figure shows the interface I/O formats.

Microprocessor Interface Formats

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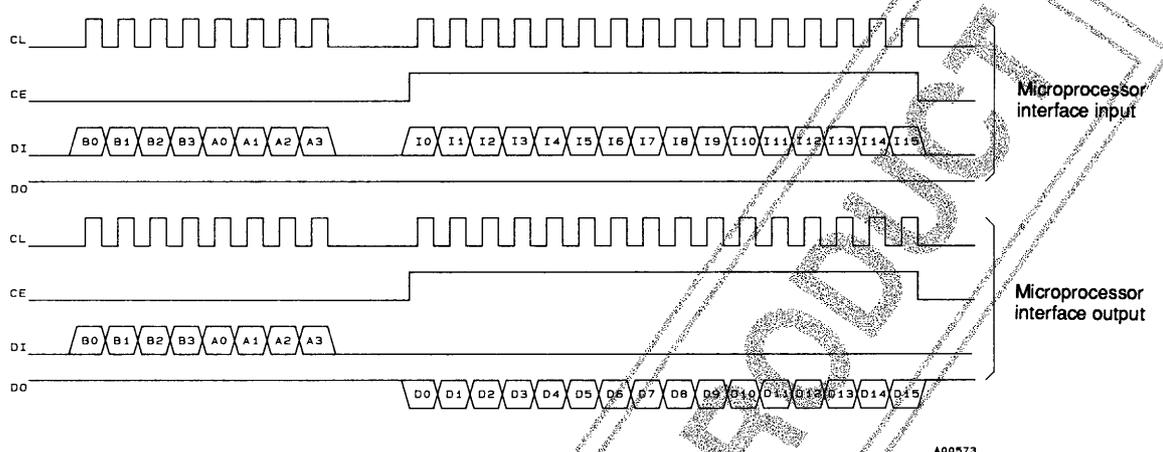
Address

The bits B0 to A3 in the format figure are the address. There are two addresses allocated to the LC8903/Q, one for input and one for output. The microprocessor must specify the input address to input data and the output address to output data.

Address Code

Mode	B0	B1	B2	B3	A0	A1	A2	A3
Data input	H	L	H	L	L	H	H	L
Data output	L	H	H	L	L	H	H	L

Microprocessor Interface Input

1. Input pin and validity output settings
   The DIN1 to DIN4 data input pins have built-in amplifiers and can accept signals with levels of about 400 mVp-p.
   DIN5 is a special-purpose input pin for optical input.

Data input system

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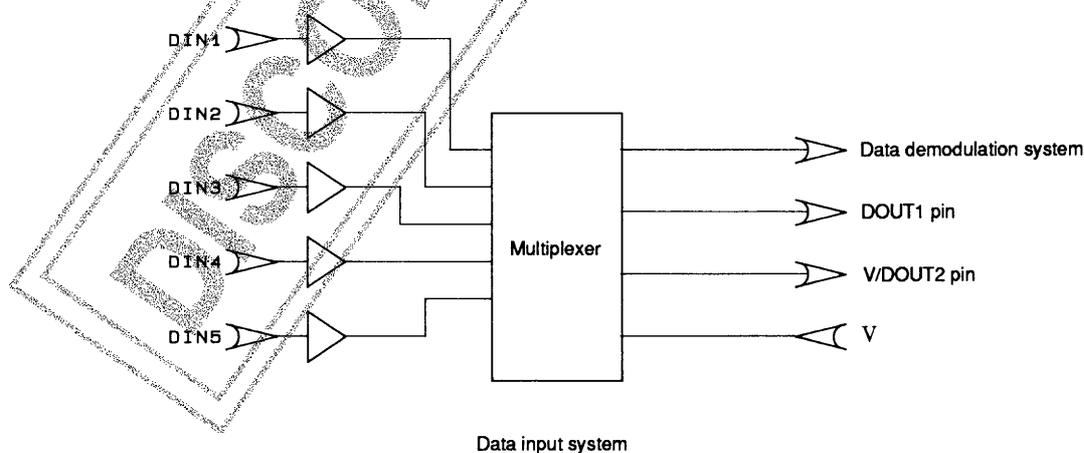
The data input system multiplexer is controlled by inputs from the microprocessor interface. The table shows the relationship between the code in bits I5 to I13 in the microprocessor interface format and the data demodulation outputs DOUT1 and V/DOUT2.
V is output from the V/DOUT2 pin.

I5	L	H	L	H	L	H	L	H
I6	L	L	H	H	L	L	H	H
I7	L	L	L	L	H	H	H	H
Data demodulation input	DIN1	DIN2	DIN3	DIN4	DIN5	XSYS	XSYS	XSYS

I8	L	H	L	H	L	H	L	H
I9	L	L	H	H	L	L	H	H
I10	L	L	L	L	H	H	H	H
DOUT1	DIN1	DIN2	DIN3	DIN4	DIN5	GND	GND	GND

I11	L	H	L	H	L	H	L	H
I12	L	L	H	H	L	L	H	H
I13	L	L	L	L	H	H	H	H
DOUT2	V	DIN1	DIN2	DIN3	DIN4	DIN5	GND	GND

Note: Setting the data demodulation input code to one of the XSYS settings switches the system clock from the VCO to the crystal oscillator and sets the LC8903/Q to analog source mode. Selecting one of the input pins once again sets the LC8903/Q to digital source mode and PLL operation.

2. Data output mode setting

There are two data output modes: 16-bit MSB first and 20-bit msb first. These are selected by the bit I14 code.

I14	L	H
Data output mode	16-bit MSB first	20-bit MSB first

3. System stop

The operation of both the VCO and the crystal oscillator can be stopped, thus stopping the whole LC8903/Q system, by setting the bit I4 code as shown in the table.

I4	L	H
—	System operation	System stop

The values of the bits I4 to I14 are all initialized to low immediately after the XMODE pin goes from low to high. Since bits I0 to I3 and I15 are not used, their initial values are undefined.

Microprocessor Interface Output

Bits D0 to D15 in the microprocessor interface output format have the following meanings.

Bit	Function
D0	Invalid bit. Always output as a low level.
D1 D2	Indicates the sample frequency. Corresponds to the fs external output pin.
D3	Indicates the state of the copy flag. High = copy enabled, low = copy protect
D4	Outputs the first bit of the channel status bits.
D5 to D12	These pins output the channel status 8-bit category codes serially.
D13 to D15	Invalid bits. Always output as low levels.

Interpretation of the D1 and D2 bits

Sampling frequency	32 kHz	44.1 kHz	48 kHz	#1
D1	H	L	L	H
D2	H	L	H	L

Note: 1. The "#1" value indicates either a PLL lock error or analog source mode. In these states the data is cleared and bits D0 and D3 to D15 are all set to low.
2. D1 and D2 are in the "#1" state in the initial values of the codes immediately after the XMODE pin goes from low to high. All other codes are set to low.
3. The interval between one microprocessor data readout operation and the next must be 6 ms or longer.

FS Output Code

The SUB1 and SUB2 pins indicate the input data sampling frequency.

Sampling frequency	32 kHz	44.1 kHz	48 kHz	#1
SUB1	H	L	L	H
SUB2	H	L	H	L

Note: The "#1" value indicates PLL lock error or analog source mode. When SUB1 and SUB2 have these values, the DATAOUT and EMPHA pins will output low levels.

CD Subcode Interface

The LC8903 and LC8903Q use the SFSY, SBCK, PW and SBSY pins to output the CD subcode data. This data is the user bits that were transferred according to the CP-1201 interface format and converted to a format that conforms to the CP-2401 interface format. The timing is shown in the figures.
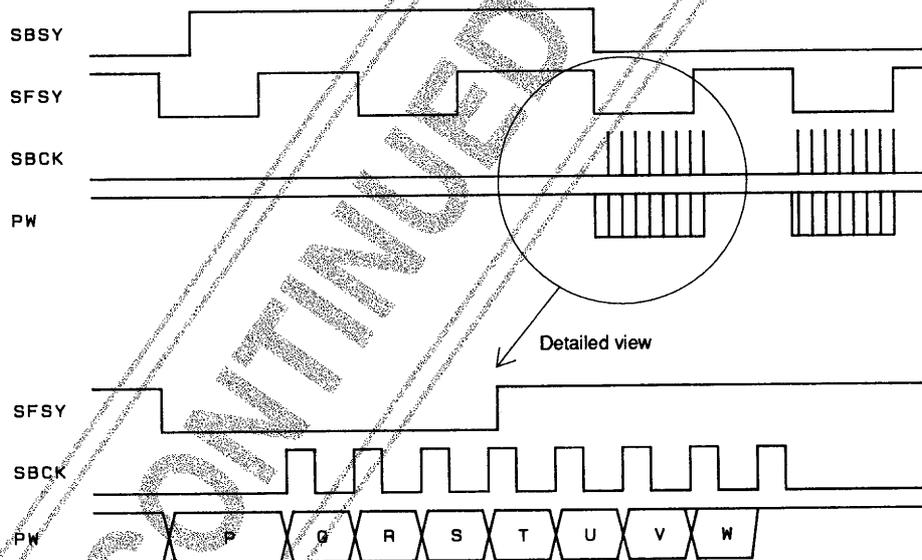
The timing of the rising and falling edges of the SFSY signal is changed according to the timing of the start bits in the input data user bits as shown in the figure.
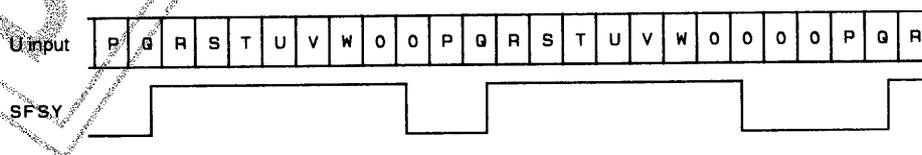
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Errors

1. ERROR pin: This pin goes high when there are errors in the input data or when the PLL circuit is unlocked. When data demodulation returns to normal, the high level is held for about 200 to 300 ms and then the ERROR pin goes low. This time is inversely proportional to the fs of the input data.
2. Data processing when an error occurs: The table lists the data processing performed when an error occurs.

Error Type	Audio Output Data	FS Output Code	V Flag
Up to 8 consecutive parity errors	Previous data value output	Retained	Output
Nine or more consecutive parity errors	Data with the value zero is output.	Retained	Output
PLL lock error	Data with the value zero is output.	Data is cleared and the "#1" state is indicated.	Cleared, and a low level output.

Note: Preamble detection is used to recognize PLL lock errors.

Analog Source Mode

The LC8903 and LC8903Q switch to analog source in the following two cases.

1. When analog source mode is selected by the data sent over the microprocessor interface
2. When there is no signal on the input pin selected for data demodulation
   In analog source mode, the clock that runs the whole system is supplied by the crystal oscillator clock and the PLL circuit and data demodulation are stopped. The BCLK, LRCK, CLK, OUT1 and CLKOUT2 clocks are output. The output pins function as follows in analog source mode.

   - DOUT1, V/DOUT2
     Data specified through the microprocessor interface is output.
   - ERROR
     The lock error state high level is output.
   - SUB1, SUB2
     The "#1" lock error state code is output.
   - DATAOUT
     The lock error state low level is output.
   - EMPHA, V flag
     The lock error state low level is output.
   - Microprocessor interface codes
     Input codes: The code values set through the microprocessor interface are retained.
     Output codes: Values identical to those for a PLL lock error are output.

Crystal Oscillator

1. The presence or absence of data is determined by an internal detection circuit. This circuit operates on either the VCO or the crystal oscillator clock. When power is first applied, the clock is supplied from the VCO, and the LC8903 and LC8903Q switch to the crystal oscillator if a no data state is detected. Here, if a clock signal was not supplied from the crystal oscillator after a no data state is detected, the whole system would stop and remain in the stopped state, since the detection circuit would not operate even if data were supplied.
2. The XIN and XOUT pins include a built-in oscillator amplifier circuit, and take on the following states when a crystal oscillator is connected.

Pin	Data Present*	Data Absent
XIN	High	Accepts crystal oscillator input.
XOUT	Low	Outputs the inverted state of the XIN pin.

Note: * The XIN pin is pulled-up internally when the LC8903/Q is in the data present state.

XMODE

The XMODE pin resets the LC8903 and LC8903Q system. The LC8903 and LC8903Q will start to function normally if a high level is applied to this pin after the power supply voltage rises above a value of at least 4.5 V.
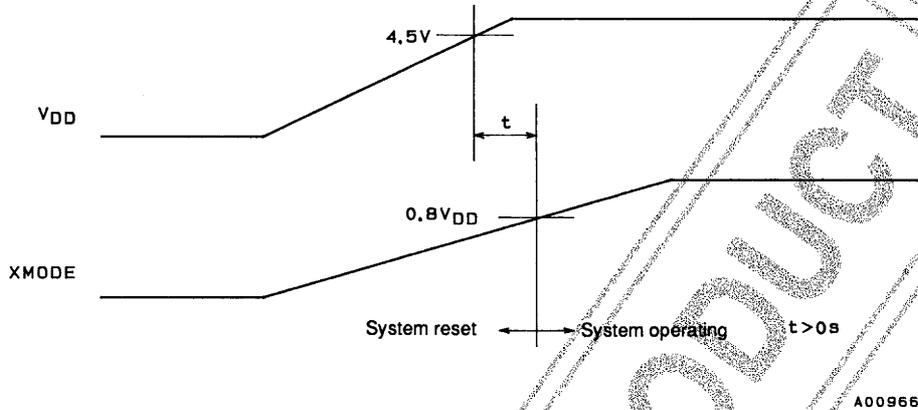

1. Once the LC8903 and LC8903Q is operating, the system will be reset if a low level is applied once again to the XMODE pin.
2. This IC can be used without using the microprocessor interface by tying the CE, CL and DI microprocessor interface input pins low and using D1 as the data input pin. This technique can be used as a simplified method for product evaluation.

Data Output Timing

The figures show the data output timing.

1. Data is output in synchronization with the falling edge of the BCLK signal.
2. Data, BCLK and LRCK are output in synchronization with the rising edge of the 256 fs clock.
3. The data output timings for 20-bit MSB first and 16-bit MSB first output are shown in the timing charts.

Timing Chart
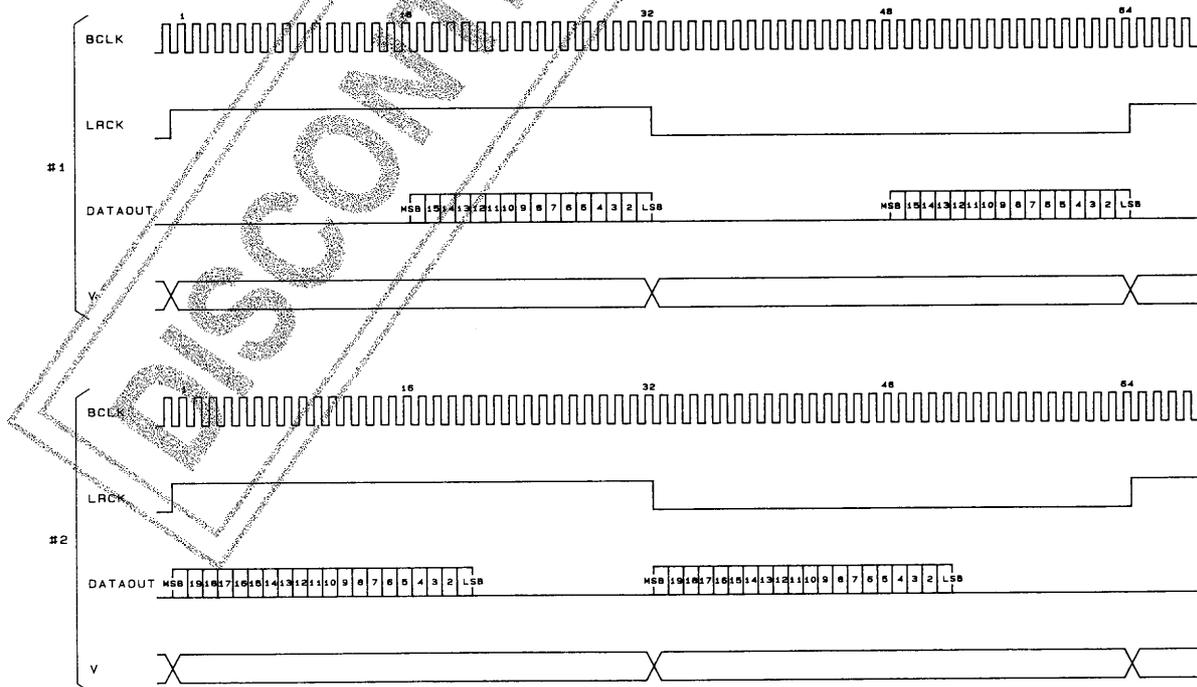
Timing chart #1 is for 16-bit MSB first output mode.
Timing chart #2 is for 20-bit MSB first output mode.

Sample Application Circuit

1 DIN1	DV$_{DD}$	42
2 DIN2	CL	41
3 DIN3	CE	40
4 DIN4	DI	39
5 DGND	DO	38
6 DIN5	EMPHA	37
7 DOUT1	LRCK	36
8 V/DOUT2	DATAOUT	35
9 RC1	BCLK	34
10 RC2	SUB2	33
11 CLKMD	SUB1	32
12 CLK	ERROR	31
13 TEST1	CLKOUT2	30
14 TEST2	CLKOUT1	29
15 XMODE	XOUT	28
16 AV$_{DD}$	XIN	27
17 R	DV$_{DD}$	26
18 AGND	SBCK	25
19 VIN	SFSY	24
20 VCO	PW	23
21 DGND	SBSY	22

Input pins
Described in detail
on the following
page in the section

Microprocessor
interface

CD subcode
interface

A01636

Circuit Constants

Item	Symbol	Value	Item	Symbol	Value
Resistors	R1	33 kΩ	Capacitors	C1	1000 pF
	R2	10 kΩ		C2	10 to 100 µF
	R3	24 kΩ		C3	0.1 µF
	R4	5.6 kΩ		C4	0.01 µF
	R5	5.6 kΩ		C5	10 to 47 pF
	R6	120 to 150 Ω		C6	10 to 47 pF
	R7	200 Ω			
	R8	200 kΩ			

Input Pin Application Circuits

Coaxial input circuit

330k

0.1μ

≥75

DIN1 to DIN4

Optical input

56k

75

DIN1 to DIN4

Optical module

75

DIN5

Optical module

Unit (resistance: Ω, capacitance: F)

A00969

Sample optical modules: TORX174, TORX176