

# **OKI** Semiconductor

# MSM531655E

524,288-Double Words x 32-bit or 1,048,576-Words x 16-bit MaskROM 8Double Word x 32-Bit or 16Word x 16-Bit/Page Mode MASKROM

#### DESCRIPTION

The OKI MSM531655E is a 524,288-double words x 32-bit or 1,048,576-words x 16-bit CMOS Mask ROM with an asynchronous page read mode. Each page is organized 8 double words x 32-bit or 16 words x 16-bit. It operates on a single 5.0V power supply and is TTL compatible. The chip's asynchronous I/O requires no external clock assuring easy operation. A power-down mode provides low power dissipation when the chip is not selected. The CE and OE pins are provided as control signals that permit three-stated output allowing easy memory expansion on a system bus. The MSM531655E is suited for use as large capacity fixed memory for microcomputers and data terminals.

#### ■ FEATURES

- Single 5.0V power supply
- 524,288-double words x 32-bit / 1,048,576-words x 16-bit
- 8-double words(A2,A1,A0) or 16-words(A2,A1,A0,A-1) / Page
- Access time 100ns Max (Normal access)
- 50ns Max (Page access)

  Input/Output TTL compatible
- Tri-State output configurations
- Internal powerdown function
- Packages:

70-PIN PLASTIC SSOPP (SSOP70-P-500/0.8-K) (MSM531655E-xxGS-K) 70-PIN PLASTIC TSOP(Type II) (TSOP70-P-400/0.65-K) (MSM531655E-xxTS-K)

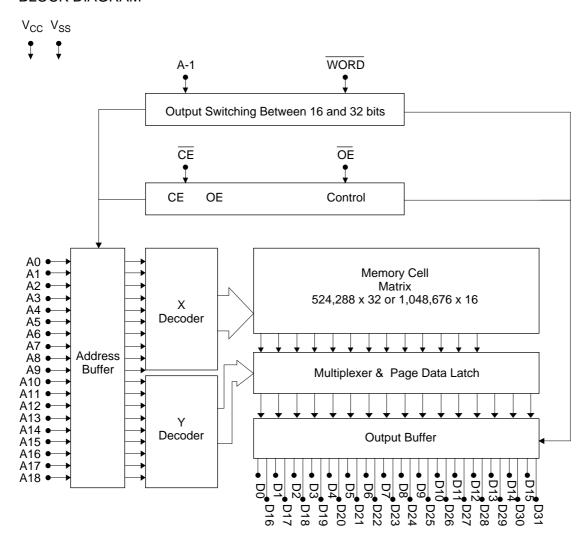
Pin compatible OTP available

# PIN CONFIGURATION

		ı	
A0 1	0	70	NC
A1 2		69	NC
A2 3			NC
A3 4		67	WORD
A4 5		66	OE
A5 6		65	CE
Vcc 7		64	Vss
D0 8		63	D31/A-1
D16 9		62	D15
D1 10		61	D30
D1711		60	D14
Vss 12		59	Vss
Vcc 13		58	Vcc
D2 14		57	D29
D18 15		56	D13
D3 16		55	D28
D1917		54	D12
D4 18		53	D27
D2019		52	D11
D5 20		51	D26
D21 21		50	D10
Vss 22		49	Vss
Vcc 23		48	Vcc
D6 24		47	D25
D22 25		46	D9
D7 26		45	D24
D23 <sub>27</sub>		44	D8
Vss <sub>28</sub>		43	Vcc
A6 29		42	NC
A730		41	A18
A8 31		40	A17
A932		39	A16
A1033		38	A15
A1134		37	A14
A1235		36	A13
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Pin Name	Function
D31/A-1	Data output / address input
A0 to A18	Address input
D0 to D30	Data output
CE	Chip enable
ŌĒ	Output enable
WORD	Mode switch (H:DW/L:W)
V <sub>CC</sub> , V <sub>SS</sub>	Power supply

## **BLOCK DIAGRAM**



# **FUNCTION TABLE**

CE	ŌĒ	BYTE	A-1/D31	D0—D15	D16—D31	D <sub>OUT</sub> Mode	LSB	MSB
Н	Χ	Х	X	Hi-Z	Hi-Z	Hi-Z		
L	Н	Х	X	Hi-Z	Hi-Z	1 II-Z	_	_
L	L	Н	Input Inhibited (D31)	D0 to D15	D16 to D31	32 bit	A0	A18
L	L	Н	Input Inhibited (D31)	D0 to D15	D16 to D31	32 bit(Page Mode)	A0	A2
L	L	L	L	D0 to D15	Hi-Z	16 bit	A-1	A18
L	L	L	Н	D16 to D31	Hi-Z	10 011		AIO
L	L	L	L	D0 to D15	Hi-Z	16 bit(Page Mode)	۸ 1	A2
L	L	L	Н	D16 to D31	Hi-Z	10 bit(Fage Mode)	A-1	AZ

# ABSOLUTE MAXIMUM LIMITS

Parameter	Symbol	Conditions	Limits	Unit
Power Supply Voltage	V <sub>cc</sub>		-0.3 to 7	V
Input Voltage	V <sub>I</sub>	to V <sub>SS</sub>	$-0.3$ to $V_{CC} + 0.5$	V
Output Voltage	Vo		$-0.3$ to $V_{CC} + 0.5$	V
Power Dissipation	P <sub>D</sub>	Per Package T <sub>opr</sub> = 25°C	1.0	W
Operating Temperature	T <sub>opr</sub>	_	0 to 70	°C
Storage Temperature	T <sub>stg</sub>		-55 to 150	°C

# RECOMMENDED OPERATING CONDITIONS

Devenuetes	0	0		1.1:4		
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Power Supply Voltage	V <sub>cc</sub>	_	4.5	5.0	5.5	V
	V <sub>SS</sub>	_	0.0	0.0	0.0	V
"H" Input Voltage	V <sub>IH</sub>	_	2.2	5.0	5.5	V
"L" Input Voltage	V <sub>IL</sub>	_	-0.3	0.0	0.8	V
Operating Temperature	T <sub>opr</sub>	_	0	_	70	°C

# n DC CHARACTERISTICS

 $(V_{CC} = 5V \pm 10\%, Ta = 0 \text{ to } 70^{\circ}C)$ 

Parameter	Symbol	Conditions		Unit		
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
"H" Output Voltage	V <sub>OH</sub>	$I_{OH} = -400uA$	2.4	_	_	V
"L" Output Voltage	V <sub>OL</sub>	I <sub>OH</sub> = 2.1mA	_	_	0.4	V
Input Leakage Current	ILI	$V_I = 0$ to $V_{CC}$	-10		10	μA
Output Leakage Current	I <sub>LO</sub>	$\frac{V_O}{CE} = 0 \text{ to } V_{CC}$	-10	_	10	μΑ
Power Supply Current (Operating)	I <sub>CC</sub>	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}, t_C = 100$ ns	_	_	120	mA
Power Supply Current	I <sub>CCS</sub> 1	$\overline{CE} = V_{CC} - 0.2V$	_	_	50	μA
(Standby)	I <sub>CCS</sub>	CE = V <sub>IH MIN</sub>	_	_	500	μA

# AC CHARACTERISTICS

# Test conditions

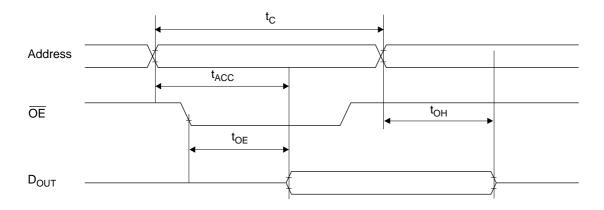
Parameter	Conditions
Input Signal Level	V <sub>IH</sub> =3.0V, V <sub>IL</sub> =0.0V
Transtion Time	t <sub>r</sub> =t <sub>f</sub> =5ns
Timing Reference Level	Input Voltage=1.5V Output Voltage=0.8V&2.0V
Load Condition	CL=100pF+1TTL

# Read Cycle

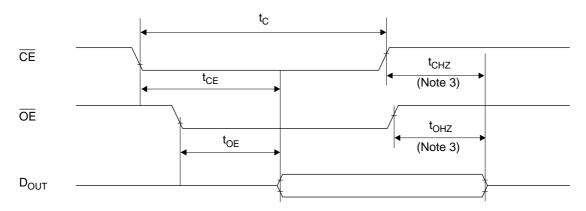
 $(Ta = 0 \text{ to } 70^{\circ}C)$ 

Parameter	Currele el	Conditions				
Farameter	Symbol		Min.	Тур.	Max.	Unit
Random Access Cycle time	t <sub>C</sub>		100	_	_	ns
Random Address Access time	t <sub>ACC</sub>	_	_	_	100	ns
Page Set up time	t <sub>PSET</sub>	_	120	_	_	ns
Page Access Cycle time	t <sub>PC</sub>	_	50	_	_	ns
Page Access time	t <sub>PAC</sub>	_	_	_	50	ns
CE Access time	t <sub>CE</sub>	_	_	_	100	ns
OE Access time	t <sub>OE</sub>	_	_	_	50	ns
CE Output Disable time	t <sub>CHZ</sub>		0	_	40	ns
OE Output Disable time	t <sub>OHZ</sub>	_	0	_	30	ns
Output Hold time	t <sub>OH</sub>	_	0	_	_	ns

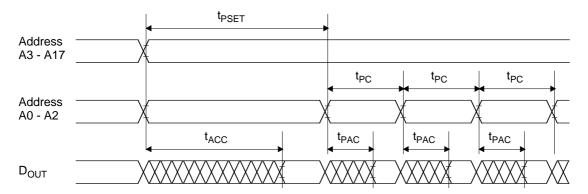
# Read Cycle (Note1)



# Read Cycle (Note2)



# Page Mode Read Cycle (Note4)



#### Note)

- 1.  $\overline{CE}$  is low level.
- 2. Address is fixed before or at the same time when  $\overline{\text{CE}}$  level falls.
- t<sub>CHZ</sub> & t<sub>OHZ</sub> indicate the time until floating. They are not determined by the output level.
   \overline{CE} is low level and \overline{OE} is low level.

### I/O CAPACITANCE

Parameter	Symbol	Conditions	R	1.1:4		
		Conditions	Min.	Тур.	Max.	Unit
Input Capacitance	Cı	V <sub>I</sub> =0V	_	_	8	pF
Output Capacitance	Co	V <sub>O</sub> =0V	_	_	10	pF



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