

# THYRISTOR MODULE

## PAT2008 PAH2008

### 200A / 800V

#### FEATURES

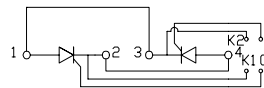
- \* Isolated Base
- \* Dual Thyristors or Thyristor and Diode Anti-Parallel Circuit
- \* High Surge Capability
- \* UL Recognized, File No. E187184

#### TYPICAL APPLICATIONS

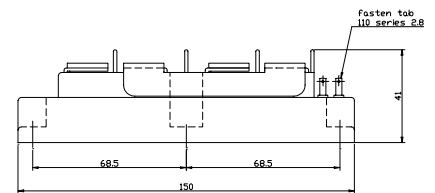
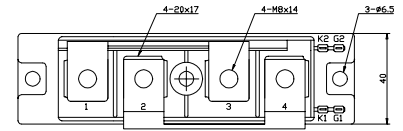
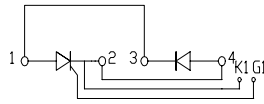
- \* Rectified For General Use

#### OUTLINE DRAWING

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#### Maximum Ratings

Approx Net Weight:500g

Parameter	Symbol	Grade	Unit
		PAT/PAH2008	
Repetitive Peak Off-State Voltage	$V_{DRM}$	800	V
Non Repetitive Peak Off-State Voltage	$V_{DSM}$	900	
Repetitive Peak Reverse Voltage	$V_{RRM}$	800	V
Non Repetitive Peak Reverse Voltage	$V_{RSM}$	900	

Parameter		Conditions	Max Rated Value	Unit
Average Rectified Output Current	$I_{O(AV)}$	50Hz Half Sine Wave condition $T_c=65^\circ\text{C}$	200	A
RMS On-State Current	$I_{T(RMS)}$		314	A
Surge On-State Current	$I_{TSM}$	50 Hz Half Sine Wave, 1Pulse Non-Repetitive	4000	A
I Squared t	$I^2t$	2msec to 10msec	8000	$\text{A}^2\text{s}$
Critical Rate of Turned-On Current	$di/dt$	$V_D=2/3V_{DRM}$ , $I_{TM}=2 \cdot I_o$ , $T_j=125^\circ\text{C}$ $I_G=300\text{mA}$ , $di_G/dt=0.2\text{A}/\mu\text{s}$	100	$\text{A}/\mu\text{s}$
Peak Gate Power	$P_{GM}$		5	W
Average Gate Power	$P_{G(AV)}$		1	W
Peak Gate Current	$I_{GM}$		2	A
Peak Gate Voltage	$V_{GM}$		10	V
Peak Gate Reverse Voltage	$V_{RGM}$		5	V
Operating Junction Temperature Range	$T_{jw}$		-40 to +125	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$		-40 to +125	$^\circ\text{C}$
Isolation Voltage	Viso	Base Plate to Terminals, AC1min	2000	V
Mounting torque	Case mounting	Ftor	M6 Screw	N.m
	Terminals		M8 Screw	

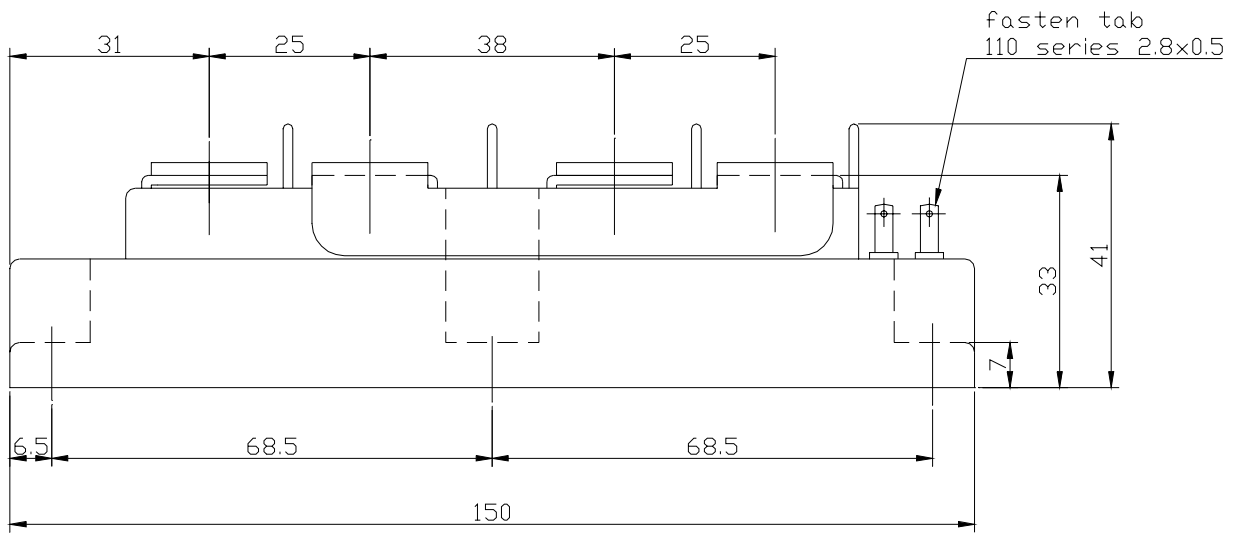
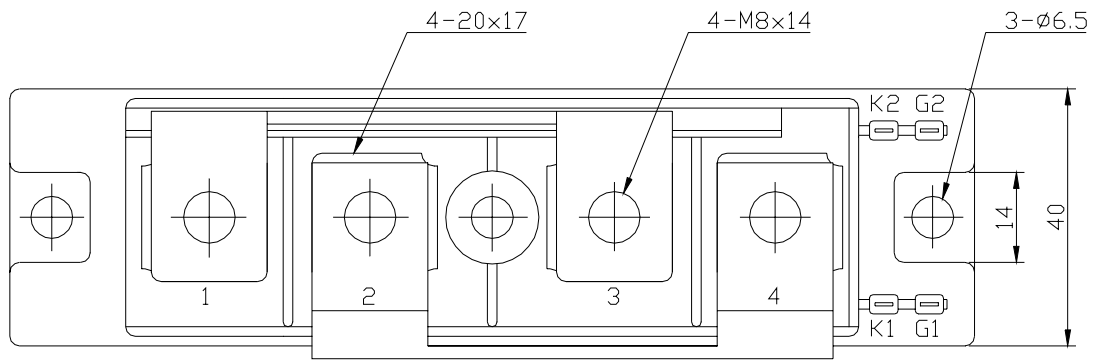
Value per 1 Arm

**Electrical • Thermal Characteristics**

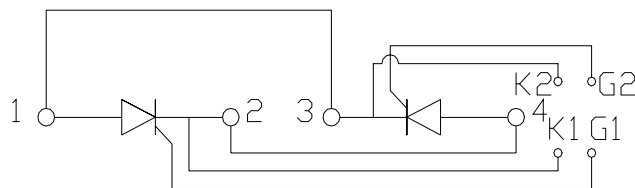
Characteristics	Symbol	Test Conditions	Maximum Value.			Unit
			Min.	Typ.	Max.	
Peak Off-State Current	$I_{DM}$	$V_{DM} = V_{DRM}, T_j = 125^\circ\text{C}$			30	mA
Peak Reverse Current	$I_{RM}$	$V_{RM} = V_{RRM}, T_j = 125^\circ\text{C}$			30	mA
Peak Forward Voltage	$V_{TM}$	$I_{TM} = 600\text{A}, T_j = 25^\circ\text{C}$			1.34	V
Gate Current to Trigger	$I_{GT}$	$V_D = 6\text{V}, I_T = 1\text{A}$	$T_j = -40^\circ\text{C}$		300	mA
			$T_j = 25^\circ\text{C}$		150	
			$T_j = 125^\circ\text{C}$		80	
Gate Voltage to Trigger	$V_{GT}$	$V_D = 6\text{V}, I_T = 1\text{A}$	$T_j = -40^\circ\text{C}$		5	V
			$T_j = 25^\circ\text{C}$		3	
			$T_j = 125^\circ\text{C}$		2	
Gate Non-Trigger Voltage	$V_{GD}$	$V_D = 2/3V_{DRM}, T_j = 125^\circ\text{C}$	0.25			V
Critical Rate of Rise of Off-State Voltage	dv/dt	$V_D = 2/3V_{DRM}, T_j = 125^\circ\text{C}$	500			V/ $\mu\text{s}$
Turn-Off Time	tq	$I_{TM} = I_O, V_D = 2/3V_{DRM}$ $dv/dt = 20\text{V}/\mu\text{s}, V_R = 100\text{V}$ $-di/dt = 20\text{A}/\mu\text{s}, T_j = 125^\circ\text{C}$		100		$\mu\text{s}$
Turn-On Time	tgt	$V_D = 2/3V_{DRM}, T_j = 125^\circ\text{C}$ $I_G = 300\text{mA}, di_G/dt = 0.2\text{A}/\mu\text{s}$		6		$\mu\text{s}$
Delay Time	td			2		$\mu\text{s}$
Rise Time	tr			4		$\mu\text{s}$
Latching Current	$I_L$	$T_j = 25^\circ\text{C}$		100		mA
Holding Current	$I_H$	$T_j = 25^\circ\text{C}$		60		
Thermal Resistance	Rth(j-c)	Junction to Case			0.23	$^\circ\text{C}/\text{W}$
	Rth(c-f)	Base Plate to Heat Sink with Thermal Compound			0.1	

Value Per 1Arm

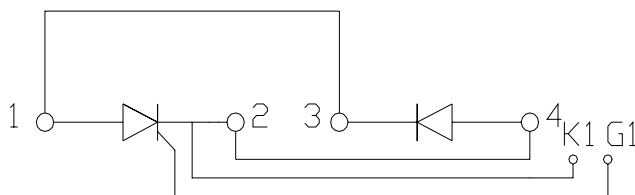
PAT/PAH2008 OUTLINE DRAWING (Dimensions in mm)



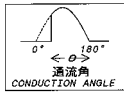
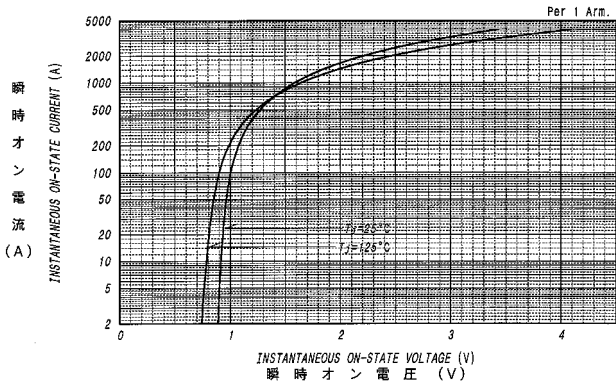
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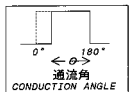
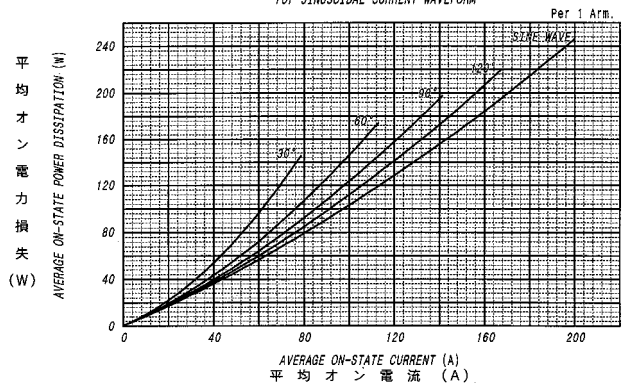
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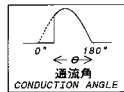
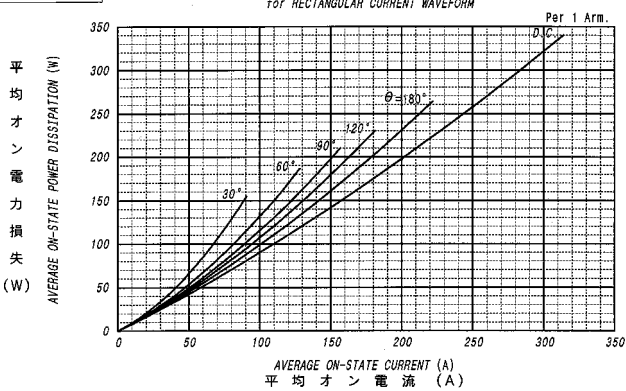
オン電圧特性  
ON-STATE CURRENT VS. VOLTAGE



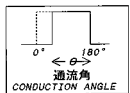
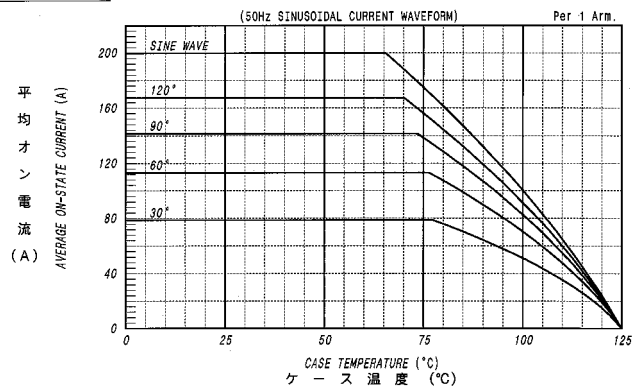
平均オン電力損失特性  
AVERAGE ON-STATE POWER DISSIPATION



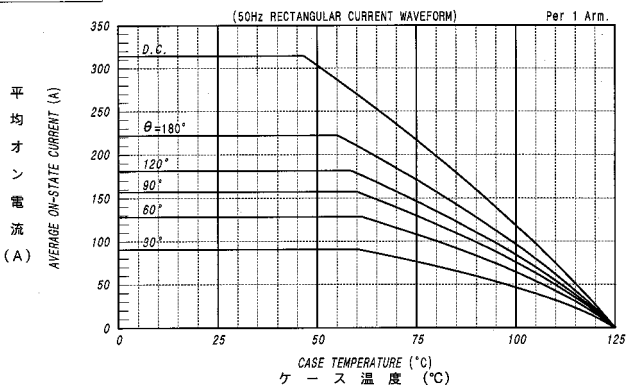
平均オン電力損失特性  
AVERAGE ON-STATE POWER DISSIPATION



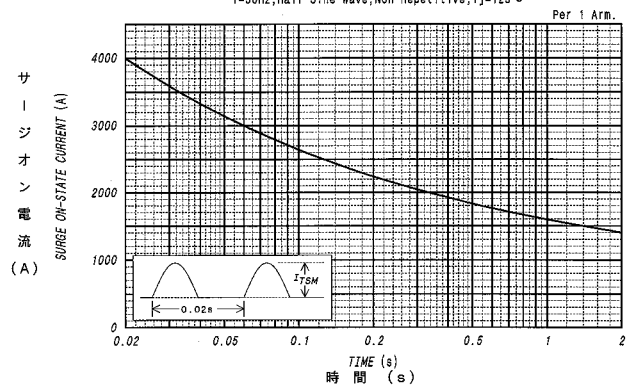
平均オン電流 - ケース温度定格  
AVERAGE ON-STATE CURRENT VS. CASE TEMPERATURE



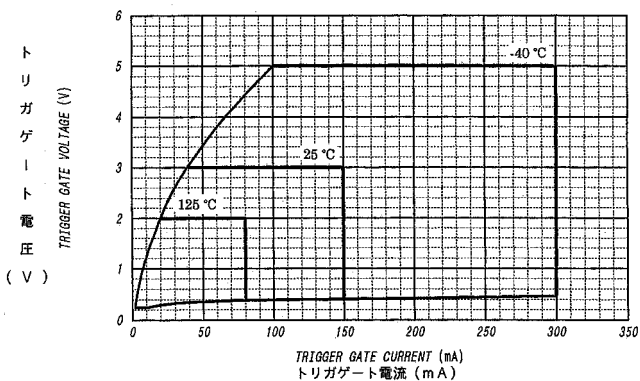
平均オン電流 - ケース温度定格  
AVERAGE ON-STATE CURRENT VS. CASE TEMPERATURE



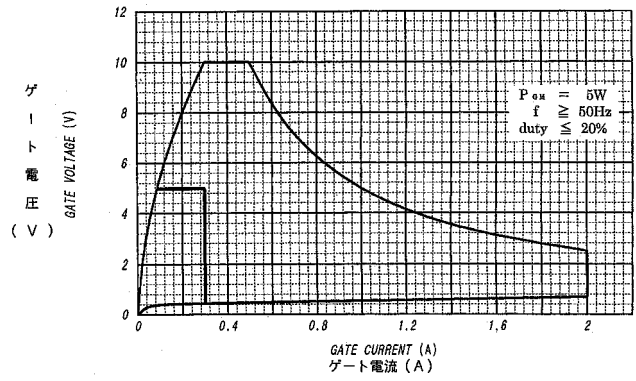
サージオン電流定格  
SURGE CURRENT RATINGS



ゲート特性  
GATE CHARACTERISTICS



ゲート定格  
GATE RATINGS



過渡熱抵抗特性  
MAXIMUM TRANSIENT THERMAL IMPEDANCE

Junction to Case

Per 1 Arm.

