CMOS 4-BIT MICROCONTROLLER

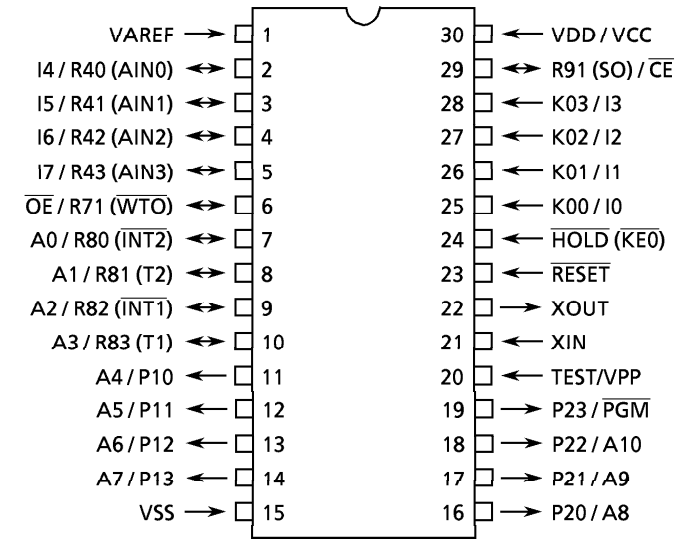
TMP47P242VN

The 47P242V is the system evaluation LSI of 47C242B with 16K bits one-time PROM. The 47P242V programs / verifies using an adapter socket to connect with PROM programmer, as it is in TMM2764AD.
In addition, the 47P242V and the 47C242B are pin compatible. The 47P242V operates as the same as the 47C242B by programming to the internal PROM.

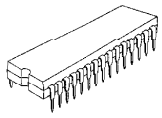
PART No.	EPROM	RAM	PACKAGE	ADAPTER SOCKET
TMP47P242VN	OTP 2048 × 8-bit	128 × 4-bit	SDIP30-P-400-1.78	BM1124

PIN ASSIGNMENT (TOP VIEW)

SDIP30-P-400-1.78



SDIP30-P-400-1.78



TMP47P242VN

PIN FUNCTION

The 47P242V has MCU mode and PROM mode.

(1) MCU mode

The 47C242B and the 47P242V are pin compatible (TEST pin for out-going test. Be fixed to low level).

(2) PROM mode

PIN NAME	INPUT / OUTPUT	FUNCTIONS	PIN NAME(MCU mode)
A10	INPUT	Address inputs	P22
A9			P21
A8			P20
A7 to A4			P13 to P10
A3 to A0			R83 to R80
I7 to I4	I/O	Data outputs (Inputs)	R43 to R40
I3 to I0			K03 to K00
$\overline{PGM}$	INPUT	Program control input	P23
$\overline{CE}$		Chip Enable input	R91
$\overline{OE}$		Output Enable input	R71
VPP	Power supply	+ 12.5 V / 5 V (Program supply voltage)	TEST
VCC		+ 5 V	VDD
VSS		0 V	VSS
$\overline{RESET}$	INPUT	PROM mode setting pin. Be fixed to low level.	
$\overline{HOLD}$	INPUT		
XIN	INPUT	Resonator connecting pin.	
XOUT	OUTPUT		
VAREF	Power supply	Be fixed to low level.	

OPERATIONAL DESCRIPTION

The following is an explanation of hardware configuration and operation in relation to the 47P242V. The 47P242V is the same as the 47C242B except that an OTP is used instead of a built-in mask ROM.

1. OPERATION mode

The 47P242V has an MCU mode and a PROM mode.

1.1 MCU mode

The MCU mode is set by fixing the TEST/VPP pin at the "L" level. Operation in the MCU mode is the same as for the 47C242B, except that the TEST/VPP pin does not have built in pull-down resistor and cannot be used open.

1.1.1 Program Memory

The program storage area is the same as for the 47C242B.

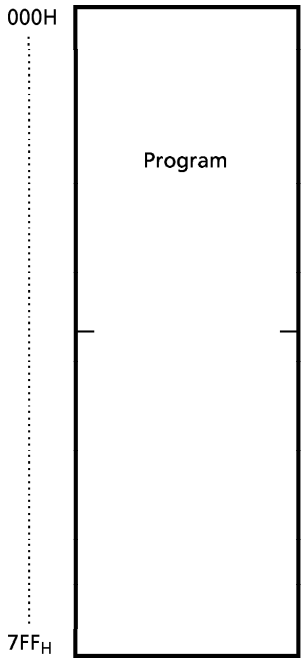


Figure 1-1. Program area

1.1.2 Data Memory

The 47P242V has 128 × 4-bit of data memory (RAM).

1.1.3 Input / Output Circuitry

(1) Control pins
This is the same as for the 47C242B except that there is no built-in pull-down resistance for the TEST pin.

(2) I/O Ports
The input / output circuit of the 47P242V is the same as I/O code SA of the 47C242B.
External resistance, for example, is required when using as evaluator of other I/O codes (SB, SC).

(a) Equivalent to IO code SB (b) Equivalent to IO code SC

Figure 1-2. I/O code and external circuitry

1.2 PROM mode

The PROM mode is set by setting the $\overline{\text{RESET}}$, $\overline{\text{HOLD}}$ pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification (A high-speed program mode is used set the ROM type the same as for the TMM 2764AD).

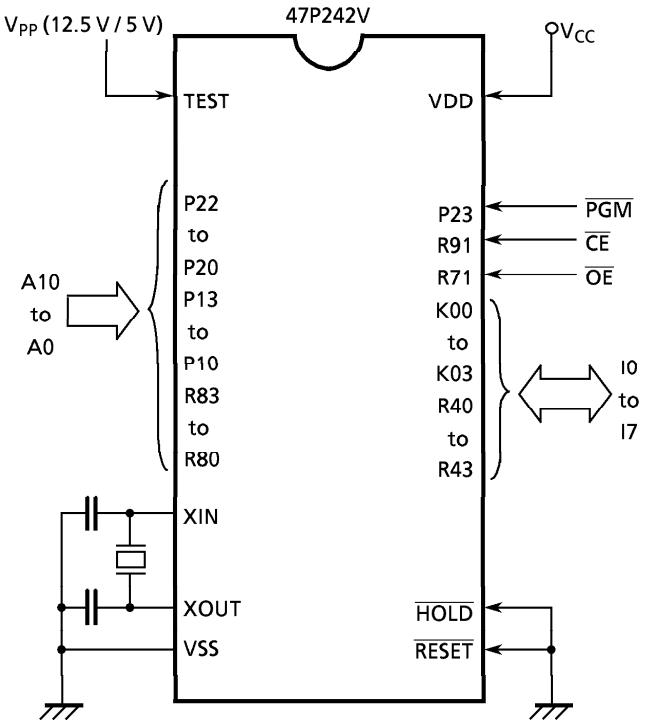


Figure 1-3. Setting for PROM mode

1.2.1 Programming

When writing a program, set a ROM type to 2764A (programming voltage : 12.5V).
Since the 47P242v has 2048 × 8 bit internal PROM (000 to $7FF_H$), set a stop address of a PROM writer to "$7FF_H$".

1.2.2 High Speed Programming Mode

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+ 12.5 V) is applied to the V_{PP} terminal with V_{CC} = 6 V and $\overline{PGM}$ = $V_{IH}4$.

The programming is achieved by applying a single low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC} = V_{PP} = 5 V.

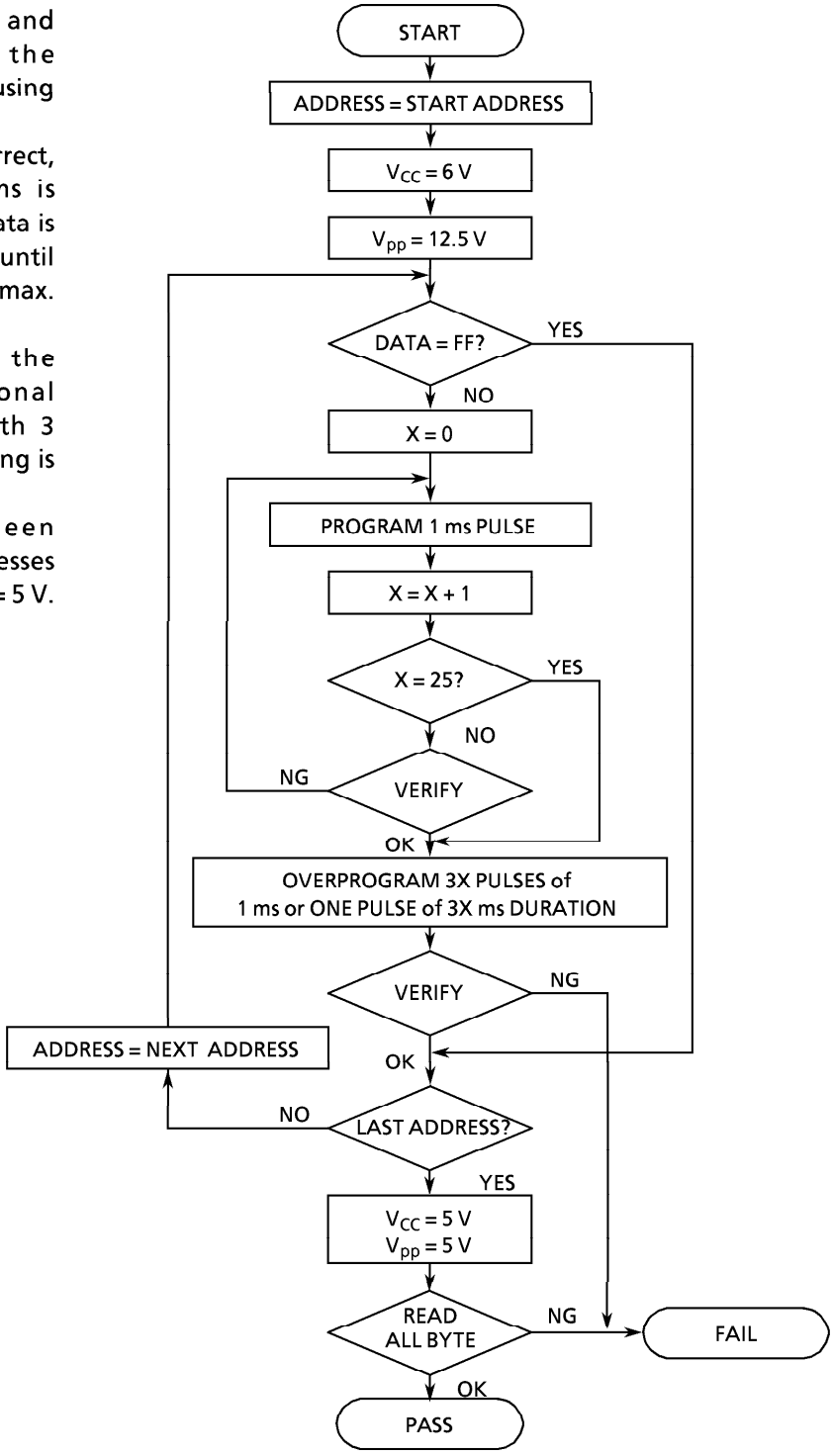


Figure 1-4. Flow Chart

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		– 0.3 to 7	V
Program Voltage	Vpp	TEST/VPP pin	– 0.3 to 14.0	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin	– 0.3 to V_{DD} + 0.3	
	V_{OUT2}	Ports P1, P2, R7 to R9	– 0.3 to 10	
	V_{OUT3}	Port R4 (Analog inputs)	– 0.3 to V_{DD} + 0.3	mA
Output Current (Per 1 pin)	I_{OUT1}	Ports P1, P2	30	
	I_{OUT2}	Port R7 to R9, R4	3.2	
Output Current (Total)	ΣI_{OUT1}	Ports P1, P2	120	mA
Power Dissipation [T_{opr} = 70 °C]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10 s)	°C
Storage Temperature	T_{stg}		– 55 to 125	°C
Operating Temperature	T_{opr}		– 30 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 V, T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	4.5	6.0	V
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.1$	
Clock Frequency	fc			0.4	4.2	MHz

Note. Input voltage V_{IH3}, V_{IL3} : in the HOLD mode

D.C. CHARACTERISTICS

(V_{SS} = 0 V, T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5 V, V_{IN} = 5.5 V / 0 V	—	—	± 2	μA
	I_{IN2}	Ports R (open drain)					
Low Input Current	I_{LO}	Ports R (push-pull)	VDD = 5.5 V, VIN = 0.4 V	—	—	– 2	mA
Input Resistance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Ports R (open drain)	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	—	—	2	μA
Output Low Voltage	V_{OL2}	Except XOUT, ports P	VDD = 4.5 V, IOL = 1.6 m A	—	—	0.4	V
Low Output Current	I_{OL1}	Ports P1, P2	V_{DD} = 4.5 V, V_{OL} = 1.0 V	—	20	—	mA
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5 V, fc = 4 MHz	—	3	6	mA
Supply Current (in the HOLD mode)	IDDH		V_{DD} = 5.5 V	—	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25 °C, V_{DD} = 5 V.

Note 2. Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. Supply Current I_{DD}, I_{DDH} ; V_{IN} = 5.3 V / 0.2 V
The K0 port is open when the input resistor is contained. The voltage applied to the R port is within the valid range.

A / D CONVERSION CHARACTERISTICS

(T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Reference Voltage	V_{AREF}		V_{DD} – 1.5	—	V_{DD}	V
Analog Reference Voltage Range	ΔV_{AREF}	V_{AREF} – V_{SS}	3.0	—	—	V
Analog Input Voltage	V_{AIN}		V_{SS}	—	V_{AREF}	V
Analog Supply current	I_{REF}		—	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 5.0 V, V_{SS} = 0.0 V V_{AREF} = 5.000V	—	—	± 1	LSB
Zero Point Error			—	—	± 1	
Full Scale Error			—	—	± 1	
Total Error			—	—	± 2	

A. C. CHARACTERISTICS

(V_{SS} = 0 V, V_{DD} = 4.5 to 6.0 V, T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		1.9	—	20	μs
High level Clock pulse Width	t_{WCH}	External clock mode	80	—	—	ns
Low level Clock pulse Width	t_{WCL}					
A/D Sampling Time	t_{AIN}	fc = 4 MHz	—	4	—	μs

RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0 V, V_{DD} = 4.5 to 6.0 V, T_{opr} = – 30 to 70 °C)

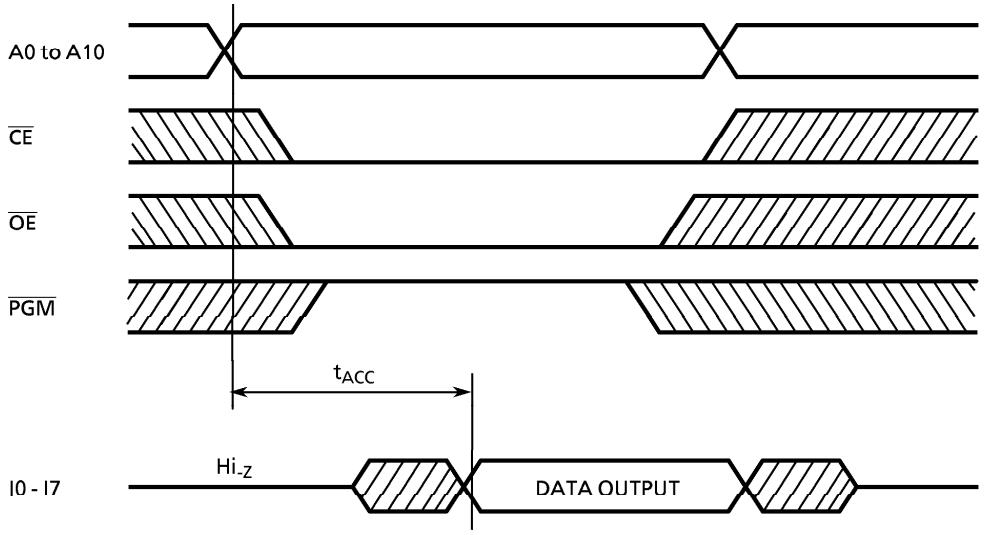
Recommended oscillating conditions of the 47P242V are equal to the 47C242B's.

DC/AC CHARACTERISTICS

(V_{SS} = 0 V)

(1) Read Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Output Level High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Output Level Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
Programming Voltage	V_{PP}					
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25 V	–	–	350	ns



(2) High Speed Programming Operation

PARAMETER	SYBOL	CONDITION	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
V_{PP} Power Supply Voltage	V_{PP}		12.0	12.50	13.0	V
Programming Pulse Width	t_{PW}	V_{CC} = 6.0 ± 0.25 V	0.95	1.0	1.05	ms