

131,072-word by 9-bit High-Speed Synchronous Static RAM

Description

The CXK77910ATM/AYM are high-speed CMOS synchronous static RAMs with common I/O pins, organized as 131,072-word-by-9-bit. These synchronous SRAMs integrate input registers, high speed SRAM and output registers onto a single monolithic IC. All input signals are latched at the positive edge of an external clock (CLK). The RAM data from the previous cycle is presented at the positive edge of the subsequent clock cycle. Write operation is initiated by the positive edge of CLK and is internally self-timed. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals. 100MHz operation is obtained from a single 5V power supply.

Function

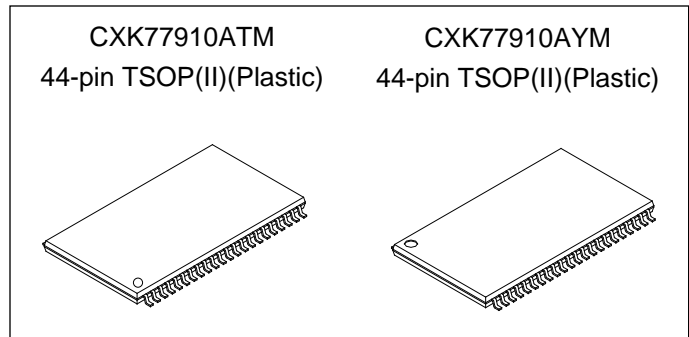
There are three possible user transactions with the STRAM — read operation, write operation and deselect operation.

The read operation requires $\overline{WE} = \text{"HIGH"}$ and $\overline{OE} = \text{"LOW"}$ on the positive edge of CLK.

The memory location pointed to by the contents of the Address registers is read internally and the contents of the location are captured in the Data-out registers on the next positive edge of CLK. The state of Data-out will reflect the contents of the Data-out registers.

The write operation requires $CE = \overline{WE} = \text{"LOW"}$ on the positive edge of CLK. The memory location pointed to by the contents of the Address registers is written with the contents of the Data-in registers. The write operation is entirely self-timed, eliminating critical timing edges.

The deselect cycle requires $CE = \text{"HIGH"}$ or $\overline{OE} = \overline{WE} = \text{"HIGH"}$ on the positive edge of CLK. Write operation and internal read operation are disabled during the clock



cycle. The data outputs are forced to a high impedance state during the next clock cycle. During the deselect cycle by $\overline{CE} = \text{"HIGH"}$, STRAM turns to power down mode.

Structure

Silicon gate CMOS IC

Features

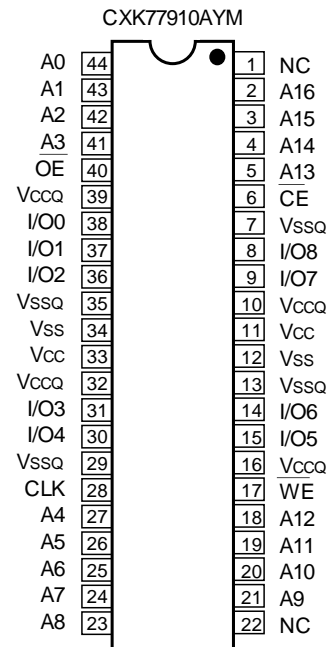
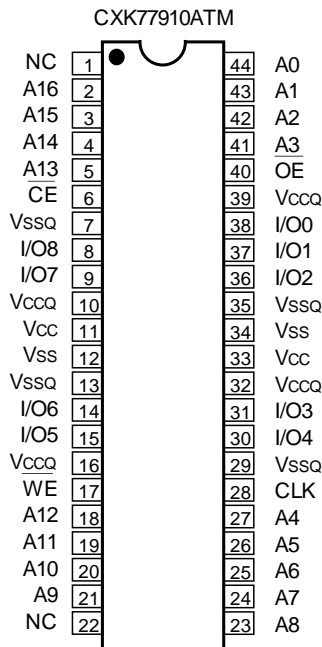
- Fast cycle time:

	(Cycle)	(Frequency)
CXK77910ATM/AYM-10	10.0ns	100MHz
CXK77910ATM/AYM-12	12.5ns	80MHz
- Fast clock to data valid

CXK77910ATM/AYM-10	5.5ns
CXK77910ATM/AYM-12	6.5ns
- High speed, low power consumption
- Single +5V power supply: $5V \pm 5\%$
- Separate output power supply: 3.15V to 5.25V
- Inputs and outputs are TTL compatible (3.3V I/O compatible)
- Common data input and output
- All inputs and outputs are registered on a single clock edge
- Self-timed write cycle
- Package line-up: 400mil 44 pin TSOP II with 0.8mm pitch

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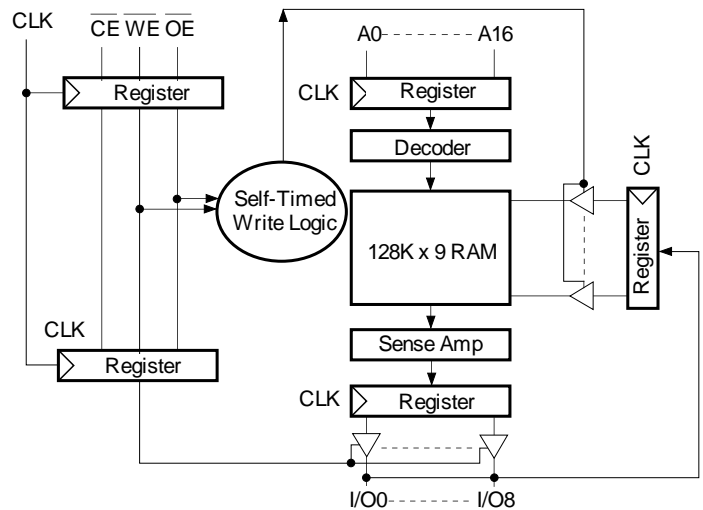
Pin Configurations (Top View)



Pin Description (1)

Symbol	Description
A0 to A16	Address input
I/O0 to I/O8	Data input/output
CLK	Clock
CE	Chip enable input
WE	Write enable input
OE	Output enable input
Vccq	Output power supply
Vcc	+5V power supply
Vss/Vssq	Ground

Block Diagram



Pin Description (2)

CLK (Clock, Positive Edge Triggered)

All timing is controlled by the rising or positive edge of CLK. All synchronous input and output signals are registered on the positive edge of CLK with set-up and hold times referenced to that edge. Since only one edge of CLK is referenced, the duty cycle of CLK is not critical.

A0 to A16 (Address)

The Address inputs are decoded on-chip to select one of 131,072 words. The state of the Address inputs is registered into the Address register on the positive edge of CLK. The Address inputs must be valid during every positive edge with all set-up and hold times referenced to that edge.

I/O0 to I/O8 (Data Input/Output)

I/O terminals are three-state and data input/output common. The state is defined by the Control block (refer to the truth table on page 4).

The data inputs for write operation must be valid during every positive edge of CLK with all set-up and hold times referenced to that edge. The data outputs are triggered by the positive edge of CLK and the contents of the Output-Registers are presented.

$\overline{\text{WE}}$ (Synchronous Write Enable, Active Low)

$\overline{\text{WE}}$ is used to indicate whether a read or write operation is to be performed. $\overline{\text{WE}}$ is "LOW" to perform a write operation. $\overline{\text{WE}}$ is registered on every positive edge of CLK with set-up and hold times referenced to that edge. The internal timing required to store data into the memory array is self-timed.

$\overline{\text{CE}}$ (Synchronous Chip Enable, Active Low)

$\overline{\text{CE}}$ is used to select the Synchronous SRAM when low (or deselect when high). When selected, the Synchronous SRAM will perform a read or write operation (refer to the truth table on page 4). The state of $\overline{\text{CE}}$ is registered on every positive edge of CLK with set-up and hold times referenced to that edge.

$\overline{\text{OE}}$ (Synchronous Output Enable, Active Low)

$\overline{\text{OE}}$ is used to indicate that a read operation is to be performed. If the Synchronous SRAM is selected, the $\overline{\text{OE}}$ is low to perform a read operation (refer to the truth table on page 4). The state of $\overline{\text{OE}}$ is registered on every positive edge of CLK with set-up and hold times referenced to that edge.

Absolute Maximum Ratings

(Ta = +25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 to V _{CC} +0.5	V
Output voltage	V _O	-0.5 to V _{CC} +0.5	V
Allowable power dissipation	P _D	1	W
Operating temperature	T _{opr}	0 to 70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature • time	T _{solder}	235 • 10	°C • sec

Truth Table

CLK	$\overline{\text{CE}}$ (tn)	$\overline{\text{WE}}$ (tn)	$\overline{\text{OE}}$ (tn)	Mode	I/O to 8	V _{CC} Current
	H	X	X	Deselect	Hi-Z	I _{SB}
	L	H	H	Read	Hi-Z	I _{CC}
	L	H	L	Read	Data out*	I _{CC}
	L	L	X	Write	Data in	I _{CC}

X: "H" or "L"

*Data come out on the next positive edge of CLK.

DC Recommended Operating Conditions

(Ta = +25°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.75	5.0	5.25	V
Output supply voltage	V _{CCQ}	3.15	—	5.25	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3*	—	0.8	V

*V_{IL} = -3.0V min. for pulse width less than 20ns.

Electrical Characteristics

DC and Operating Characteristics

(V_{CC} = 5V ± 5%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	-1	1	μA
Output leakage current	I _{LO}	V _O = GND to V _{CC} OE = V _{IH}	-1	1	
Average operating current	I _{CC}	Duty = 100% I _{OUT} = 0mA	—	150	mA
Standby current	I _{SB}	CE ≥ V _{IH} Cycle = Min. Duty = 100%	—	130	
Output high voltage	V _{OH}	I _{OH} = -2.0mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 4.0mA	—	0.4	

I/O Capacitance

(Ta = +25°C, f = 1MHz)

Item	Symbol	Test Conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	5	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

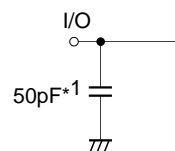
Note) These parameters are sampled and are not 100% tested.

AC Characteristics

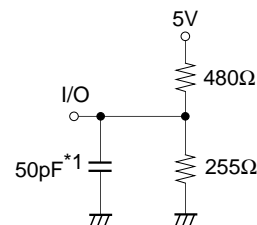
- **AC Test Conditions** (V_{CC} = 5V ±5%, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	tr = 3ns
Input fall time	tf = 3ns
Input/output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2) *2



*1. Including scope and jig capacitance.

*2. For t_{CKHQZ}, t_{CKHQX}.

Fig. 1

• Read Cycle ($\overline{WE} = "H"$)

Item	Symbol	-10		-12		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	tCKHCKH	10	—	12.5	—	ns
Clock high pulse width	tCKHCKL	3.5	—	4	—	
Clock low pulse width	tCKLCKH	3.5	—	4	—	
Clock to data valid	tCKHQV	—	5.5	—	6.5	
Address setup to clock high	tAVCKH	2.5	—	2.5	—	
Address hold from clock high	tCKHAX	0.5	—	0.5	—	
Chip enable setup to clock high	tCEVCKH	2.5	—	2.5	—	
Chip enable hold from clock high	tCKHCEX	0.5	—	0.5	—	
Output enable setup to clock high	tOEVCKH	2.5	—	2.5	—	
Output enable hold from clock high	tCKHOEX	0.5	—	0.5	—	
Clock high to output low-Z	tCKHQX*	1.5	—	1.5	—	
Clock high to output high-Z	tCKHQZ*	—	4.5	—	5	

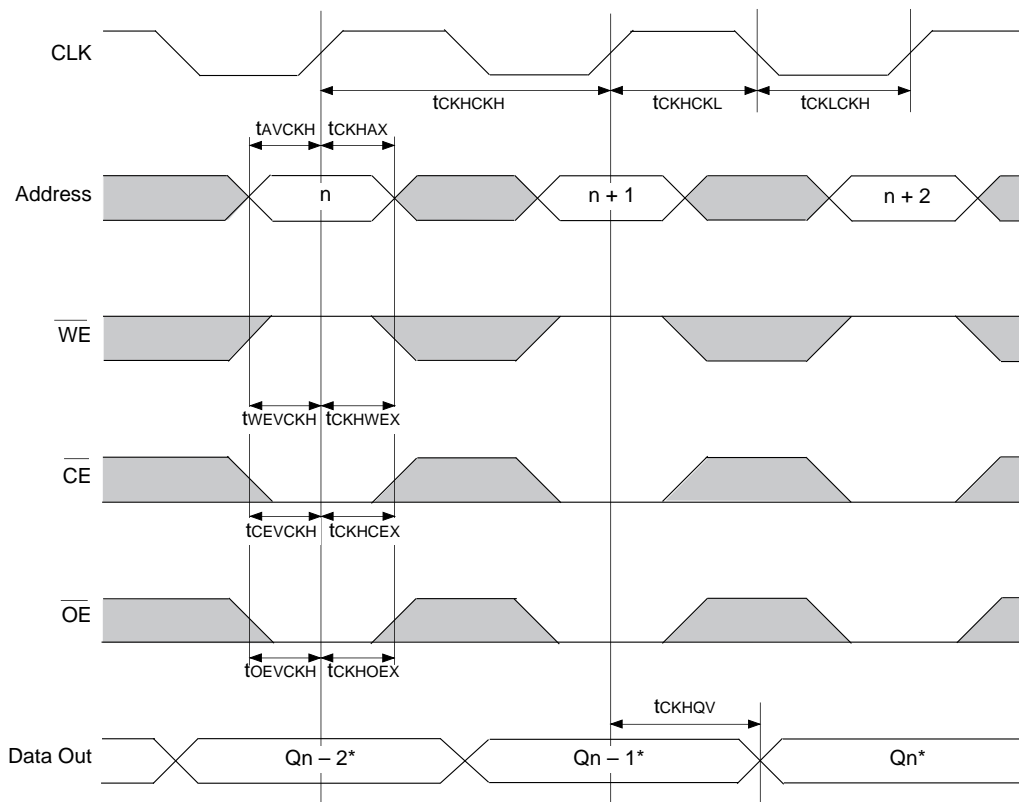
*Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2). This parameter is sampled and is not 100% tested.

• Write Cycle

Item	Symbol	-10		-12		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	tCKHCKH	10	—	12.5	—	ns
Clock high pulse width	tCKHCKL	3.5	—	4	—	
Clock low pulse width	tCKLCKH	3.5	—	4	—	
Address setup to clock high	tAVCKH	2.5	—	2.5	—	
Address hold from clock high	tCKHAX	0.5	—	0.5	—	
Chip enable setup to clock high	tCEVCKH	2.5	—	2.5	—	
Chip enable hold from clock high	tCKHCEX	0.5	—	0.5	—	
Write enable setup to clock high	tWEVCKH	2.5	—	2.5	—	
Write enable hold from clock high	tCKHWEX	0.5	—	0.5	—	
Input data setup to clock high	tDVCKH	2.5	—	2.5	—	
Input data hold from clock high	tCKHDX	0.5	—	0.5	—	

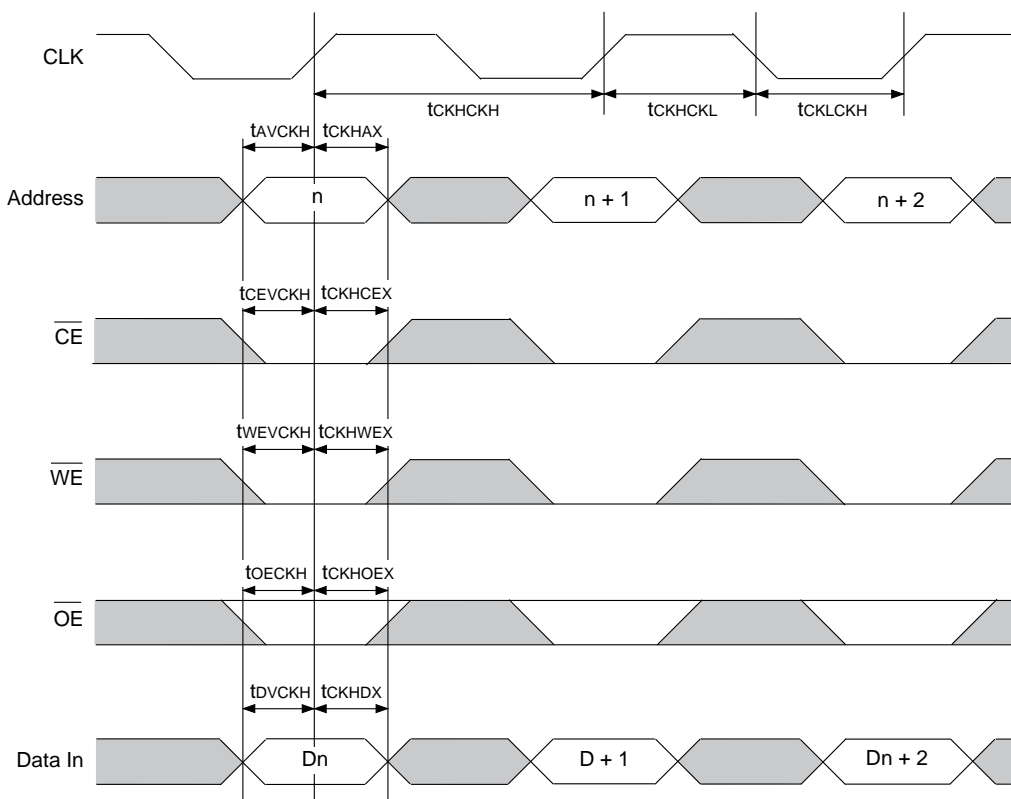
Timing Waveform

• Read Cycle

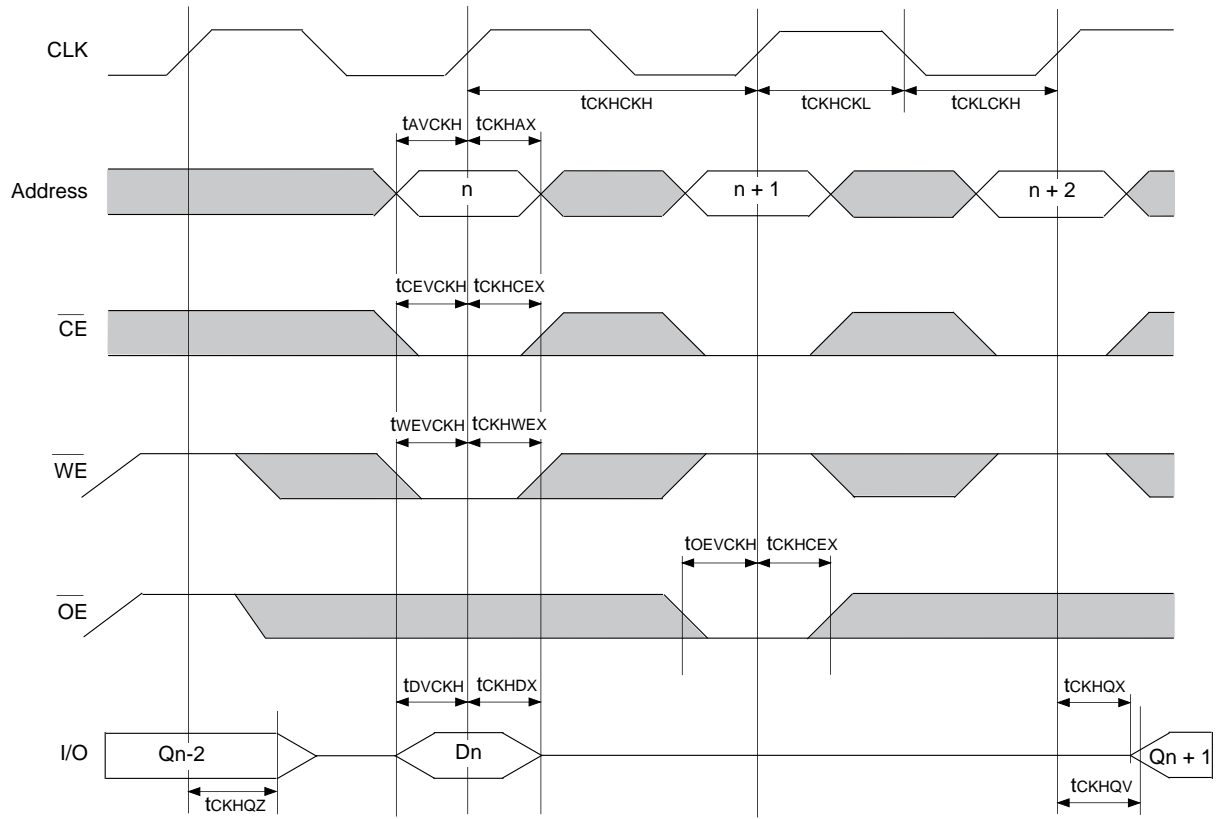


*Valid data from CLK high is the data from the previous cycle

• Write Cycle: $\overline{OE} = V_{IH}$ or V_{IL}

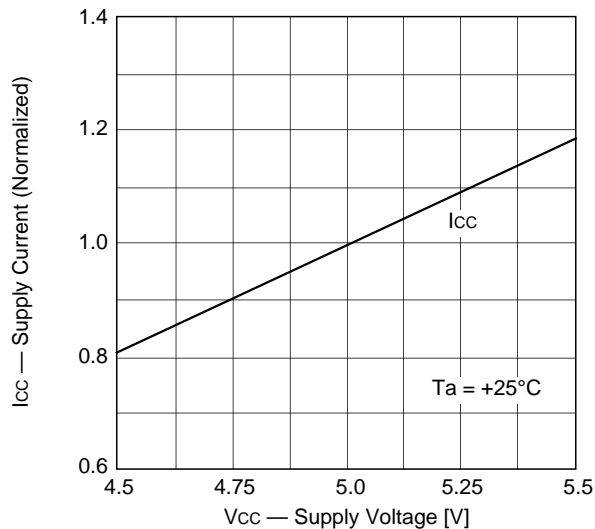


• Read/Write Cycle

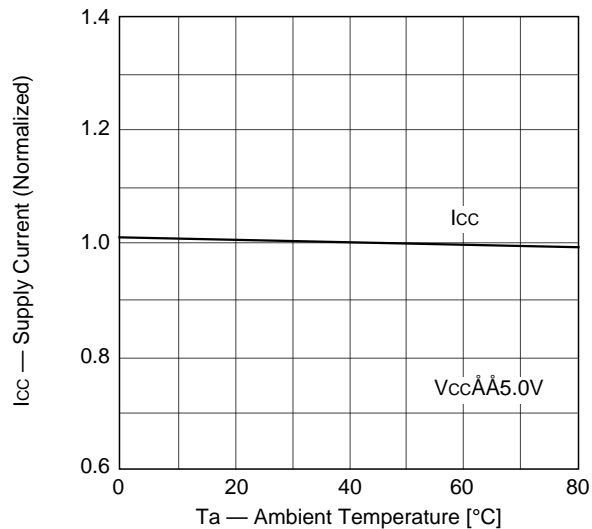


Example of Representative Characteristics

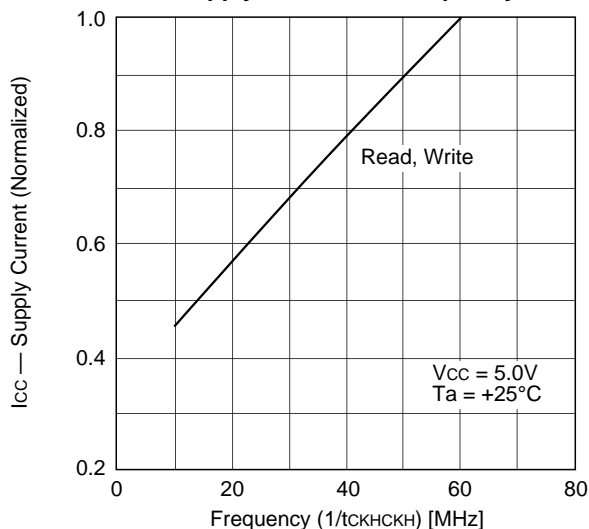
Supply Current vs. Supply Voltage



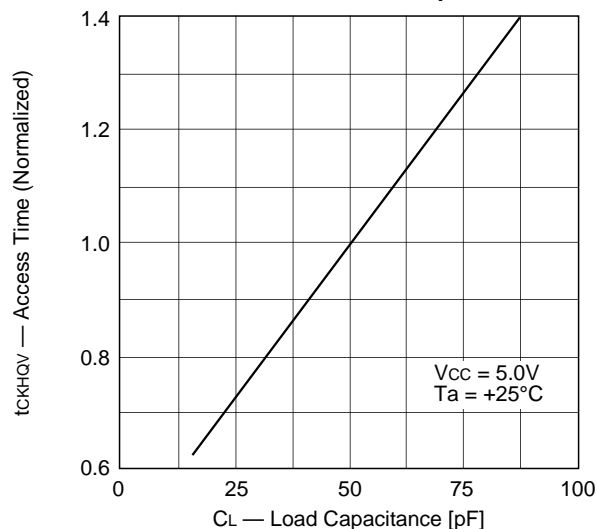
Supply Current vs. Ambient Temperature



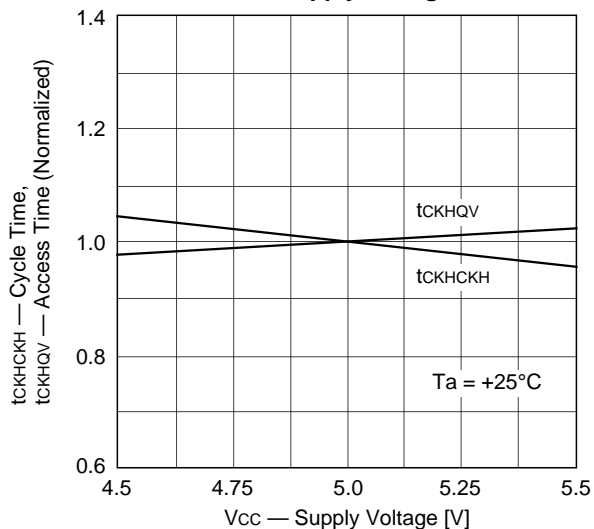
Supply Current vs. Frequency



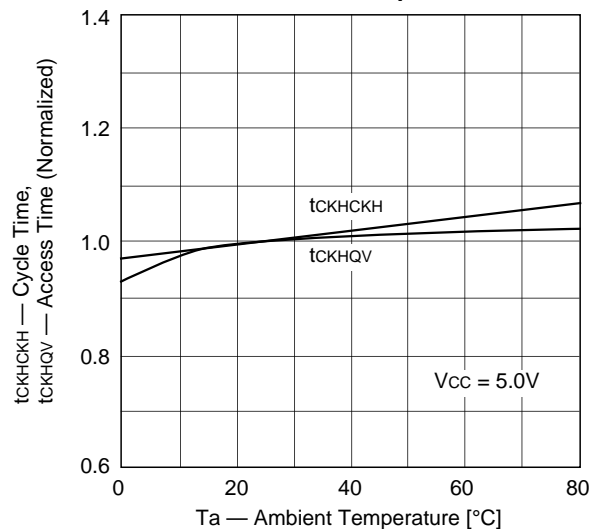
Access Time vs. Load Capacitance



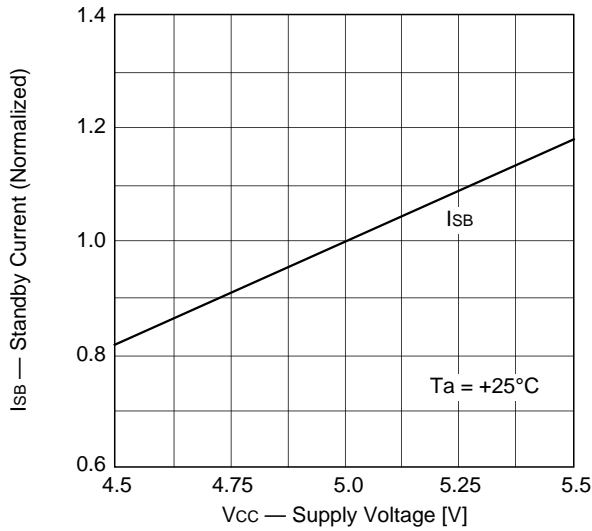
Cycle Time (Minimum)/Access Time vs. Supply Voltage



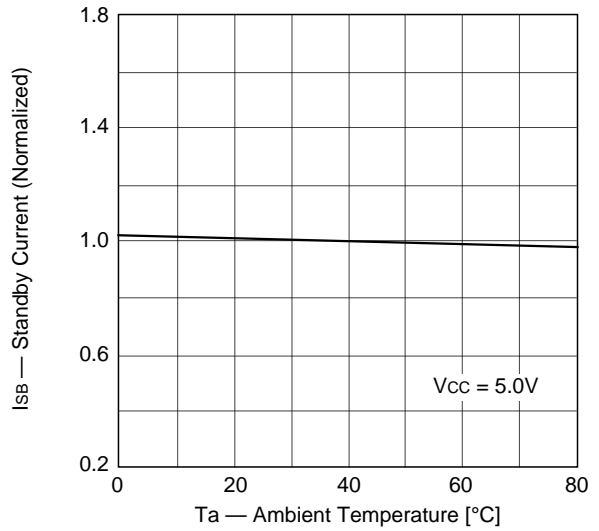
Cycle Time (Minimum)/Access Time vs. Ambient Temperature



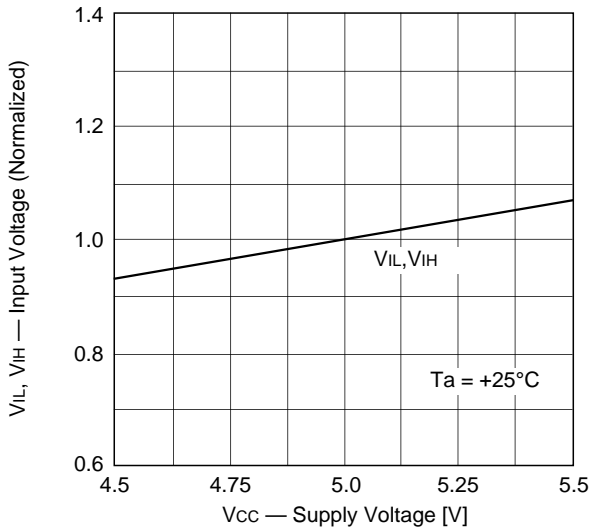
Standby Current vs. Supply Voltage



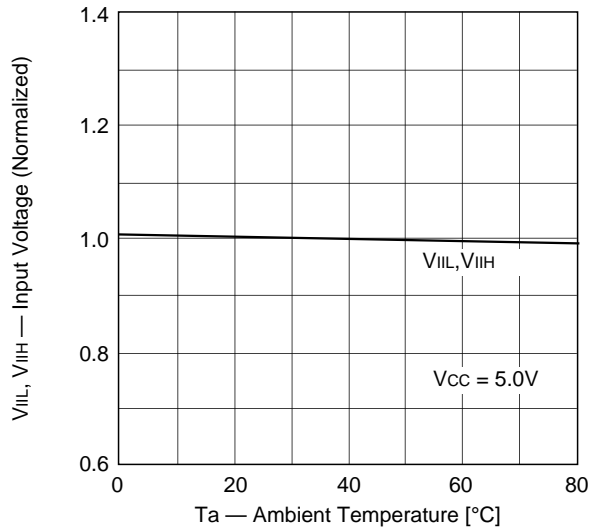
Standby Current vs. Ambient Temperature



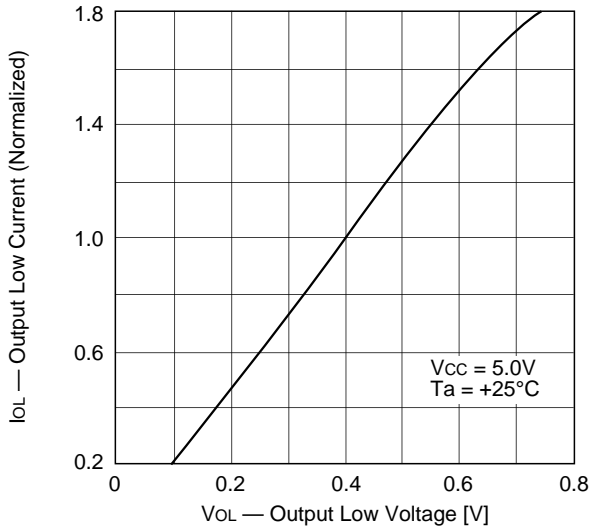
Input Voltage Level vs. Supply Voltage



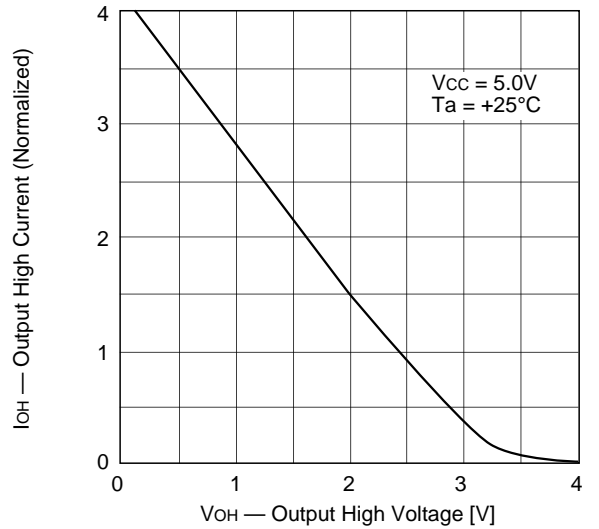
Input Voltage Level vs. Ambient Temperature



Output Low Current vs. Output Low Voltage



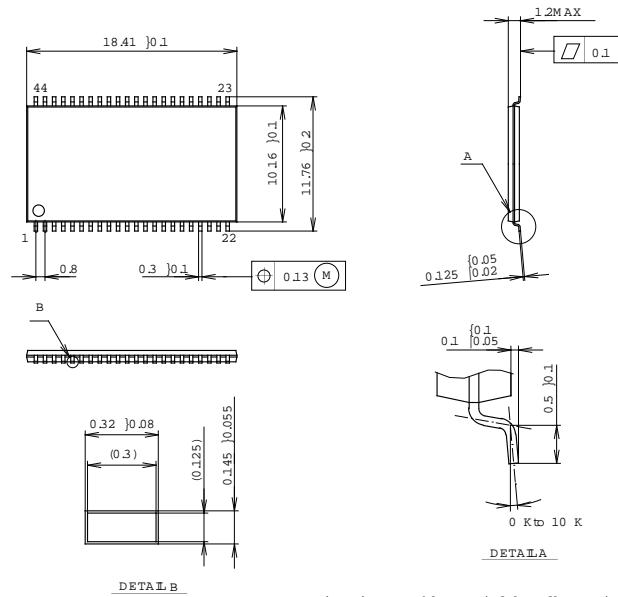
Output High Current vs. Output High Voltage



Package Outline
CXK77910ATM

Unit : mm

44P N TSOP (II) (PLASTIC) 400m il



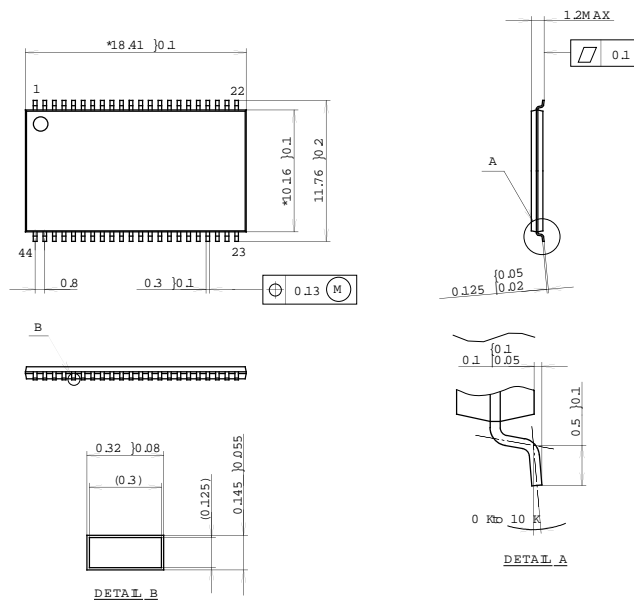
PACKAGE STRUCTURE

SONY CODE	TSOP (II)-44P-L01
ERJ CODE	TSOP (II)044P-0400-A
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.5g

CXK77910AYM

44P N TSOP (II) (PLASTIC) 400m il



PACKAGE STRUCTURE

SONY CODE	TSOP (II)-44P-L01R
ERJ CODE	TSOP (II)044P-0400-B
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.5g