

SANYO	No.1802C	LC6514B
		SINGLE-CHIP 4-BIT MICROCOMPUTER (LOW-THRESHOLD INPUT, ON-CHIP FLT DRIVER)

The LC6514B is a microcomputer with FLT drivers. It is identical with the LC6510C in the internal architecture and instruction set. Since the normal/low-threshold level of input port A can be selected by option and the on-chip pull-down resistor can be bitwise connected to the FLT driver by option, the number of external parts used in the user equipment can be minimized, reducing the cost considerably.

(Note) The LC6514B heretofore in use has been improved by changing the value of the pull-down resistor to be contained in FLT drivers as shown below. When using the LC6514B, fully check that the new resistor value meets your application specifications.

		New resistor value			Old resistor value			
		min	typ	max	min	typ	max	
"L"-level output current	I_{OL}	0.190	0.362	0.760	0.108	0.304	0.543	mA
(Output pull-down resistance)	(R_{PD})	(200)	(105)	(50)	(350)	(125)	(70)	($k\Omega$)

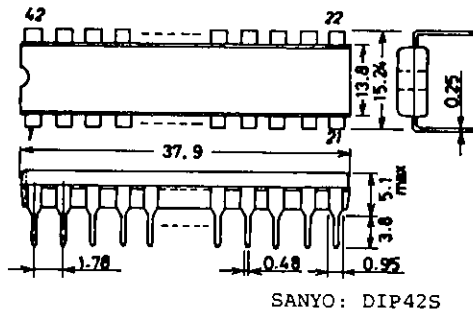
Features

- Low power dissipation
- ROM capacity: 4096 x 8 bits
- RAM capacity: 256 x 4 bits
- Subroutine stack: 8 levels (common with interrupt)
- On-chip OSC circuit
 - CR OSC: 800kHz typ.
 - Ceramic OSC: 400kHz, 800kHz, 1000kHz
 - External input: 1290kHz max.
- Power-down by 2 standby modes
 - HALT mode: Power dissipation saving by program standby during normal operation
 - HOLD mode: Power supply backup during power failure
- Input/output ports
 - Input: 4 bits x 1 port
3 bits x 1 port
 - Input/output: 4 bits x 2 ports
 - Output: 4 bits x 4 ports
2 bits x 1 port
- Interrupt
 - External interrupt: 1
 - Internal timer interrupt: 1
- On-chip 4-bit prescaler and 8-bit program timer
- Instruction cycle time: 3.1 μ s (at 1290kHz)
- Supply voltage
 - Normal operation: 4.0 to 6.0V
 - Memory hold: 1.8 to 6.0V
- Instruction set common to the LC6502, LC6505 (BANK instruction added)

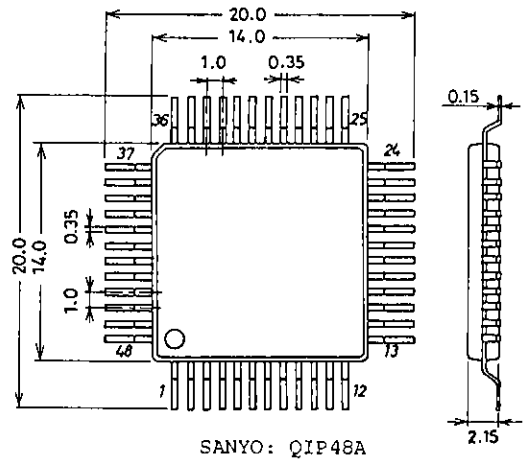
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- Package: DIP42S (shrink)
QIP48

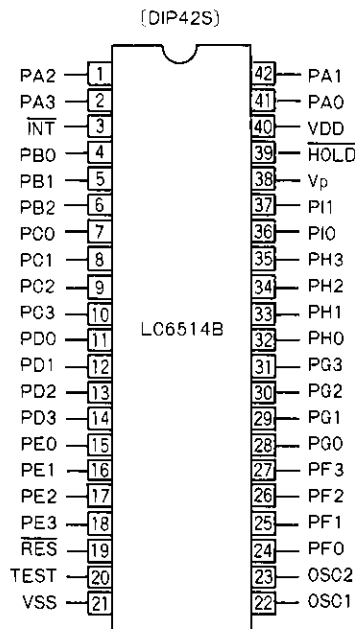
Package Dimensions 3025B-D42SIC (unit: mm)



Package Dimensions 3052A-Q48AIC (unit: mm)



Pin Assignment



Pin Name

OSC1, OSC2: C, R or ceramic resonator for system OSC

INT: Interrupt

RES: Reset

HOLD: Hold

PA0 to 3: Input port A0 to 3

PB0 to 2: Input port B0 to 2

PC0 to 3: Input/output common port C0 to 3

PD0 to 3: Input/output common port D0 to 3

PE0 to 3: Output port E0 to 3

PF0 to 3: Output port F0 to 3

PG0 to 3: Output port G0 to 3

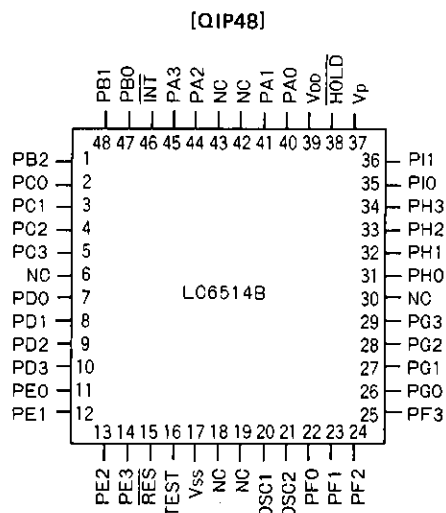
PH0 to 3: Output port H0 to 3

PI0, 1: Output port I0, 1

TEST: Test

Vp: Power supply for high-voltage port pull-down resistor

With High-voltage driver



When mounting the QIP package version on the board, do not dip it in solder.

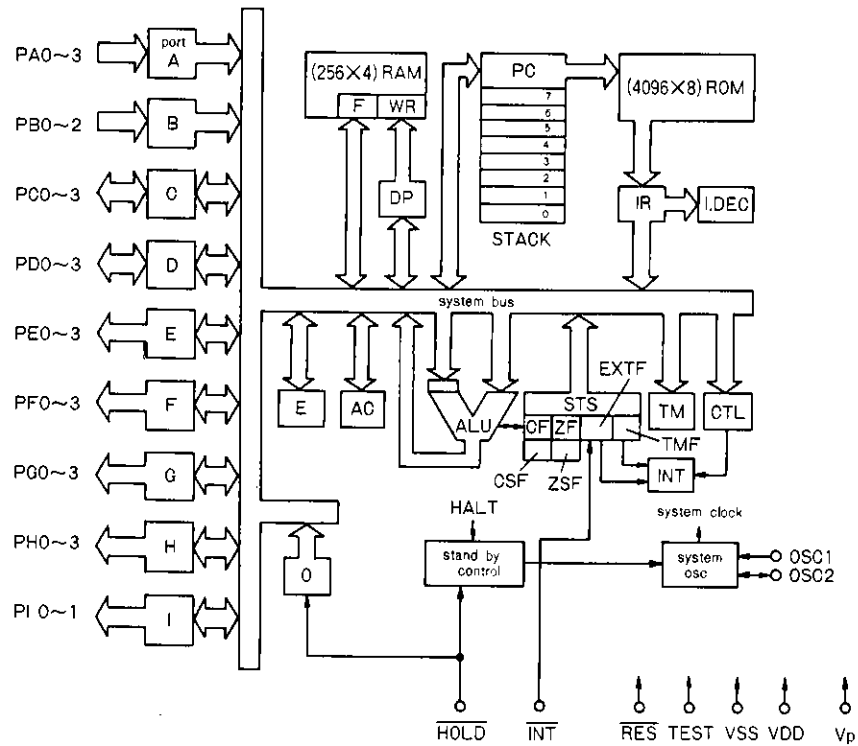
NC pin: No connection

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Pin Description

Pin Name	Input/ Output	Function
INT	Input	Interrupt request input pin.
HOLD	Input	HOLD mode request input pin (Differs from the LC6502/05 in function.) Capable of being used as a general-purpose single-bit input port unless the standby mode is used.
RES	Input	Reset input pin.
PA0 to 3	Input	Input port A ₀ to A ₃ (Normal voltage). Capable of 4-bit input and single-bit decision for branch. Used also for HALT mode release request input. Low threshold input for 4 bits selectable by option.
PB0 to 2	Input	Input port B ₀ to B ₂ (Normal voltage) Capable of 3-bit input and single-bit decision for branch.
PC0 to 3	Input/ output	Input/output common port C ₀ to C ₃ (Normal voltage). Capable of 4-bit input and single-bit decision for branch during input. Capable of 4-bit output and single-bit set/reset during output.
PD0 to 3	Input/ output	Input/output common port D ₀ to D ₃ (Normal voltage). Capable of 4-bit input and single-bit decision for branch during input. Capable of 4-bit output and single-bit set/reset during output.
PE0 to 3	Output	Output port E ₀ to E ₃ (with high-voltage segment driver). Capable of 4-bit output and single-bit set/reset. Capable of 4-bit input of output latch contents and single-bit decision of output latch for branch. Use/nonuse of pull-down resistor bitwise selectable by option.
PF0 to 3	Output	Output port F ₀ to F ₃ (with high-voltage segment driver). Capable of 4-bit output and single-bit set/reset. Capable of 4-bit input of output latch contents and single-bit decision of output latch for branch. Use/nonuse of pull-down resistor bitwise selectable by option.
PG0 to 3	Output	Output port G ₀ to G ₃ (with high-voltage digit driver). Capable of 4-bit output and single-bit set/reset. Capable of 4-bit input of output latch contents and single-bit decision of output latch for branch. Use/nonuse of pull-down resistor bitwise selectable by option.
PH0 to 3	Output	Output port H ₀ to H ₃ (with high-voltage digit driver). Capable of 4-bit output and single-bit set/reset. Capable of 4-bit input of output latch contents and single-bit decision of output latch for branch. Use/nonuse of pull-down resistor bitwise selectable by option.
PI0, 1	Output	Output port I ₀ , I ₁ (with high-voltage digit driver). Capable of 2-bit output and single-bit set/reset. Capable of 2-bit input of output latch contents and single-bit decision of output latch for branch. Use/nonuse of pull-down resistor bitwise selectable by option.
OSC1	Input	Pin for supplying external clock. If the internal clock mode is used, C, R or a ceramic resonator is connected to this pin and pin OSC2.
OSC2	Output	Pin for externally connecting a resonance circuit for the internal clock mode.
VDD	Input	Power supply pin. Normally connected to +5V.
VSS	—	Connected to 0V power supply.
Vp	Input	Power supply for high-voltage port pull-down resistor.
TEST	Input	LSI test pin. Normally connected to VSS (0V).

System Block Diagram



RAM:	Data memory	ROM:	Program memory
F:	Flag	PC:	Program counter
WR:	Working register	INT:	Interrupt control
AC:	Accumulator	IR:	Instruction register
ALU:	Arithmetic and logic unit	I.DEC:	Instruction decoder
DP:	Data pointer	CF, CSF:	Carry flag
E:	E register		Carry save flag
CTL:	Control register	ZF, ZSF:	Zero flag
OSC:	Oscillator		Zero save flag
TM:	Timer	EXTF:	External interrupt request flag
STS:	Status register	TMF:	Internal interrupt request flag

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Absolute Maximum Ratings at Ta=25°C, VSS=0V (VDD=5V±20% unless otherwise specified)

				unit
Maximum Supply Voltage	VDD max		-0.3~+7.0	V
Input Voltage	VIN (1)	Inputs other than Vp	-0.3~VDD+0.3	V (Note 1)
	VIN (2)	Vp	VDD-45~VDD+0.3	V
Output Voltage	VOUT (1)	Outputs other than ports E, F, G, H, I	-0.3~VDD+0.3	V
	VOUT (2)	Ports E, F, G, H, I	VDD-45~VDD+0.3	V
Peak Output Current	IO (1)	Each pin of ports C, D	-2.0~+2.0	mA
	IO (2)	Each pin of ports E, F	-10~0	mA
	IO (3)	Each pin of ports G, H, I	-15~0	mA
	IO (4)	All pins of ports C to I	-90~+16	mA
Allowable Power Dissipation	Pd max (1)	DIP package, Ta=-30 to +70°C	600	mW
	Pd max (2)	Flat package, Ta=-30 to +70°C	400	mW
Operating Temperature	Topr		-30~+70	°C
Storage Temperature	Tstg		-55~+125	°C

Note 1: For pin OSC1, up to oscillation amplitude generated when internally oscillated under the recommended oscillation conditions in Fig. 3 is allowable.

Recommended Operating Conditions at Ta=-30 to +70°C, VSS=0V (VDD=4.0 to 6.0V unless otherwise specified)

			min	typ	max	unit
Operating Supply Voltage	VDD		4.0	5.0	6.0	V
Power-down Supply Voltage	VDD(MR)	HOLD=VIL(4), HOLD mode	1.8		6.0	V
"H"-Level Input Voltage	VIH (1)	Ports A to D, port A: "normal threshold input"	0.7VDD		VDD	V
	VIH (2)	VDD=4.5 to 5.5V, port A: "low threshold input"	1.9		VDD	V
"L"-Level Input Voltage	VIH (3)	INT, RES, HOLD, OSC1 pins	0.8VDD		VDD	V
	VIL (1)	Ports A to D, port A: "normal threshold input"	VSS		0.3VDD	V
	VIL (2)	VDD=4.5 to 5.5V, port A: "low threshold input"	VSS		0.5	V
	VIL (3)	INT, RES, OSC1 pins	VSS		0.2VDD	V
	VIL (4)	VDD=1.8 to 6.0V, HOLD, TEST pins	VSS		0.2VDD	V
Operating Clock Frequency	fextosc	At external clock input, See Fig. 1.	222		1290	kHz
"H"-Level Clock Pulse Width	twpH	∕	0.3			μs
"L"-Level Clock Pulse Width	twpL	∕	0.3			μs
Clock Input Rise Time	toscR	∕			0.2	μs
Clock Input Fall Time	toscF	∕			0.2	μs
External Capacitance for CR OSC	Cext	} See Fig. 8			220±5%	pF
External Resistance for CR OSC	Rext				6.8±1%	kΩ
External Circuit Constants for Ceramic OSC	R1, R2 C1, C2	See Fig. 3				
Standby Timing	tVDDR	See Fig. 6, VDD=1.8 to 6.0V	0			μs
	tVDDF	∕	0			μs
Allowable Delay in Key Scan Circuit	tDL	See Figs. 9, 10.			(N-3) · Tc	μs
	tDH	∕			(N-3) · Tc	μs

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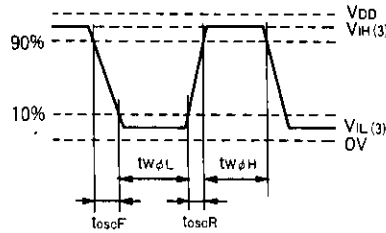


Fig. 1 OSC1 Pin Input Waveform

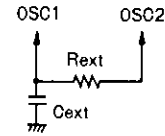


Fig. 2 Recommended Oscillator for CR OSC

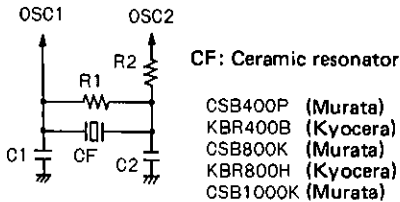


Fig. 3 Recommended Oscillator for Ceramic OSC

Center Frequency	CF	C1(pF)	C2(pF)	R1(kΩ)	R2(kΩ)
400kHz	CSB400P(Murata)	470	470	1000	1.5
	KBR400B(Kyocera)	470	470	1000	1.5
800kHz	CSB800K (Murata)	220	220	1000	1.0
	KBR800H(Kyocera)	220	220	1000	1.0
1000kHz	CSB1000K (Murata)	150	150	1000	1.5
1000kHz	CSB1000K (Murata)	100	100	1000	1.5

C1, C2: Tolerance ±10%

R1, R2: Tolerance ±5%

Electrical Characteristics/Ta=-30 to +70°C, V_{DD}=5V ±20%, V_{SS}=0V

			min	typ	max	unit
"H"-Level Input Current	I _{IH}	All input pins except V _p , V _{IN} =V _{DD}			1	μA
"L"-Level Input Current	I _{IL}	All input pins except V _p , V _{IN} =V _{SS}	-1			μA
"H"-Level Output Voltage	V _{OH} (1)	Ports C, D: I _{OH} =-1mA	V _{DD} -2.0			V
	V _{OH} (2)	Ports C, D: I _{OH} =-100μA	V _{DD} -0.5			V
	V _{OH} (3)	Ports E, F: I _{OH} =-2mA	V _{DD} -1.0			V
	V _{OH} (4)	Ports E, F: I _{OH} =-1mA,	V _{DD} -0.5			V
		all ports I _{OH} =-1mA				
	V _{OH} (5)	Ports G, H, I: I _{OH} =-10mA	V _{DD} -1.8			V
	V _{OH} (6)	Ports G, H, I: I _{OH} =-2mA	V _{DD} -1.0			V
"L"-Level Output Voltage	V _{OL} (1)	Ports C, D: I _{OL} =1mA			0.4	V
	V _{OL} (2)	Ports E, F, G, H, I: V _p =-35V, output Tr OFF, output open, with pull-down resistor			-33	V
"L"-Level Output Current (Output Pull-down resistor)	I _{OL} (R _{PD})	Ports E, F, G, H, I: V _p =-35V, V _{OL} =3V, V _{DD} =5V, with pull-down resistor	0.190	0.362	0.760	mA
			(200)	(105)	(50)	
Output OFF Leak Current	I _{OFF} (1)	Ports C, D: V _{OUT} =V _{DD}			1.0	μA
	I _{OFF} (2)	Ports C, D: V _{OUT} =V _{SS}	-1.0			μA
	I _{OFF} (3)	Port E to I: V _{OUT} =V _{DD} , OD output			30	μA
	I _{OFF} (4)	Port E to I: V _{OUT} =V _{DD} -40V, OD output	-30			μA
Clock OSC Frequency for Ceramic OSC	f _{CFOSC} (1)	Recommended conditions for ceramic OSC, at OSC circuit in Fig. 3 (Note 1)	384	400	416	kHz
	f _{CFOSC} (2)	"	768	800	832	kHz
	f _{CFOSC} (3)	"	960	1000	1040	kHz
Clock OSC Frequency for CR OSC	f _{CROSC}	C _{ext} =220pF, R _{ext} =6.8kΩ, at OSC circuit in Fig. 2	600	800	1220	kHz
Current Dissipation	I _{DD} (1)	At CR OSC, C _{ext} =220pF, R _{ext} =6.8kΩ, output pin open, input pin, V _{IN} =V _{DD}		1.0	2.0	mA
	I _{DD} (2)	At ceramic OSC (800kHz), output pin open, input pin, V _{IN} =V _{DD}		1.0	2.0	mA
	I _{DD} (3)	HALT mode, V _{DD} =4.0 to 6.0V, at test circuit in Fig. 4			10	μA
	I _{DD} (4)	HOLD mode, V _{DD} =1.8 to 6.0V, at test circuit in Fig. 5			10	μA

(Note 1) f_{CFOSC}: Oscillatable frequency

Continued on next page.

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Continued from preceding page.

			min	typ	max	unit
Input Capacitance	C _{IN}	f=1MHz		5		pF
Output Capacitance	C _{OUT}	f=1MHz, output: high impedance		10		pF
Input/Output Capacitance	C _{IO}	"		10		pF

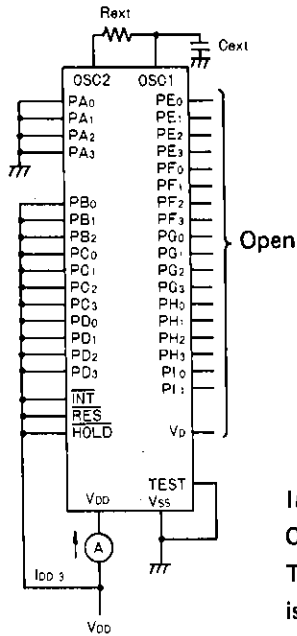


Fig. 4 IDD(3) Test Circuit

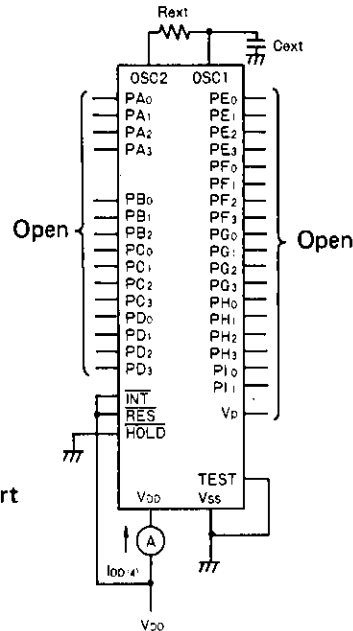


Fig. 5 IDD(4) Test Circuit

Input/output common port
C, D: Output inhibit
The HALT instruction
is executed to cause the
HALT mode to be entered.

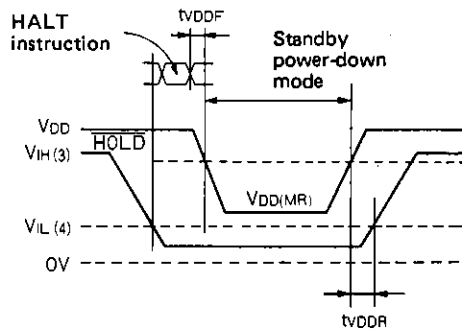


Fig. 6 Standby Mode Timing

(Note)
During the HALT instruction
execution cycle, no chattering
must be applied to the HOLD
pin and PA0 to 3 pins.

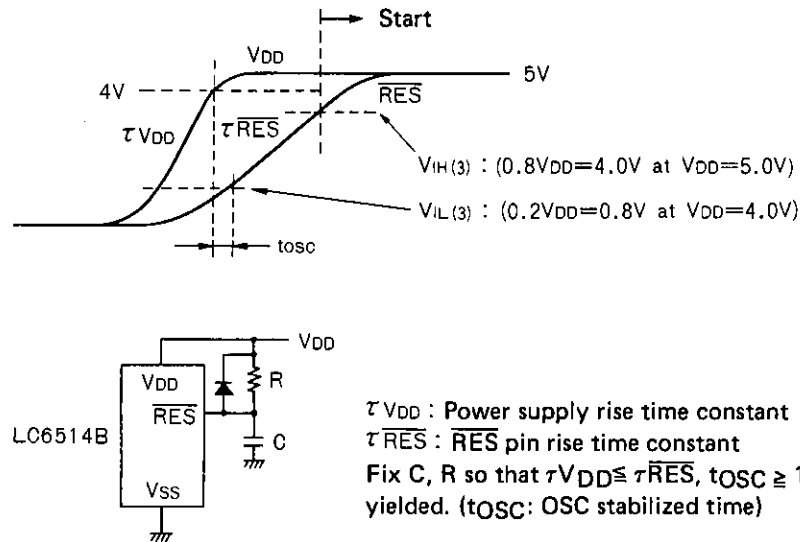


Fig. 7 Initial Reset Timing

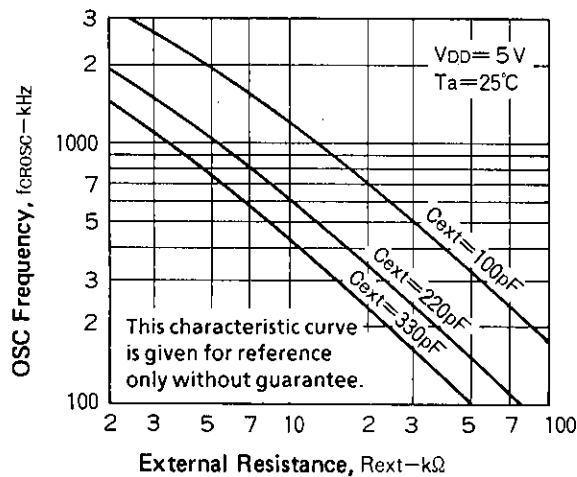
CR OSC characteristic of LC6514B

Fig. 8 shows the CR OSC characteristic of the LC6514B. For the variation range of CR OSC frequency of the LC6514B, the following is guaranteed at external constants of $C_{ext}=220\text{pF}$, $R_{ext}=6.8\text{kohm}$ only. The outgoing inspection is performed under this condition only.

$$600\text{kHz} \leq f_{CROSSC} \leq 1220\text{kHz} \quad \left(\begin{array}{l} T_a = -30^\circ\text{C} \sim +70^\circ\text{C} \\ V_{DD} = 4 \sim 6\text{V} \end{array} \right)$$

If any other constants than specified above are used, the range of $R_{ext}=5\text{k}$ to 50kohm , $C_{ext}=100\text{p}$ to 300pF must be observed. (See Fig. 8.)

Fig. 8 f_{CROSSC} .- R_{ext}



Note 1. The OSC frequency at $V_{DD}=5\text{V}$, $T_a=25^\circ\text{C}$ must be 800kHz or less.

Note 2. The OSC frequency at $V_{DD}=4$ to 6V , $T_a=-30$ to $+70^\circ\text{C}$ must be within the operation clock frequency range (222kHz to 1290kHz).

Proper cares in using the IC

[Digit drive signal-used key scan]

When key-scanning with the FLT digit drive signal in Fig. 9 and inputting the return signal to port A, the following must be observed.

- (a) Estimate voltage drop (V_{ON}) in the output transistor using the current flowing in an FLT used and the V-I characteristic of the output port of the LC6514B.
- (b) Estimate voltage drop (V_{SW}) in the switch circuit.
- (c) Check to see that ($V_{ON} + V_{SW}$) meets the V_{IH}/V_{IL} requirement of the input port.

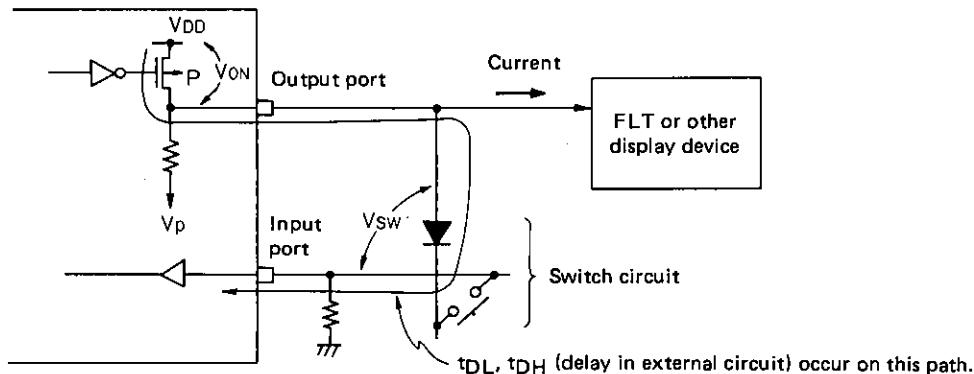
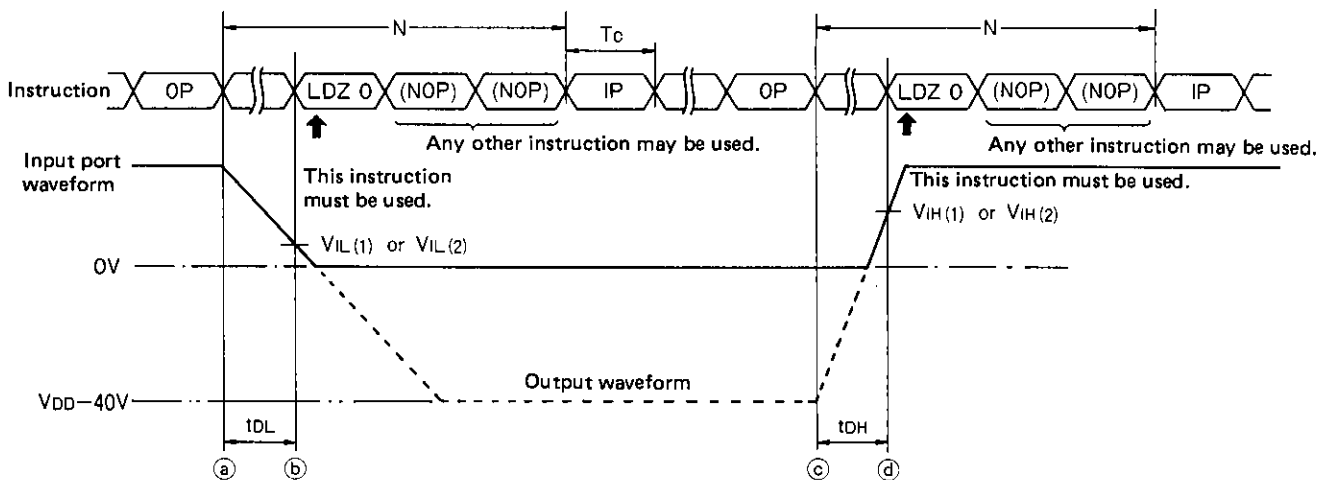


Fig. 9 Sample Key Scan Application

For the key scan application in Fig. 9, make the program considering the delay in the external circuit and the input delay shown below.



N: Number of instruction cycles existing between instruction (OP, SPB, RPB) used to output data to output port and instruction (IP, BP, BNP) used to input data from input port.

(Number of instruction cycles to be programmed according to the length of t_{DL} , t_{DH})

t_{DL} , t_{DH} : Delay in external circuit from output port to input port .

When the IP instruction is used to input the return signal as shown in Fig. 10, the input delay must be considered and three instructions are placed between the IP instruction and the crossing of input port waveform and $V_{IL(1)}$ or $V_{IL(2)}$, $V_{IH(1)}$ or $V_{IH(2)}$ respectively.

Some instructions must be placed additionally according to the length of delay (t_{DL} , t_{DH}) in the external circuit after the digit drive signal is delivered with the execution of the OP instruction (a and c).

<Notes for Standby Function Application>

[Proper cares in using standby function]

The LC6514B provides the standby function called HALT, HOLD mode to minimize the current dissipation when the program is in the wait state. The standby function is controlled by the HALT instruction, the $\overline{\text{HOLD}}$ pin, $\overline{\text{RES}}$ pin. A peripheral circuit and program must be so designed as to provide precise control of the standby function. In most applications where the standby function is performed, voltage regulation, instantaneous break of power, and external noise are not negligible. When designing an application circuit and program, whether or not to take some measures must be considered according to the extent to which these factors are allowed.

This section mainly describes power failure backup for which the standby function is mostly used. A sample application circuit where the standby function is performed precisely is shown below and notes for circuit design and program design are also given below. When using the standby function, the application circuit shown below must be used and the notes must be also fully observed. If any other method than shown in this section is applied, it is necessary to fully check the environmental conditions such as power failure and the actual operation of an application equipment.

[Sample application and notes]

When using the HOLD mode, an application circuit and program must be designed with the following in mind.

- (1) The supply voltage at the standby state must not be less than specified.
- (2) Input timing of each control signal ($\overline{\text{HOLD}}$, $\overline{\text{RES}}$, port A, $\overline{\text{INT}}$, etc.) at the standby initiate/release state.
- (3) Release operation must not be overlapped at the time of execution of the HALT instruction.

A sample application where the standby function is used for power failure backup is shown below as a concrete method to observe these notes. A sample application circuit, its operation, and notes for program design are given below.

1. Sample application where the standby function is used for power failure backup

Power failure backup is an application where power failure of the main power source is detected by the $\overline{\text{HOLD}}$ pin, etc. to cause the HOLD mode to be entered so that the current dissipation is minimized and a backup capacitor is used to retain the contents of the internal registers even during power failure.

1-1. Sample application circuit (CF OSC)

Fig. 11 shows a CF OSC-applied circuit where the standby function is used for power failure backup.

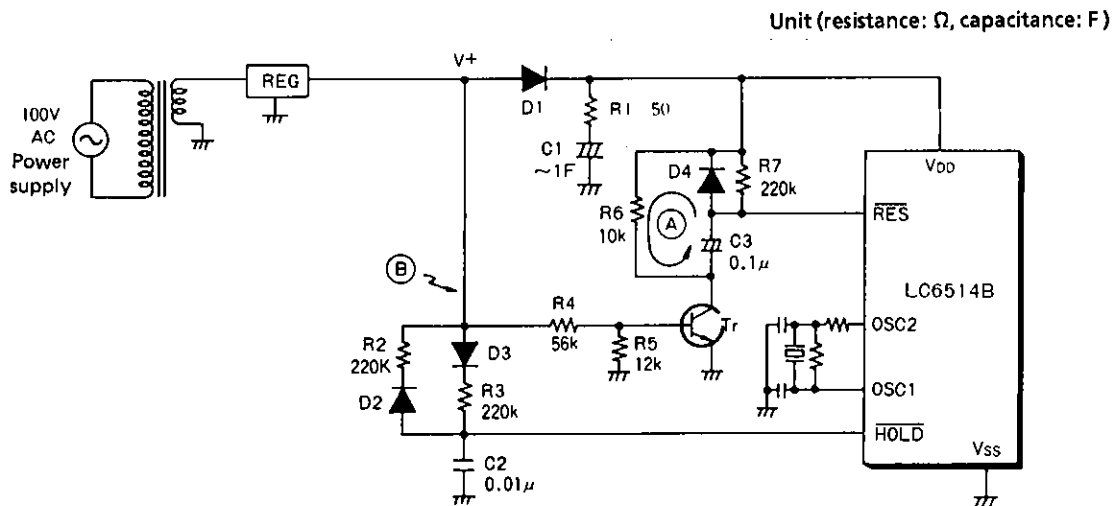
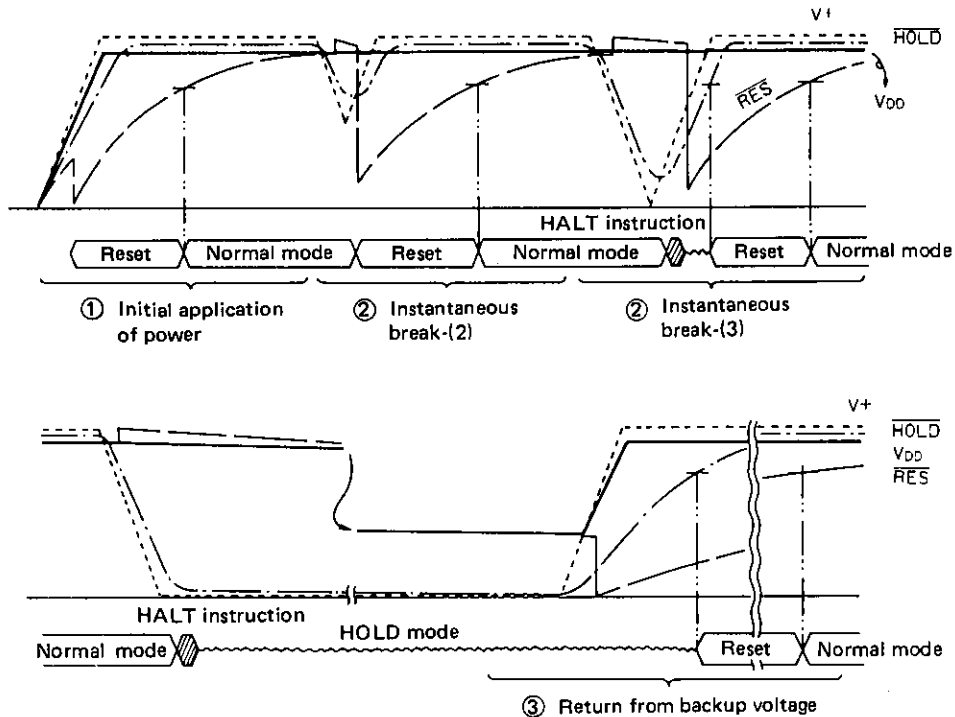


Fig. 11 Sample Application Circuit

1-2. Operating waveform

The operating waveform in the sample application circuit in Fig. 11 is shown below. The mode is roughly divided as follows:

- ① Initial application of power
- ② Instantaneous break
- ③ Return from backup mode



1-3. Operation of sample application circuit

- ① At the time of initial application of power
A reset occurs and the execution of the program starts at address 000H of the program counter (PC).
- ② At the time of instantaneous break
 - (1) At the time of very short instantaneous break
The execution of the program continues.
 - (2) At the time of instantaneous break being a little longer than (1)
(When the \overline{RES} input voltage meets V_{IL} and \overline{HOLD} input voltage does not meet V_{IL})
A reset occurs during the execution of the program and the execution of the program starts at address 000H of the program counter (PC).
Since the \overline{HOLD} request signal is not applied to the \overline{HOLD} pin, the HOLD mode is not entered.
 - (3) At the time of long instantaneous break (When both of the \overline{RES} input voltage and \overline{HOLD} input voltage meet V_{IL})
The \overline{HOLD} request signal is applied to the \overline{HOLD} pin and the HOLD mode is entered.
When V+ rises after instantaneous break, a reset occurs to release the HOLD mode and the execution of the program starts at address 000H of the program counter (PC).
- ③ At the time of return from backup voltage
A reset occurs and the execution of the program starts at address 000H of the program counter (PC).

1-4. Notes for circuit design

- ① How to fix C3, R6, C2, R2
 Fix closed loop (A) discharge time constants C3, R6 and $\overline{\text{HOLD}}$ pin charge time constants C2, R2 so that closed loop (A) fully discharges before the $\overline{\text{HOLD}}$ input voltage gets lower than V_{IL} at the time of instantaneous break and the $\overline{\text{RES}}$ input voltage is sure to get lower than V_{IL} (a reset occurs) when $V+$ rises after instantaneous break where the $\overline{\text{HOLD}}$ input voltage gets lower than V_{IL} .
- ② How to fix C3, R7
 Fix $\overline{\text{RES}}$ pin charge time constants C3, R7 so that when power is applied initially or the HOLD mode is released the CF OSC oscillates normally and the $\overline{\text{RES}}$ input voltage exceeds V_{IH} and the program starts running.
- ③ How to fix R4, R5
 Fix Tr bias constants R4, R5 so that when $V+$ rises after instantaneous break the $\overline{\text{RES}}$ input voltage gets lower than V_{IL} (brought to "L" level) before the $\overline{\text{HOLD}}$ input voltage exceeds V_{IH} (brought to "H" level).
- ④ How to fix C2, R3
 Fix $\overline{\text{HOLD}}$ pin charge time constants C2, R3 so that when the HOLD mode is released from the backup mode the $\overline{\text{HOLD}}$ input voltage does not exceed V_{IH} (not brought to "H" level) until the $\overline{\text{RES}}$ input voltage gets lower than V_{IL} (brought to "L" level).
 Fix C3, R7 and C2, R3 so that the time interval from the moment the $\overline{\text{HOLD}}$ input voltage exceeds V_{IH} until the $\overline{\text{RES}}$ input voltage exceeds V_{IH} is longer than the CF OSC stabilizing time.
- ⑤ When the load is heavy or the polling interval is long
 Since C1 discharges largely, increase the capacity of C1 or separate (B) detection from $V+$ and use a power supply or signal that rises faster than $V+$.

1-5. Notes for software design

When the HOLD request signal is detected, the HALT instruction is executed immediately. A concrete example is shown below.

- ① An interrupt is inhibited before polling the HOLD request pin ($\overline{\text{HOLD}}$ pin).
- ② Polling of the $\overline{\text{HOLD}}$ pin and the HALT instruction are programmed consecutively.

[Concrete example]

```

      RCTL      3      ; EXTEN, TMEN ← 0 (External, timer interrupt inhibit)
      BPO      AAA    ; Polling of the  $\overline{\text{HOLD}}$  pin (If "H" level, a branch occurs to AAA.)
      HALT
AAA:
  
```

Application development tools

Evaluation chip (LC6597), simulation chip (LC65PG97) and the dedicated equipment called "application development tools" are available to facilitate application development of the LC6514B.

- SDS-410 system

This is a combination of floppy disk-provided CPU, CRT, and printer. This system enables application development programs of microcomputers to be prepared (edited, assembled) very speedily and efficiently in assembly language. By connecting the EVA-410 to the CPU, programs can be debugged and assembled data can be written into the EPROM (using EPROM WRITER function contained in the EVA-410).

- EVA-410

This is an evaluation kit having EPROM WRITER function, function of parallel/serial data communication with external equipment (SDS-410, etc.). This kit enables application development programs to be corrected or debugged on the machine language level.

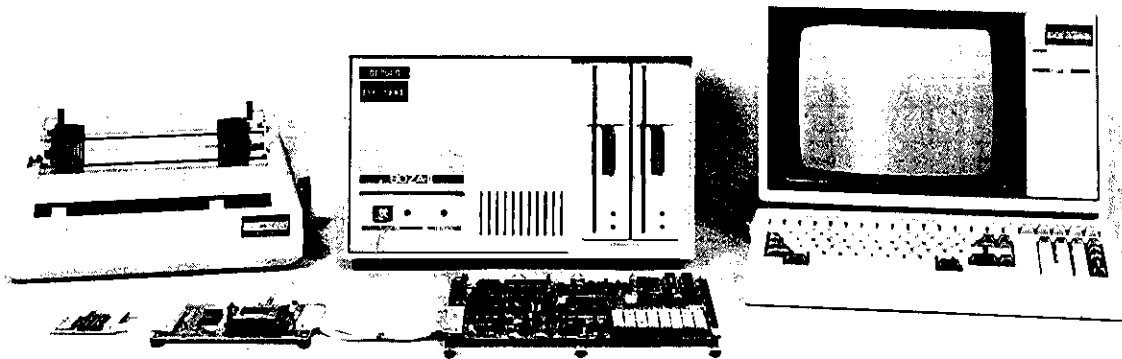
- EVA-TB3B

This is a board which is connected with the EVA-410 to develop programs dedicated to the LC6514B.

- EVA-97-14B

Simulation chip (LC65PG97) is identical with the LC6510C in the I/O port breakdown voltage and pin assignment. Since the LC6514B has high-voltage output ports and differs partially in the pin assignment, conversion board "EVA-97-14B" with high-voltage drivers is used to evaluate the LC6514B.

(Note) The threshold level of input port A of the LC6514B can be selected to be normal/low level by option. However, since port A of the EVA-TB3B, EVA-97-14B is of normal threshold input type, they cannot be used to evaluate the low threshold input version of the LC6514B.



APPENDIX LC6510 Series Instruction Set (by Function)

Symbols	Meaning	M:	Memory	(), { }	: Contents
AC:	Accumulator	M(DP):	Memory addressed by DP	←, →	: Transfer and direction
ACT:	Accumulator bit t	P(DPL):	Input/output port addressed by DPL	+	: Addition
CF:	Carry flag	PC:	Program counter	-	: Subtraction
CTL:	Control register	STACK:	Stack register	∧	: AND
DP:	Data pointer	TM:	Timer	∨	: OR
E:	E register	TMF:	Timer (internal) interrupt request flag	⊕	: Exclusive OR
EXTF:	External interrupt request flag	At, Ha, La:	Working register		
Fn:	Flag bit n	ZF:	Zero flag		

Instruction	Mnemonic	Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks
		D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀						
Accumulator manipulation instructions	CLA	Clear AC	1 1 0 0	0 0 0 0	1	1	AC ← 0	ZF	* 1
	CLC	Clear CF	1 1 1 0	0 0 0 1	1	1	CF ← 0	CF	
	STC	Set CF	1 1 1 1	0 0 0 1	1	1	CF ← 1	CF	
	CMA	Complement AC	1 1 1 0	1 0 1 1	1	1	AC ← \overline{AC}	ZF	
	INC	Increment AC	0 0 0 0	1 1 1 0	1	1	AC ← (AC) + 1	ZF CF	
	DEC	Decrement AC	0 0 0 0	1 1 1 1	1	1	AC ← (AC) - 1	ZF CF	
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC ₀ ← (CF), AC _{n-1} ← AC _n , CF ← AC ₃	ZF CF	
	TAE	Transfer AC to E	0 0 0 0	0 0 1 1	1	1	E ← (AC)		
	XAE	Exchange AC with E	0 0 0 0	1 1 0 1	1	1	(AC) ↔ (E)		
	Memory manipulation instructions	INM	Increment M	0 0 1 0	1 1 1 0	1	1	M(DP) ← (M(DP)) + 1	ZF CF
DEM		Decrement M	0 0 1 0	1 1 1 1	1	1	M(DP) ← (M(DP)) - 1	ZF CF	
SMB bit		Set M data bit	0 0 0 0	1 0 B ₁ B ₀	1	1	M(DP, B ₁ B ₀) ← 1		
RMB bit		Reset M data bit	0 0 1 0	1 0 B ₁ B ₀	1	1	M(DP, B ₁ B ₀) ← 0	ZF	
Operation/comparison instructions	AD	Add M to AC	0 1 1 0	0 0 0 0	1	1	AC ← (AC) + (M(DP))	ZF CF	
	ADC	Add M to AC with CF	0 0 1 0	0 0 0 0	1	1	AC ← (AC) + (M(DP)) + (CF)	ZF CF	
	DAA	Decimal adjust AC in addition	1 1 1 0	0 1 1 0	1	1	AC ← (AC) + 6	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 1 0	1 0 1 0	1	1	AC ← (AC) + 10	ZF	
	EXL	Exclusive or M to AC	1 1 1 1	0 1 0 1	1	1	AC ← (AC) ⊕ (M(DP))	ZF	
	AND	And M to AC	1 1 1 0	0 1 1 1	1	1	AC ← (AC) ∧ (M(DP))	ZF	
	OR	Or M to AC	1 1 1 0	0 1 0 1	1	1	AC ← (AC) ∨ (M(DP))	ZF	
	CM	Compare AC with M	1 1 1 1	1 0 1 1	1	1	(M(DP)) + (AC) + 1	ZF CF	
	CI data	Compare AC with immediate data	0 0 1 0 0 1 0 0	1 1 0 0 1 3 1 2 1 1 0	2	2	$1312110 + (AC) + 1$	ZF CF	
	CLI data	Compare DPL with immediate data	0 0 1 0 0 1 0 1	1 1 0 0 1 3 1 2 1 1 0	2	2	(DPL) ∨ 1312110	ZF	
Load/store instructions	LI data	Load AC with immediate data	1 1 0 0	1 3 1 2 1 1 0	1	1	AC ← 1312110	ZF	* 1
	S	Store AC to M	0 0 0 0	0 0 1 0	1	1	M(DP) ← (AC)		
	L	Load AC from M	0 0 1 0	0 0 0 1	1	1	AC ← (M(DP))	ZF	
	XM data	Exchange AC with M, then modify DPH with immediate data	1 0 1 0	0 M ₂ M ₁ M ₀	2	2	(AC) ↔ (M(DP)) DP _H ← (DP _H) ⊕ 0M ₂ M ₁ M ₀	ZF	The ZF is set/reset according to the result of (DP _H) ⊕ 0M ₂ M ₁ M ₀ .
	X	Exchange AC with M	1 0 1 0	0 0 0 0	1	2	(AC) ↔ (M(DP))	ZF	The ZF is set/reset according to the result of (DP _H) ⊕ 0M ₂ M ₁ M ₀ .
	XI	Exchange AC with M, then increment DPL	1 1 1 1	1 1 1 0	1	2	(AC) ↔ (M(DP)) DPL ← (DPL) + 1	ZF	The ZF is set/reset according to the result of (DPL) + 1.
	XD	Exchange AC with M, then decrement DPL	1 1 1 1	1 1 1 1	1	2	(AC) ↔ (M(DP)) DPL ← (DPL) - 1	ZF	The ZF is set/reset according to the result of (DPL) - 1.
RTBL	Read table data from program ROM	0 1 1 0	0 0 1 1	1	2	AC, E ← ROM (PCh, E, AC)			

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Instruction	Mnemonic	Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks
		D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀						
Data pointer manipulation instructions	LDZ data	Load DPH with Zero and DPL with immediate data respectively	1 0 0 0	13 12 11 10	1	DPH ← 0 DPL ← 13 12 11 10	The DPH and DPL are loaded with 0 and immediate data 13121110 respectively.		
	LHI data	Load DPH with immediate data	0 1 0 0	13 12 11 10	1	DPH ← 13 12 11 10	The DPH is loaded with immediate data 13121110.		
	IND	Increment DPL	1 1 1 0	1 1 1 0	1	DPL ← (DPL) + 1	The DPL contents are incremented +1.	ZF	
	DED	Decrement DPL	1 1 1 0	1 1 1 1	1	DPL ← (DPL) - 1	The DPL contents are decremented -1.	ZF	
	TAL	Transfer AC to DPL	1 1 1 1	0 1 1 1	1	DPL ← (AC)	The AC contents are transferred to the DPL.		
	TLA	Transfer DPL to AC	1 1 1 0	1 0 0 1	1	AC ← (DPL)	The DPL contents are transferred to the AC.	ZF	
Working register manipulation instructions	XAH	Exchange AC with DPH	0 0 1 0	0 0 1 1	1	(AC) ↔ (DPH)	The AC contents and the DPH contents are exchanged.		
	XAt	Exchange AC with working register At	1 1 1 0	11 10	1	(AC) ↔ (A0)	The AC contents and the contents of working register A0, A1, A2, or A3 specified by 1110 are exchanged.		
	XA0		1 1 1 0	0 0 0 0	1	(AC) ↔ (A1)			
	XA1		1 1 1 0	0 1 0 0	1	(AC) ↔ (A2)			
	XA2		1 1 1 0	1 0 0 0	1	(AC) ↔ (A3)			
	XH0	Exchange DPH with working register Ha	1 1 1 1	1 0 0 0	1	(DPH) ↔ (H0)	The DPH contents and the contents of working register H0 or H1 specified by a are exchanged.		
	XH1		1 1 1 1	1 1 0 0	1	(DPH) ↔ (H1)			
	XLa	Exchange DPL with working register La	1 1 1 1	0 0 0 0	1	(DPL) ↔ (L0)	The DPL contents and the contents of working register L0 or L1 specified by a are exchanged.		
	XL1		1 1 1 1	0 1 0 0	1	(DPL) ↔ (L1)			
Flag manipulation instructions	SFB flag	Set flag bit	0 1 0 1	B ₃ B ₂ B ₁ B ₀	1	F _n ← 1	A flag specified by B ₃ B ₂ B ₁ B ₀ is set.		
	RFB flag	Reset flag bit	0 0 0 1	B ₃ B ₂ B ₁ B ₀	1	F _n ← 0	A flag specified by B ₃ B ₂ B ₁ B ₀ is reset.	ZF	The flags are divided into 4 groups of F0 to F3, F4 to F7, F8 to F11, F12 to F15. The ZF is set/reset according to the 4 bits including a single bit specified by immediate data B ₃ B ₂ B ₁ B ₀ .
Jump/subroutine instructions	JMP addr	Jump in the current bank	0 1 1 0	1 P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄	2	PC ← PC ₁₁ (OR PC ₁₁) P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀	A jump to an address specified by the PC ₁₁ (or PC ₁₁) and immediate data P ₁₀ to P ₀ occurs.		If the BANK and JMP instructions are executed consecutively, PC ₁₁ → PC ₁₁ .
	JPEA	Jump in the current page modified by E and AC	1 1 1 1	1 0 1 0	1	PC _{7~0} ← (E, AC)	A jump to an address specified by the contents of the PC whose low-order 8 bits are replaced with the E and AC contents occurs.		
	CZP addr	Call subroutine in the zero page	1 0 1 1	P ₃ P ₂ P ₁ P ₀	1	STACK ← (PC) + 1 PC _{11~6} , PC _{1~0} ← 0 PC _{5~2} ← P ₃ P ₂ P ₁ P ₀	A subroutine in page 0 of bank 0 is called.		
	CAL addr	Call subroutine in the zero bank	1 0 1 0	1 P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄	2	STACK ← (PC) + 2 PC _{11~0} ← 0 P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀	A subroutine in bank 0 is called.		
	RT	Return from subroutine	0 1 1 0	0 0 1 0	1	PC ← (STACK)	A return from a subroutine occurs.		
	RTI	Return from interrupt routine	0 0 1 0	0 0 1 0	1	PC ← (STACK) CF ZF ← CSF, ZSF	A return from an interrupt servicing routine occurs.	ZF CF	
	BANK	Change bank	1 1 1 1	1 1 0 1	1	PC ₁₁ ← (PC ₁₁)	The bank is changed.		Effective only when used immediately before the JMP instruction.
Branch instructions	BAI addr	Branch on AC bit	0 1 1 1	0 0 1 1 1 0 P ₇ P ₆ P ₅ P ₄	2	PC _{7~0} ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if AC ₁ = 1	If a single bit of the AC specified by immediate data 1110 is 1, a branch to an address specified by immediate data P ₇ to P ₀ within the current page occurs.		Mnemonic is BAI0 to BAI3 according to the value of t.
	BNAI addr	Branch on no AC bit	0 0 1 1	0 0 1 1 1 0 P ₇ P ₆ P ₅ P ₄	2	PC _{7~0} ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if AC ₁ = 0	If a single bit of the AC specified by immediate data 1110 is 0, a branch to an address specified by immediate data P ₇ to P ₀ within the current page occurs.		Mnemonic is BNAI0 to BNAI3 according to the value of t.
	BMI addr	Branch on M bit	0 1 1 1	0 1 1 1 1 0 P ₇ P ₆ P ₅ P ₄	2	PC _{7~0} ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (M(DP, t, t, t)) = 1	If a single bit of the MIDP ₁ specified by immediate data 1110 is 1, a branch to an address specified by immediate data P ₇ to P ₀ within the current page occurs.		Mnemonic is BMO0 to BMO3 according to the value of t.
	BNMI addr	Branch on no M bit	0 0 1 1	0 1 1 1 1 0 P ₇ P ₆ P ₅ P ₄	2	PC _{7~0} ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (M(DP, t, t, t)) = 0	If a single bit of the MIDP ₁ specified by immediate data 1110 is 0, a branch to an address specified by immediate data P ₇ to P ₀ within the current page occurs.		Mnemonic is BNMI0 to BNMI3 according to the value of t.
	BPI addr	Branch on Port bit	0 1 1 1	1 0 1 1 1 0 P ₇ P ₆ P ₅ P ₄	2	PC _{7~0} ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (P(DPL, t, t, t)) = 1	If a single bit of port P(DPL) specified by immediate data 1110 is 1, a branch to an address specified by immediate data P ₇ to P ₀ within the current page occurs.		Mnemonic is BPI0 to BPI3 according to the value of t.
	BNPI addr	Branch on no Port bit	0 0 1 1	1 0 1 1 1 0 P ₇ P ₆ P ₅ P ₄	2	PC _{7~0} ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (P(DPL, t, t, t)) = 0	If a single bit of port P(DPL) specified by immediate data 1110 is 0, a branch to an address specified by immediate data P ₇ to P ₀ within the current page occurs.		Mnemonic is BNPI0 to BNPI3 according to the value of t.
	BTM addr	Branch on timer	0 1 1 1	1 1 0 0 P ₇ P ₆ P ₅ P ₄	2	PC _{7~0} ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if TMF = 1 then TMF ← 0	If the TMF is 1, a branch to an address specified by immediate data P ₇ to P ₀ within the current page occurs. The TMF is reset.	TMF	

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Instruction	Mnemonic	Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks	
		D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀							
Branch instructions	BNTM addr	Branch on no timer	0 0 1 1 P ₇ P ₆ P ₅ P ₄	1 1 0 0 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if TMF = 0 then TMF ← 0	If the TMF is 0, a branch to an address specified by immediate data P ₇ to P ₀ within the current page occurs. The TMF is reset.	TMF	
	BI addr	Branch on interrupt	0 1 1 1 P ₇ P ₆ P ₅ P ₄	1 1 0 1 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if EXTF = 1 then EXTF ← 0	If the EXTF is 1, a branch to an address specified by immediate data P ₇ to P ₀ within the current page occurs. The EXTF is reset.	EXTF	
	BNI addr	Branch on no interrupt	0 0 1 1 P ₇ P ₆ P ₅ P ₄	1 1 0 1 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if EXTF = 0 then EXTF ← 0	If the EXTF is 0, a branch to an address specified by immediate data P ₇ to P ₀ within the current page occurs. The EXTF is reset.	EXTF	
	BC addr	Branch on CF	0 1 1 1 P ₇ P ₆ P ₅ P ₄	1 1 1 1 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if CF = 1	If the CF is 1, a branch to an address specified by immediate data P ₇ to P ₀ within the current page occurs.		
	BNC addr	Branch on no CF	0 0 1 1 P ₇ P ₆ P ₅ P ₄	1 1 1 1 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if CF = 0	If the CF is 0, a branch to an address specified by immediate data P ₇ to P ₀ within the current page occurs.		
	BZ addr	Branch on ZF	0 1 1 1 P ₇ P ₆ P ₅ P ₄	1 1 1 0 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if ZF = 1	If the ZF is 1, a branch to an address specified by immediate data P ₇ to P ₀ within the current page occurs.		
	BNZ addr	Branch on no ZF	0 0 1 1 P ₇ P ₆ P ₅ P ₄	1 1 1 0 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if ZF = 0	If the ZF is 0, a branch to an address specified by immediate data P ₇ to P ₀ within the current page occurs.		
	BF _n addr	Branch on flag bit	1 1 0 1 P ₇ P ₆ P ₅ P ₄	n ₃ n ₂ n ₁ n ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if F _n = 1	If a flag bit of the 16 flags specified by immediate data n ₃ n ₂ n ₁ n ₀ is 1, a branch to an address specified by immediate data P ₇ to P ₀ within the current page occurs.		Mnemonic is BF ₀ to BF ₁₅ according to the value of n.
	BNF _n addr	Branch on no flag bit	1 0 0 1 P ₇ P ₆ P ₅ P ₄	n ₃ n ₂ n ₁ n ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if F _n = 0	If a flag bit of the 16 flags specified by immediate data n ₃ n ₂ n ₁ n ₀ is 0, a branch to an address specified by immediate data P ₇ to P ₀ within the current page occurs.		Mnemonic is BNF ₀ to BNF ₁₅ according to the value of n.
Input/output instructions	IP	Input port to AC	0 0 0 0	1 1 0 0	1	1	AC ← (P(DPL))	The contents of port P(DPL) are inputted to the AC.	ZF	
	OP	Output AC to port	0 1 1 0	0 0 0 1	1	1	P(DPL) ← (AC)	The AC contents are outputted to port P(DPL).		
	SPB bit	Set port bit	0 0 0 0	0 1 B ₁ B ₀	1	2	P(DPL, B ₁ B ₀) ← 1	Immediate data B ₁ B ₀ -specified one bit in port P(DPL) is set.		Mnemonic is BF ₀ to BNF ₁₅ according to the value of n.
	RPB bit	Reset port bit	0 0 1 0	0 1 B ₁ B ₀	1	2	P(DPL, B ₁ B ₀) ← 0	Immediate data B ₁ B ₀ -specified one bit in port P(DPL) is reset.	ZF	When this instruction is executed, the E register contents are destroyed.
Other instructions	SCTL bit	Set control register bit(S)	0 0 1 0 1 0 0 0	1 1 0 0 B ₃ B ₂ B ₁ B ₀	2	2	CTL ← (CTL) V B ₃ B ₂ B ₁ B ₀	Immediate data B ₃ B ₂ B ₁ B ₀ -specified bits in the control register are set.		
	RCTL bit	Reset control register bit(S)	0 0 1 0 1 0 0 1	1 1 0 0 B ₃ B ₂ B ₁ B ₀	2	2	CTL ← (CTL) A B ₃ B ₂ B ₁ B ₀	Immediate data B ₃ B ₂ B ₁ B ₀ -specified bits in the control register are reset.	ZF	
	WTTM	Write timer	1 1 1 1	1 0 0 1	1	1	TM ← (E), (AC) TMF ← 0	The E and AC contents are loaded in the timer. The TMF is reset.	TMF	
	HALT	Halt	1 1 1 1	0 1 1 0	1	1	Halt	The standby mode is entered.		
	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	No operation is performed, but 1 machine cycle is consumed.		

*1 If the LI instruction or CLA instruction is used consecutively in such a manner as LI, LI, LI, -----, or CLA, CLA, CLA, -----, the first LI instruction or CLA instruction only is effective and the following LI instructions or CLA instructions are changed to the NOP instructions.

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