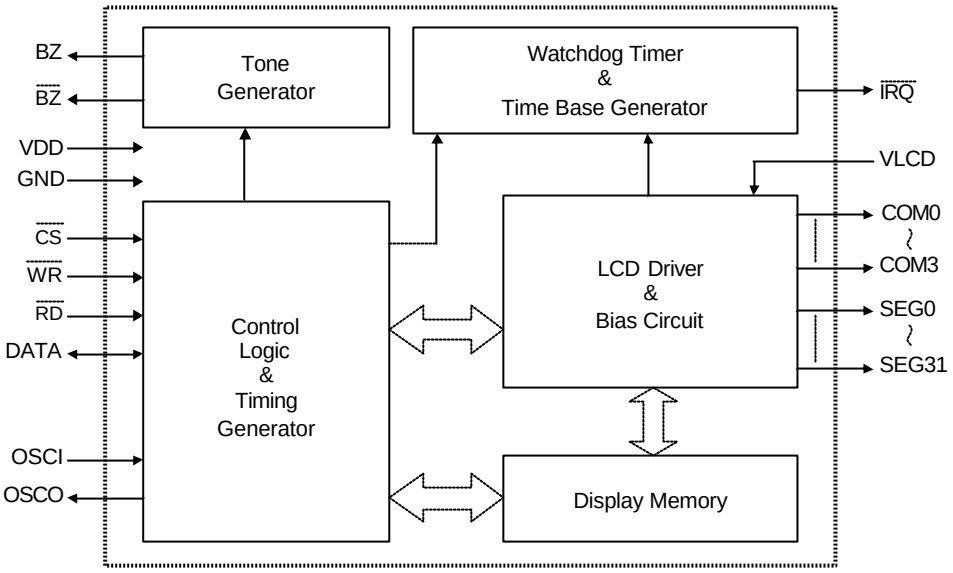
General Descriptions

The ESC1621 is a 128-pattern (32x4), memory mapping, and multi-function LCD driver. The S/W configuration feature of the ESC1621 makes it suitable for multiple LCD applications including LCD modules and display subsystems. Only three or four lines are required for the interface between the host controller and the ESC1621. The ESC1621 contains a power down command to reduce power consumption.

Features

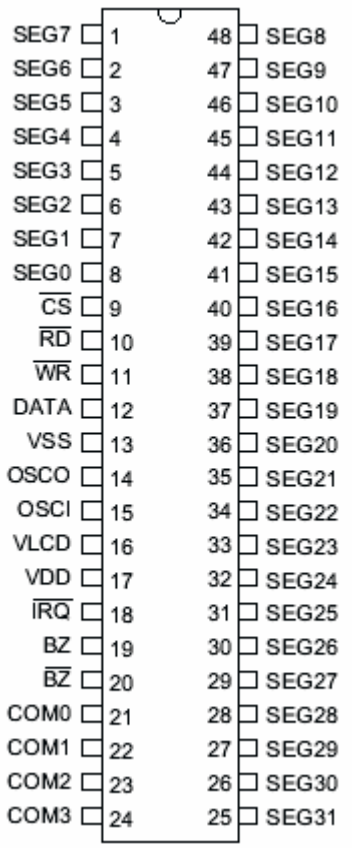
- Operating voltage: 2.4V~5.2V.
- Built-in 256kHz RC oscillator.
- External 32.768kHz crystal or 256kHz frequency source input.
- Selection of 1/2 or 1/3 bias, and selection of 1/2 or 1/3 or 1/4 duty LCD applications.
- Internal time base frequency sources.
- Two selectable buzzer frequencies (2kHz/4kHz).
- Built-in time base generator and WDT.
- Time base or WDT overflow output.
- Power down command reduces power Consumption.
- 8 kinds of time base/WDT clock sources.
- 32x4 LCD driver.
- Built-in 32x4 bit display RAM.
- 3-wire serial interface.
- Internal LCD driving frequency source.
- Software configuration feature.
- Data mode and command mode instructions.
- R/W address auto increment.
- Three data accessing modes.
- VLCD pin for adjusting LCD operating voltage.

Block Diagram

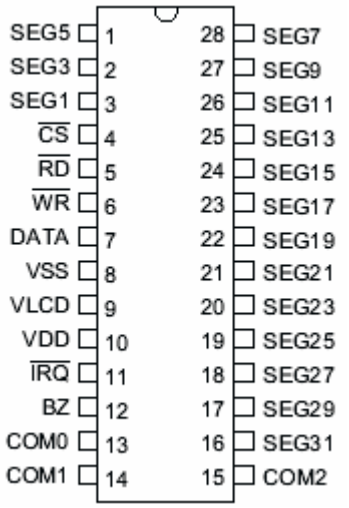


Note: $\overline{CS}$: Chip selection
BZ, $\overline{BZ}$: Tone outputs
$\overline{WR}$, $\overline{RD}$, DATA: Serial interface
$\overline{IRQ}$: Time base or WDT overflow output
COM0~COM3, SEG0~SEG31: LCD outputs

Pin Assignment



ESC1621B-48SSOP



ESC1621D-28SKDIP

Pad Description

Pad No.	Pad Name	I/O	Function
1	$\overline{CS}$	I	Chip selection input with pull-high resistor When the $\overline{CS}$ is logic high, the data and command read from or written to the ESC1621 are disabled. The serial interface circuit is also reset. But if $\overline{CS}$ is at logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the ESC1621 are all enabled.
2	$\overline{RD}$	I	READ clock input with pull-high resistor Data in the RAM of the ESC1621 are clocked out on the falling edge of the $\overline{RD}$ signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data.
3	$\overline{WR}$	I	WRITE clock input with pull-high resistor Data on the DATA line are latched into the ESC1621 on the rising edge of the $\overline{WR}$ signal.
4	DATA	I/O	Serial data input/output with pull-high resistor
5	GND	—	Negative power supply, ground
6	OSCO	O	The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if and on-chip RC oscillator is selected instead, the OSCI and OSCO pads can be left open.
7	OSCI	I	
8	VLCD	I	LCD power input
9	VDD	—	Positive power supply
10	$\overline{IRQ}$	O	Time base or WDT overflow flag, NMOS open drain output
11,12	BZ, $\overline{BZ}$	O	2kHz or 4kHz tone frequency output pair
13~16	COM0~COM3	O	LCD common outputs
48~17	SEG0~SEG31	O	LCD segment outputs

Absolute Maximum Ratings

Supply Voltage……-0.3V ~ 5.5V
Input Voltage…… V_{SS} - 0.3V ~ V_{DD} + 0.3V
Storage Temperature……-50°C ~ 125°C
Operating Temperature……-25°C ~ 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

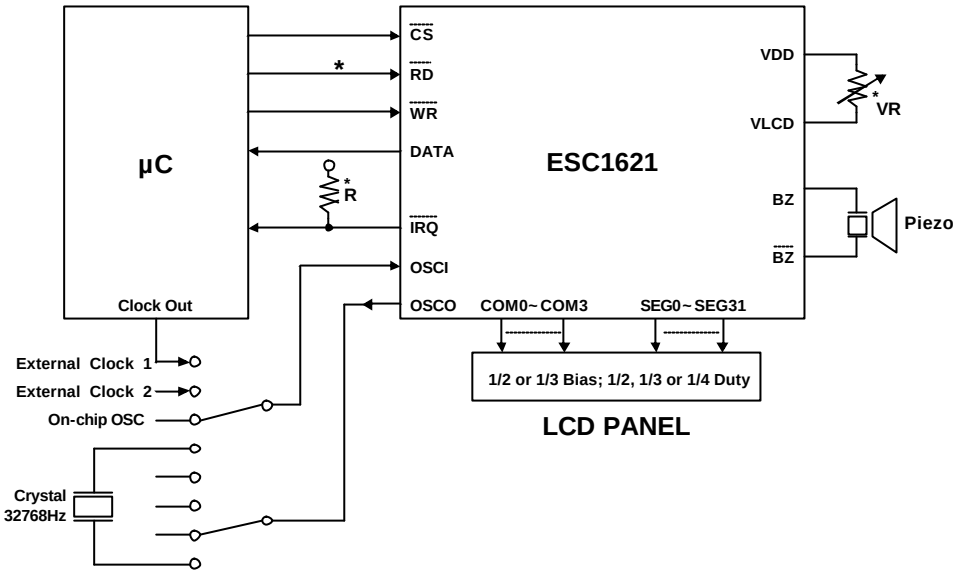
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	—	5.2	V
I_{DD1}	Operating Current	3V	No load/LCD ON On-chip RC oscillator	—	220	300	µA
		5V		—	450	600	µA
I_{DD2}	Operating Current	3V	No load/LCD ON Crystal oscillator	—	90	120	µA
		5V		—	180	240	µA
I_{DD3}	Operating Current	3V	No load/LCD ON External clock source	—	150	200	µA
		5V		—	300	400	µA
I_{STB}	Standby Current	3V	No load Power down mode	—	0.1	5	µA
		5V		—	0.3	10	µA
V_{IL}	Input Low Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	0	—	0.6	V
		5V		0	—	1.0	V
V_{IH}	Input High Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	2.4	—	3.0	V
		5V		4.0	—	5.0	V
I_{OL1}	DATA, BZ, $\overline{BZ}$, $\overline{IRQ}$	3V	V_{OL}=0.3V	0.5	1.2	—	mA
		5V	V_{OL}=0.5V	1.3	2.6	—	mA
I_{OH1}	DATA, BZ, $\overline{BZ}$	3V	V_{OH}=2.7V	-0.4	-0.8	—	mA
		5V	V_{OH}=4.5 V	-0.9	-1.8	—	mA
I_{OL2}	LCD Common Sink Current	3V	V_{OL}=0.3V	80	150	—	µA
		5V	V_{OL}=0.5V	150	250	—	µA
I_{OH2}	LCD Common Source Current	3V	V_{OH}=2.7V	-80	-120	—	µA
		5V	V_{OH}=4.5 V	-120	-200	—	µA
I_{OL3}	LCD Segment Sink Current	3V	V_{OL}=0.3V	60	120	—	µA
		5V	V_{OL}=0.5V	120	200	—	µA
I_{OH3}	LCD Segment Source Current	3V	V_{OH}=2.7V	-40	-70	—	µA
		5V	V_{OH}=4.5 V	-70	-100	—	µA
R_{PH}	Pull-high Resistor	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	40	80	150	kO
		5V		30	60	100	kO

A.C. Characteristics

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS1}	System Clock	3V	On-chip RC oscillator	—	256	—	kHz
		5V		—	256	—	kHz
f_{SYS2}	System Clock	3V	Crystal oscillator	—	32.768	—	kHz
		5V		—	32.768	—	kHz
f_{SYS3}	System Clock	3V	External clock source	—	256	—	kHz
		5V		—	256	—	kHz
f_{LCD}	LCD Clock	—	On-chip RC oscillator	—	F_{SYS1}/1024	—	Hz
			Crystal oscillator	—	F_{SYS2}/128	—	Hz
			External clock source	—	F_{SYS3}/1024	—	Hz
t_{COM}	LCD Common Period		n: Number of COM	—	n/f_{LCD}	—	s
f_{CLK1}	Serial Data Clock ($\overline{WR}$ Pin)	3V	Duty cycle 50%	—		150	kHz
		5V		—		300	kHz
f_{CLK2}	Serial Data Clock ($\overline{RD}$ Pin)	3V	Duty cycle 50%	—		75	kHz
		5V		—		150	kHz
f_{TONE}	Tone Frequency		On-chip RC oscillator	—	2.0 or 4.0	—	kHz
t_{CS}	Serial Interface Reset Pulse Width (Figure 3)	3V	$\overline{CS}$	—	250	—	ns
		5V					
t_{CLK}	$\overline{WR}$, $\overline{RD}$ Input Pulse Width (Figure 1)	3V	Write mode	3.34	—	—	µs
			Read mode	6.67	—	—	
		5V	Write mode	1.67	—	—	µs
			Read mode	3.34	—	—	
t_r, t_f	Rise/Fall Time Serial Data Clock Width (Figure 1)	3V	—	—	120	—	ns
		5V					
t_{su}	Setup Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	3V	—	—	120	—	ns
		5V					
t_h	Hold Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	3V	—	—	120	—	ns
		5V					
t_{su1}	Setup Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	3V	—	—	100	—	ns
		5V					
t_{h1}	Hold Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	3V	—	—	100	—	ns
		5V					

Application Circuits

Host controller with a ESC1621 display system



Note: The connection of $\overline{IRQ}$ and $\overline{RD}$ pin can be selected depending on the requirement of the µC.

The voltage applied to V_{LCD} pin must be lower than V_{DD}.

Adjust VR to fit LCD display, at V_{DD}=5V, V_{LCD}=4V, VR=15kΩ±20%

Adjust R (external pull-high resistance) to fit user's time base clock.