IDT79RV4640/IDT79RC64V474 PCI MEZZANINE CARD

PRELIMINARY
IDT7M9510
IDT7M9514

FEATURES:

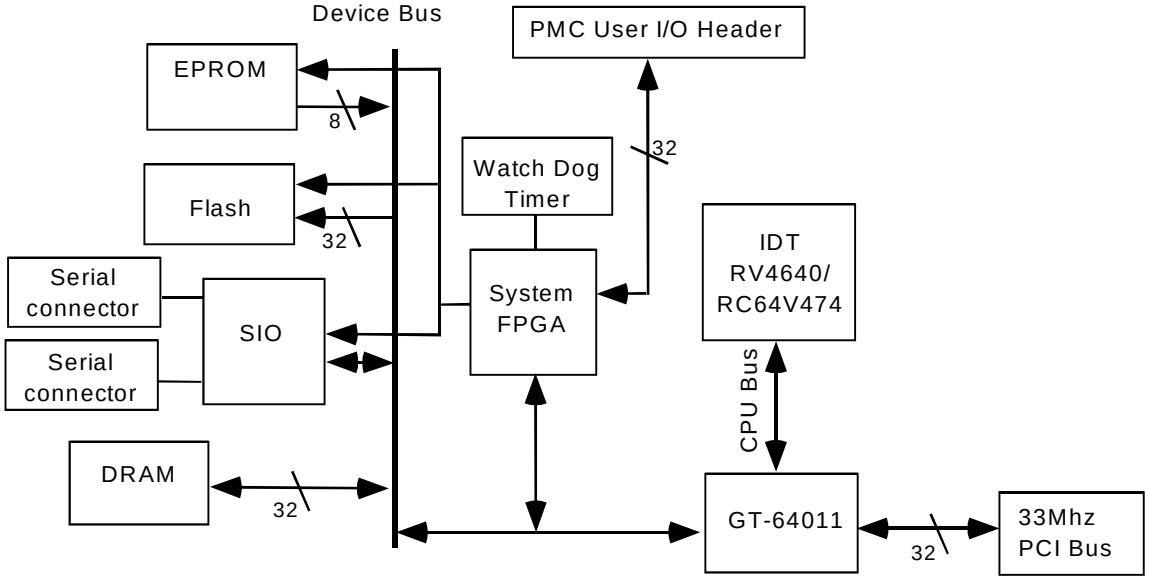
- **PCI Mezzanine Card (PMC) (IEEE 1386) form factor**
- **7M9510 High performance IDT79RV4640 MIPS Processor**
  - *100Mhz, 150Mhz, 180Mhz, 200MHz CPU speeds supported*
  - *50MHz maximum CPU bus frequency*
  - *33MHz maximum PCI bus frequency*
- **7M9514 High performance IDT79RC64V474 MIPS Processor**
  - *180Mhz, 200Mhz, 250Mhz CPU speeds supported*
  - *50MHz maximum CPU bus frequency*
  - *33MHz maximum PCI bus frequency*
- **DRAM**
  - *72-position SIMM slot*
  - *4MB to 128MB of DRAM supported*
  - *32-bit width*
- **Flash**
  - *2MB of on board Flash memory*
  - *32-bit width*
- **EPROM**
  - *up to 512KB*
  - *8-bit width*
  - *32 Pin PLCC socket*
- **Two serial interface ports (16550A compatible)**
- **Uses Galileo GT-64011 PCI System controller**
  - *DMA*
    - *four independent channels*
    - *chaining via linked lists of records*
    - *byte alignment on source and destination*
    - *transfers through a 32 byte internal FIFO which moves data between PCI, memory and devices*
  - *PCI*
    - *host to PCI bridge*
    - *PCI to main memory bridge*
    - *fully compatible to PCI rev 2.1*
    - *high performance PCI interfaces via 96 bytes of posted write and read prefetch buffers*
- **Other Features**
  - *Manual Cold Reset (Pushbutton and two pin header)*
  - *hardware based masking of interrupts*
  - *Configurable Timer Interrupt Generator*
  - *32 Bits of user defined I/O mapped through system FPGA*
  - *VxWorks Board Support Package available from IDT*

DESCRIPTION:

The IDT7M9510/7M9514 is a Single Board Computer utilizing IDT's 79RV4640/79RC64V474 MIPS processor. This CPU Mezzanine Card is designed for use in applications where low profile, parallel board to board mounting is required. The 7M9510/7M9514 consists of an IDT79RV4640 / IDT79RC64V474 processor based subsystem that can either form the core CPU function for an embedded application, or can be an optional add-in accelerator to a PCI based system through a PCI v2.1 compatible, PMC Standard (IEEE P1386.1) connector.

The card conforms, in length and width to the standard single size PMC form factor as specified in IEEE P1386.1, and it contains all the features required of a typical CPU subsystem for embedded processor applications. Some of these features include: DRAM, Flash, serial ports and full PCI interrupt support.

FUNCTIONAL BLOCK DIAGRAM



4095 drw 01

March 1999

BOARD OVERVIEW

The IDT7M9510/9514 consists of the following functional blocks: IDT79RV4640/IDT79RC64V474 MIPS processor, Galileo GT-64011 PCI System Controller, DRAM memory, system Glue Logic (FPGA based), Flash/EPROM and dual serial channels. The IDT7M9510/9514 CPU subsystem is designed to interface with its targeted system through a standard PCI Mezzanine Card form factor.

IDT79RV4640 PROCESSOR

The IDT79RV4640 is a high performance cost-effective MIPS processor targeted at embedded applications which runs at internal frequencies from 100MHz to 200MHz. Further information can be found in the 79RV4640 Data Sheet, available from IDT.

IDT79RC64V474 PROCESSOR

The IDT79RC64V474 is a high performance cost-effective MIPS processor targeted at embedded applications which runs at internal frequencies from 180MHz to 250MHz. Further information can be found in the 79RC64V474 Data Sheet, available from IDT.

GT-64011 PCI SYSTEM CONTROLLER

The GT-64011 is a system support device from Galileo Technology, Inc. This chip provides the bulk of the system control and support functions required for a MIPS RV4640/RC64V474 CPU based system. The GT-64011 has a three bus architecture. These three busses are: a CPU bus interface, a PCI bus interface and a memory/device bus interface. In addition the GT-64011 contains a DRAM controller and a DMA controller. Further information can be found in the GT-64011 Data Sheet, available from Galileo Technology.

DRAM

The main memory is implemented using one standard 72-position DRAM SIMM providing a 32-bit path to memory.

The main memory is designed to support one or two banks of DRAM which is dependent on the type of SIMM being used. One bank is supported when a single bank DRAM SIMM is used (e.g., 1M x 32), and two banks are supported when a double bank DRAM SIMM is used (e.g., 2M x 32). The design can use any standard DRAM SIMM containing 4MB (1M x 32), 8MB (2M x 32), 16 MB (4M x 32), or 32MB (8M x 32), 64MB (16M x 32), or 128MB (32M x 32) allowing the 7M9510/7M9514 to have up to a maximum of 128MB of memory. 60ns memory is recommended. The memory configuration is flexible and is field upgradeable.

BOOT EPROM

The Boot EPROM is a standard 512K x 8 EPROM which holds the boot code, the debug monitor and power-on diagnostics. (Socket supports Flash chip for development)

FLASH MEMORY

The 7M9510 / 7M9514 has 2MB of Flash on board, configured as 512K x 32.

SYSTEM FPGA

The system FPGA is responsible for the following functions: Processor initialization, Reset Control, Device Decoding, Interrupt Masking / Mapping.

PROCESSOR INITIALIZATION

The 79RV4640 / 79RC64V474 requires a serial data stream for initialization. The initialization process is handled by the system FPGA.

RESET CONTROL

Once the FPGA is loaded, the CPU is booted by sequencing the VCCOK, WARMRESET, COLDRESET lines. At boot-up, the CPU applies MODECLOCK to the FPGA to read out several bytes of configuration information using the MODEIN line.

There is a push button for resetting the 7M9510 / 7M9514. This is connected to the FPGA through the SYSRESET signal. Additionally, a 2-pin header is provided for connection to an external reset switch.

INTERRUPT STRUCTURE

The system FPGA implements a basic interrupt controller that maps the various interrupt sources to the CPU interrupts. It also gives the CPU the ability to mask interrupts and generate PCI interrupts.

PCI INTERFACE

The GT-64011 includes a full featured host to PCI bridge which can operate as either a target or initiator. For improved performance the bridge contains 96 bytes of posted write and read prefetch buffers.

The GT-64011 initiates PCI cycles when either the CPU or the DMA engine generates a bus cycle to PCI address space. These cycles can be either Memory, Interrupt Acknowledge, Special, I/O, or Configuration cycles. Configuration registers can be accessed from either the host bus or the PCI bus.

The GT-64011 includes a full featured DRAM controller and generates all control signals for the DRAM SIMM.

Further information can be found in the GT-64011 Data Sheet, available from Galileo Technology.

PC16552 DUAL SERIAL PORT CONTROLLER

The PC16552D is a Dual Universal Asynchronous Receiver/Transmitter. Each independent channel is software compatible with the PC16550D. Further information can be found in the PC16552D Data Sheet, available from National Semiconductor.

WATCHDOG TIMER

The WatchDog Timer generates a non-maskable interrupt from a MAX706TCSA. It is used to control the system reset logic and to provide a watchdog reset. Further information can be found in the MAX706 Data Sheet, available from Maxim.

SERIAL PORTS

There are two RS232-C serial port connectors on the 7M9510 / 7M9514 which are labeled on the board as "COM1" and "COM2". The Pin #1 reference marking on the PCB should be utilized to ensure proper orientation when connecting adapter cables to the header.

SERIAL HEADER PINOUT (COM1, COM2)

(Top View)

DCD	1	2	DSR
RD	3	4	RTS
TD	5	6	CTS
DTR	7	8	RI
GND	9	10	NC

SOFTWARE MEMORY MAP

The following is the default memory map of the IDT7M9510 / 7M9514. These values can be changed by writing to the appropriate address decode registers in the GT-64011. For further information on reconfiguring the Memory Map refer to the GT-64011 Data Sheet, available from Galileo Technology.

GT-64011 Physical Address	Size	Description	Device Select
0x0000 0000	8MB	DRAM Bank 0	-----
0x0080 0000	8MB	DRAM Bank 1	-----
0x1000 0000	-----	PCI I/O	-----
0x1200 0000	-----	PCI Memory 0	-----
0x1400 0000	-----	GT64011 Internal Registers	-----
0x1FC0 0000	4MB	Boot EPROM	BootCS
0x1C80 0000	2MB	Flash Memory	CS1
0x1C20 0BE0	-----	Serial Port - COM1	CS0
0x1C20 0FE0	-----	Serial Port - COM2	CS0
0xF200 0000	-----	PC1 Memory 1	-----

4095 tbl 01

POWER REQUIREMENTS

	7M9510S180M		7M9510S150M		7M9510S100M	
	Min	Max	Min	Max	Min	Max
V_{CC5}	4.75V	5.25V	4.75V	5.25V	4.75V	5.25V
V_{CC3}	3.15V	3.45V	3.15V	3.45V	3.15V	3.45V
I_{CC5}	-----	TBD	-----	TBD	-----	TBD
I_{CC3}	-----	TBD	-----	TBD	-----	TBD

4095 tbl 02

ENVIRONMENTAL

	Temp. (C)		Humidity (1)		Altitude	
Condition	Min	Max	Min	Max	Min	Max
Operating	0	50	20%	80%	0	10,000
Under Bias	-10	50	10%	90%	0	10,000
Storage	-25	60	10%	90%	0	

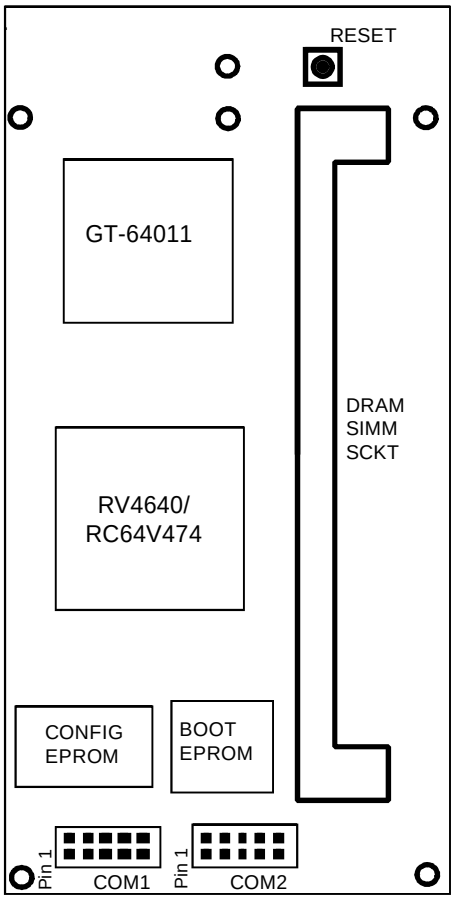
4095 tbl 03

Notes:

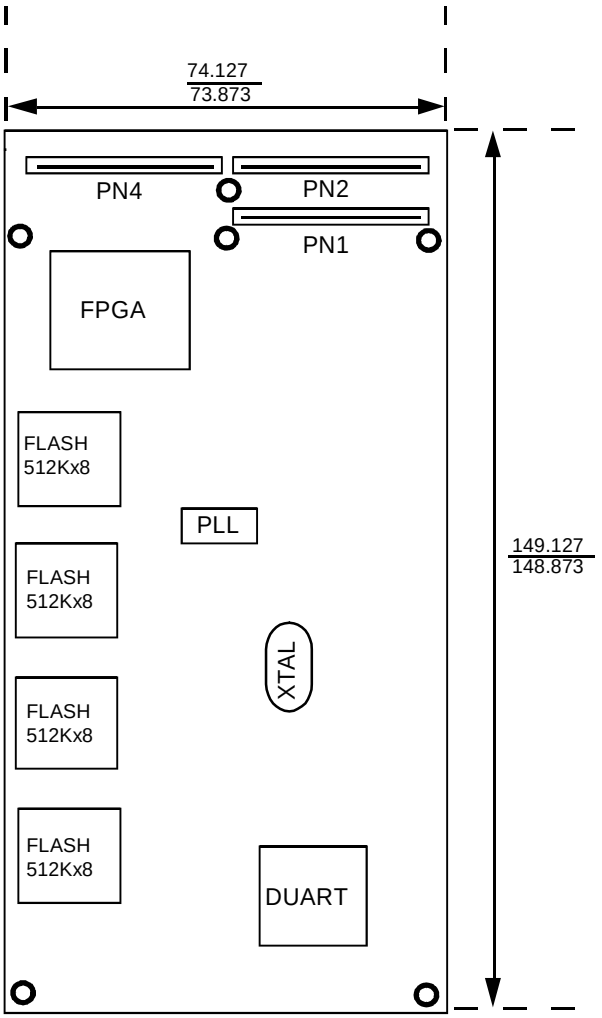
1. Non-Condensing

BOARD DIMENSIONS

TOP VIEW



BOTTOM VIEW

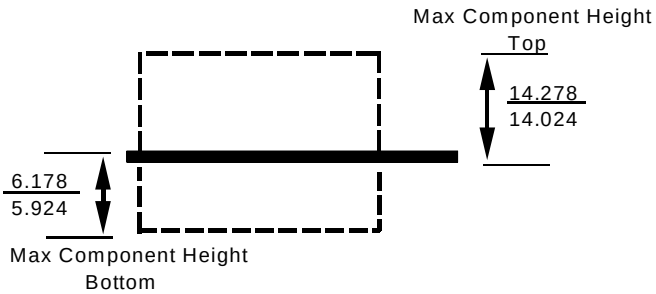


4095 drw 02

NOTES:

1. All dimensions in millimeters (mm).

SIDE VIEW



4095 drw 03

PMC CONNECTORS

The 7M9510 / 7M9514 utilizes three 64 position connectors that are compliant with the PMC standard. The placement of these connectors is in compliance with the Common Mezzanine Card (CMC) Specification (IEEE 1386) and the PCI Mezzanine Card (PMC) Specification (IEEE 1386.1). Headers correspond as follows:

-J1 on the 7M9510 / 7M9514 corresponds to PN11 (PN1) and P12 (PN2) in the PMC and CMC Specifications.

-J2 on the 7M9510 / 7M9514 corresponds to P14 (PN4) in the PMC and CMC Specifications.

For further information on the mechanical placement of the PMC headers, refer to the Common Mezzanine Card (CMC) Specification (IEEE 1386).

PIN ASSIGNMENTS

The 32-bit bus is implemented in J1 (PN1 and PN2), in compliance with the PMC Specifications and is provided below. The User-Defined I/O is implemented in J2 (PN4) and is provided below.

PN1

Pin #	Signal Name	Signal Name	Pin #
1	TCK	-12V (1)	2
3	GND	INTA#	4
5	INTB#	INTC#	6
7	BUSMODEE1#	+5v	8
9	INTD#	PCI-RSVD (1)	10
11	GND	PCI-RSVD (1)	12
13	CLK	GND	14
15	GND	GNT#	16
17	REQ#	+5V	18
19	V(I/O) (1)	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	GND	24
25	GND	C/BE[3]#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	V(I/O) (1)	AD[17]	32
33	FRAME#	GND	34
35	GND	IRDY#	36
37	DEVSEL#	+5V	38
39	GND	LOCK#	40
41	SDONE#((1)	SBO# (1)	42
43	PAR	GND	44
45	V(I/O) (1)	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	GND	C/BE[0]#	52
53	AD[06]	AD[05]	54
55	AD[04]	GND	56
57	V(I/O)	AD[13]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	GND	REQ64#	64

4095 tbl 04

PN2

Pin #	Signal Name	Signal Name	Pin #
1	+12V (1)	TRST#	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	PCI-RSVD (1)	8
9	PCI-RSVD (1)	PCI-RSVD (1)	10
11	BUSMODE2# (1)	+3.3V	12
13	RST#	BUSMODE3#	14
15	+3.3V	BUSMODE4#	16
17	PCI-RSVD (1)	GND	18
19	AD[30]	AD[29]	20
21	GND	AD[26]	22
23	AD[24]	+3.3V	24
25	IDSEL	AD[23]	26
27	+3.3V	AD[20]	28
29	AD]18]	GND	30
31	AD[16]	C/BE[2]#	32
33	GND	PMC-RSVD (1)	34
35	TRDY#	+3.3V	36
37	GND	STOP#	38
39	PERR#	GND	40
41	+3.3V	SERR#	42
43	C/BE[1]#	GND	44
45	AD[14]	AD[13]	46
47	GND	AD[10]	48
49	AD[08]	+3.3V	50
51	AD[07]	PMC-RSVD (1)	52
53	+3.3V	PMC-RSVD (1)	54
55	PMC-RSVD (1)	GND	56
57	PMC-RSVD (1)	PMC-RSVD (1)	58
59	GND	PMC-RSVD (1)	60
61	ACK64# (1)	+3.3V	62
63	GND	PMC-RSVD (1)	64

4095 tbl 05

NOTES:

1. Not connected on 7M9510 / 7M9514

PN4 (1)

Pin #	Signal Name	Signal Name	Pin #
1	USER I/O #1	NC	2
3	USER I/O #3	NC	4
5	USER I/O #5	USER I/O #6	6
7	USER I/O #7	USER I/O #8	8
9	USER I/O #9	USER I/O #10	10
11	USER I/O #11	USER I/O #12	12
13	USER I/O #13	USER I/O #14	14
15	NC	USER I/O #16	16
17	NC	NC	18
18	NC	NC	20
21	USER I/O #21	USER I/O #22	22
23	USER I/O #23	USER I/O #24	24
25	NC	USER I/O #26	26
27	USER I/O #27	USER I/O #28	28
29	USER I/O #29	USER I/O #30	30
31	NC	NC	32
33	USER I/O #33	USER I/O #34	34
35	NC	NC	36
37	NC	NC	38
39	NC	NC	40
41	NC	NC	42
43	NC	NC	44
45	NC	NC	46
47	NC	NC	48
49	NC	NC	50
51	NC	NC	52
53	NC	NC	54
55	NC	NC	56
57	USER I/O #57	USER I/O #58	58
59	USER I/O #59	USER I/O #60	60
61	USER I/O #61	USER I/O #62	62
63	USER I/O #63	USER I/O #64	64

4095 tbl 06

NOTES:

1. All of the User I/O pins are mapped through the on board FPGA.

7M9510SR Version

The "SR" version of the 7M9510 is intended for customers using the I-Cube Raptor™ Fast Ethernet Switch Design. In this configuration, the Boot ROM shipped with the 7M9510 contains the most recent version of the I-Cube "Mini-Boot Monitor" (MBM). For applications other than the I-Cube Raptor™ Reference Design and the I-Cube FPGA configuration PROM, the recommended board configuration is the 7M9510SE which ships with IDT/Sim and IDT FPGA configuration PROM.

7M9510SE Version (EVALUATION)

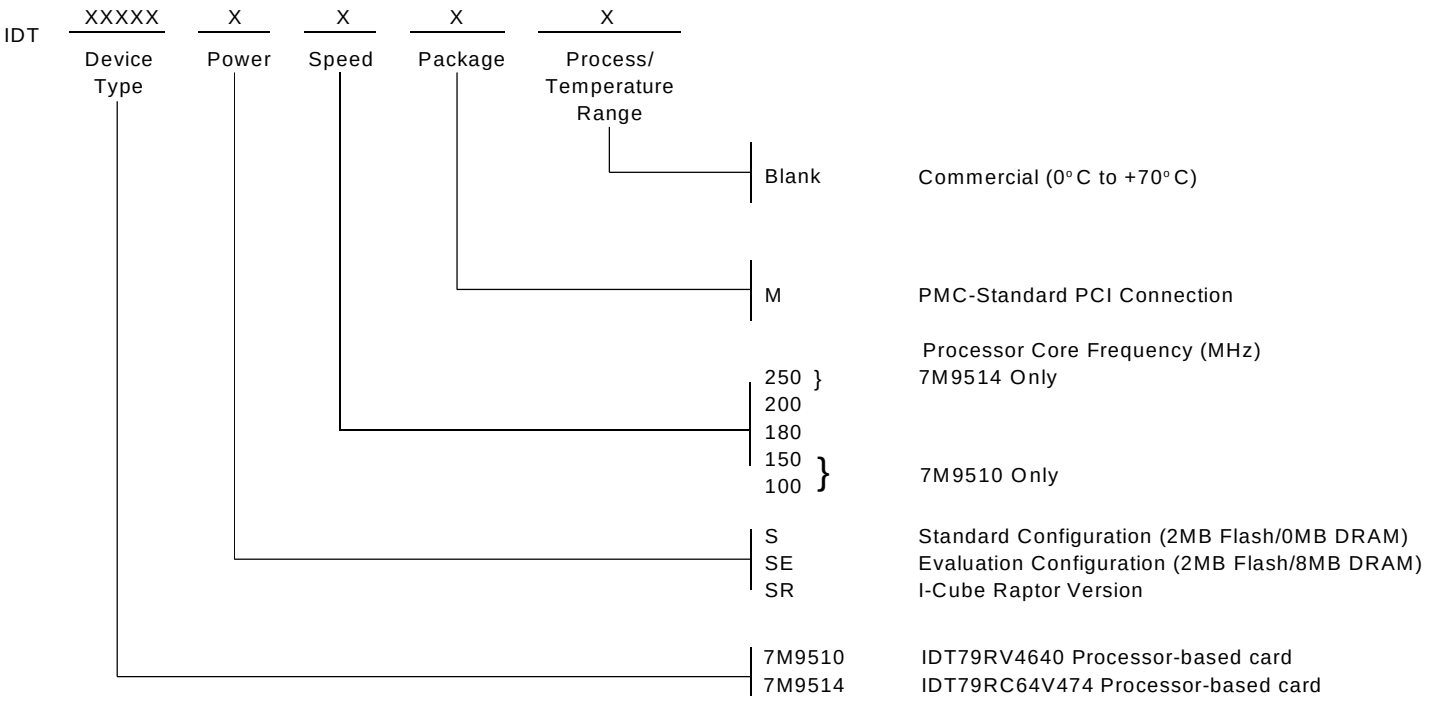
The "SE" version of the 7M9510 is packaged to support software development and prototyping. Currently the Evaluation package contains the following material:

- 1 7M9510S
- 1 8MB (2M x 32) EDO DRAM SIMM
- 1 512KB (512K x 8) IDT/Sim Boot ROM

Alternately, the 7M9710 Development Kit may be ordered. This kit includes all of the 7M9510SE components listed above. In addition the 7M9710 includes the following items:

- 1 set of 7M9510 board schematics
- 1 copy of 7M9510 Datasheet
- 2 10 pin Serial Port to DB9 Adapter Cables
- 2 6 foot DB9 to DB9 null modem serial cables
- 1 7M9502 PCI Backplane
- 1 7M9710 Quickstart Guide

ORDERING INFORMATION



4095 drw 04

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015
fax: 408-492-8674
www.idt.com

for Tech Support:
408-988-5647
ssdhelp@idt.com