LR38603

Digital Signal Processor for Color CCD Cameras

DESCRIPTION

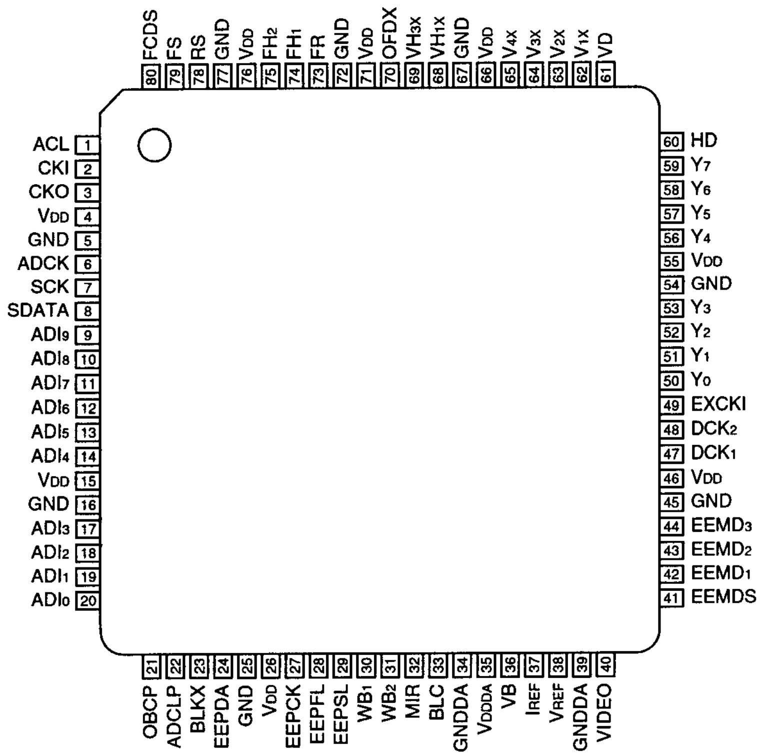
The LR38603 is a CMOS digital signal processor for color CCD video camera systems of 270 k/320 k/410 k/470 k-pixel CCDs with complementary color filters. The video camera system consists of CDS/PGA/ADC IC (IR3Y48A1), DSP IC (LR38603) and V driver IC (LR36685) with CCD.

FEATURES

- Designed for 1/4-type 270 k/320 k/410 k/470 k-pixel color CCDs with Mg, G, CY, and Ye complementary color filters
- Switchable between NTSC and PAL modes
- Built-in signal generation circuit for driving CCD and various pulses for TV signals
- Parameters for camera signal processing can be set
- Built-in auto exposure control
- Built-in auto white balance control
- Built-in auto carrier balance control
- Built-in drive circuit for 2 K-bit EEPROM
- Built-in 9-bit D/A converter
- Built-in mirror image output
- Built-in circuit to reduce line crawl noise
- Built-in auto white detect correction
- YUV digital output (8 bits x 2)
- UYVY digital output (8 bits x 1)
- Analog video output
- External clock input (8 fsc)
- Built-in vertical reset
- Built-in horizontal reset
- Single +3.3 V power supply
- Package :
  80-pin LQFP (P-LQFP080-1212) 0.5 mm pin-pitch

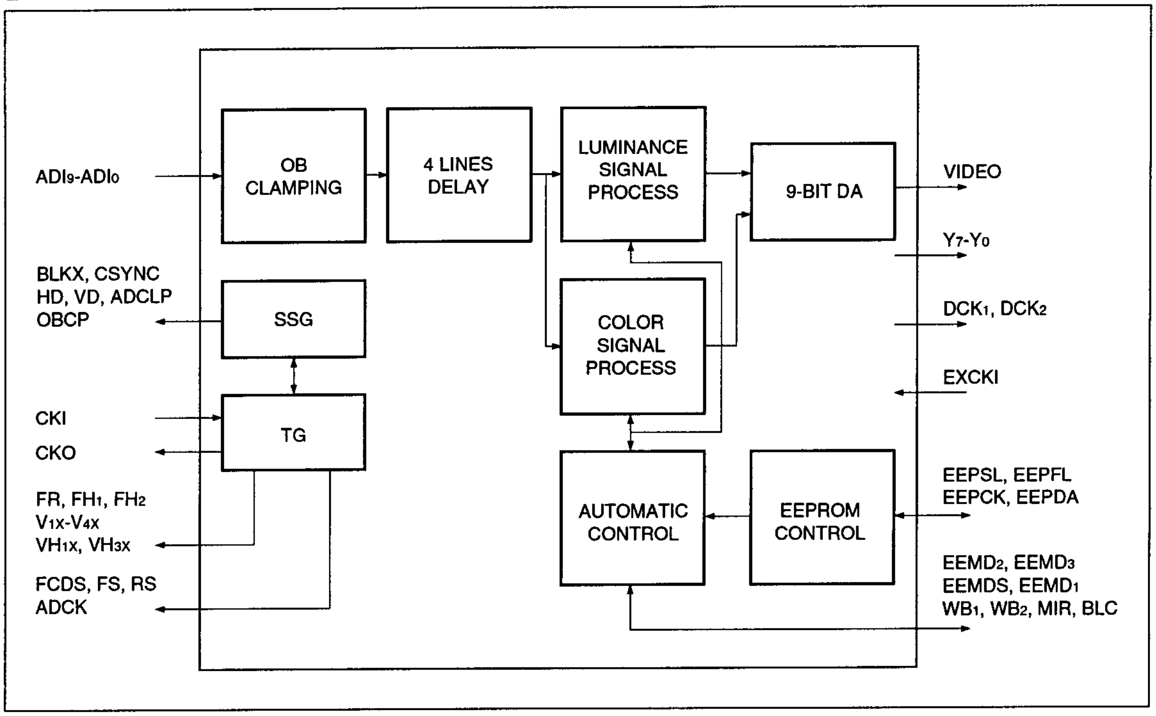
PIN CONNECTIONS

80-PIN LQFP TOP VIEW



(P-LQFP080-1212)

BLOCK DIAGRAM



PIN DESCRIPTION

PIN NO.	SYMBOL	IO SYMBOL	POLARITY	DESCRIPTION
1	ACL	ICSU		All reset
2	CKI	OSCI		Input for reference clock oscillator Connect to CKO (pin 3) with R. NTSC : 28.63636 MHz PAL : 28.375 MHz
3	CKO	OSCO		Output for reference clock oscillator. The output is the inverse of CKI (pin 2).
4	V_{DD}	–		Power supply input (+3.3 V)
5	GND	–		Ground
6	ADCK	OBF4M		Clock output for A/D converter Connect to ADCK of IR3Y48A1.
7	SCK	OBF4M		Clock output for setting parameter of IR3Y48A1
8	SDATA	OBF4M		Serial data output for setting parameter of IR3Y48A1
9	ADI_9	IC		Digital signal input (MSB)
10	ADI_8	IC		Digital signal input
11	ADI_7	IC		Digital signal input
12	ADI_6	IC		Digital signal input
13	ADI_5	IC		Digital signal input
14	ADI_4	IC		Digital signal input
15	V_{DD}	–		Power supply input (+3.3 V)
16	GND	–		Ground
17	ADI_3	IC		Digital signal input
18	ADI_2	IC		Digital signal input
19	ADI_1	IC		Digital signal input
20	ADI_0	IC		Digital signal input (LSB)
21	OBCP	OBF4M		Clamp pulse output for optical black
22	ADCLP	OBF4M		Clamp pulse output
23	BLKX	OBF4M		Blanking pulse output
24	EEPDA	IO4MU		Data input from EEPROM Connect to a data output pin of EEPROM. When setting internal register from an external device, use EEPCK, EEPFL and EEPSL together with EEPDA. This pin is for serial data input.
25	GND	–		Ground
26	V_{DD}	–		Power supply input (+3.3 V)
27	EEPCK	IO4MSU		Clock output for EEPROM Connect to clock input of EEPROM. When setting internal register from external device, this pin is used as serial clock.
28	EEPFL	ICU		Control for setting internal register from an external device Usually used at H level.
29	EEPSL	ICD		Control for setting internal register from external device Usually used at L level. When setting register, set EEPSL at H level.

PIN NO.	SYMBOL	IO SYMBOL	POLARITY	DESCRIPTION
30	WB_1	IO4MD		WB setting. Use together with WB_1 and WB_2 00 (WB_2, WB_1) : Auto white balance 01 : WB_1 mode 10 : WB_2 mode 11 : WB_3 mode These pins are 0 bit (WB_1) and 1st-bit (WB_2) of UV output in output digital YUV mode.
31	WB_2	IO4MD		
32	MIR	IO4MD		Setting for mirroring video output mode L : Normal H : Mirroring This pin is 2nd-bit of UV output in output digital YUV mode.
33	BLC	IO4MD		Switching internal register for exposure-standard This pin is 3rd-bit of UV output in digital output mode.
34	GNDDA	–		Ground for internal D/A converter
35	V_{DDDA}	–		Power supply for internal D/A converter Connect to DC 3.3 V power supply (+3.3 V).
36	VB	DAO		DC output of internal D/A converter. Connect to ground pin via capacitor.
37	I_{REF}	DAO		DC output of internal D/A converter. Connect to ground pin via register.
38	V_{REF}	DAI		DC reference input for internal D/A converter Connect to DC power supply (+1.0 V).
39	GNDDA	–		Ground for internal D/A converter.
40	VIDEO	DAO		Analog video output
41	EEMDS	IO4MU		Switching electronic shutter control Use together with EEMDS, $EEMD_1$, $EEMD_2$ and $EEMD_3$. Refer to "**Electronic Shutter Speed Setting**" in AUTOMATIC CAMERA FUNCTION CONTROL. These pins are 4th to 7th-bit of UV output in digital output mode. When in line lock mode, $EEMD_2$: H reset $EEMD_3$: V reset
42	$EEMD_1$	IO4MU		
43	$EEMD_2$	IO4MU		
44	$EEMD_3$	IO4MU		
45	GND	–		Ground
46	V_{DD}	–		Power supply input (+3.3 V).
47	DCK_1	OBF4M		Clock output synchronized with digital output Switchable among CSYNC, CBLK or L level.
48	DCK_2	OBF4M		ID pulse output of UV signal for digital output When in analog output, output is KEI or L level. KEI pulse : At power-on, begin with L level. When shutter speed is 1/60 s (PAL 1/50 s) and PGA gain is more than the value in address 92h, it goes to H level and becomes stable.
49	EXCKI	ICSU		Input for external clock
50	Y_0	OBF4M		Digital video signal output Use together with Y_7 (MSB) to Y_0 (LSB). UYVY signal or illumination signal output (according to the register).
51	Y_1	OBF4M		
52	Y_2	OBF4M		
53	Y_3	OBF4M		
54	GND	–		Ground

PIN NO.	SYMBOL	IO SYMBOL	POLARITY	DESCRIPTION
55	V_{DD}	–		Power supply input (+3.3 V)
56	Y_4	OBF4M		Digital video signal output Use together with Y_7 (MSB) to Y_0 (LSB). UYVY signal or illumination signal output (according to the register)
57	Y_5	OBF4M		
58	Y_6	OBF4M		
59	Y_7	OBF4M		
60	HD	OBF4M		Horizontal drive pulse output It is able to select horizontal drive pulse for drive timing and video output timing from BELL pulse, HREF pulse and L level. BELL pulse : The signal that goes to H level 1 time per 1 field.
61	VD	OBF4M		Vertical drive pulse output It is able to select from VD, CSYNC and VS outputs for drive timing and video output timing.
62	V_{1X}	OBF4M		CCD vertical drive pulse output Connect each pin to CCD via V driver IC.
63	V_{2X}	OBF4M		
64	V_{3X}	OBF4M		
65	V_{4X}	OBF4M		
66	V_{DD}	–		Power supply input (+3.3 V)
67	GND	–		Ground
68	VH_{1X}	OBF4M		Pulse output for reading charges Connect each pin to CCD via V driver IC.
69	VH_{3X}	OBF4M		
70	OFDX	OBF4M		OFD pulse output. Connect each pin to CCD via V driver IC.
71	V_{DD}	–		Power supply input (+3.3 V)
72	GND	–		Ground
73	FR	OBF12M		Reset pulse output. Connect each pin to CCD via capacitor.
74	FH_1	OBF12M		Horizontal transmit pulse output Connect to CCD.
75	FH_2	OBF12M		
76	V_{DD}	–		Power supply input (+3.3 V)
77	GND	–		Ground
78	RS	OBF4M		Pulse output for sample hold When using IR3Y48A1, connect to CSN pin for parameter setting.
79	FS	OBF4M		Pulse output for sample hold
80	FCDS	OBF4M		Pulse output for sample hold

IC : Input pin
ICU : Input pin with pull-up resistor
ICD : Input pin with pull-down resistor
ICSU : Schmidt input pin with pull-up resistor
DAI : Input pin for D/A converter
OSCI : Input pin for oscillation
OBF4M : Output pin
OBF12M : Output pin
DAO : Output pin for D/A converter
OSCO : Output pin for oscillation
IO4MU : Input/output pin with pull-up resistor
IO4MD : Input/output pin with pull-down resistor
IO4MSU : Input/output pin with pull-down resistor (schmidt input)

DSP REGISTER TABLE

ADDRESS	NAME	BIT	CONTENTS
00h	STOP_EEPROM	[7 : 0]	Stop reading from EEPROM only when EEPROM data is FF.
01h	LPF_TH	[7]	H : Luminance signal processing without LPF (when using B/W CCD)
	CCD_SEL	[6 : 5]	00 : 270 k pixel CCD (NTSC) 01 : 410 k pixel CCD (NTSC) 10 : 320 k pixel CCD (PAL) 11 : 470 k pixel CCD (PAL)
	ADTI	[4 : 3]	Input data timing adjustment 00 : Reference 01 : 1 clock delay 10 : 1 clock forward 11 : 2 clocks forward
		[2]	1 : Latch with inverted clock
	SEL_CDS	[1 : 0]	Fixed to 1X (IR3Y48A1)
02h	NI	[6]	0 : Interlace 1 : Non-interlace
	MODE_OUT_SIG	[5 : 3]	Select output mode. 000 : Analog video output EXCKI : Vertical reset pulse input 001 : Analog video output EXCKI : 8 fsc clock input EEMD$_2$: Horizontal reset pulse input EEMD$_3$: Vertical reset pulse input 010 : Analog video output EEMD$_2$: Horizontal reset pulse input EEMD$_3$: Vertical reset pulse input 100 : YUV digital video output : Clock rate of video data pixel-CK 101 : YUV digital video output : Clock rate of video data EXCKI 110 : UYVY digital video output : Clock rate of video data EXCKI 011, 111 are prohibited.
	START_EE	[2]	Shutter speed at power-on 0 : minimum 1 : maximum
	AGC_FIX	[1]	PGA control 0 : Auto 1 : Fixed
	OB_SEL	[0]	Carrier balance control 0 : Auto 1 : Fixed
03h	HD_SEL	[6 : 5]	Select output signal from HD pin 00 : HD output (CCD drive timing) 01 : HD output (video output timing) 10 : BELL pulse (in analog video output), HREF (in digital video output) 11 : Fixed to L level
	VD_SEL	[4 : 3]	Select output signal from VD pin 00 : VD output (CCD drive timing) 01 : VD output (video output timing) 10 : Fixed to L level (in analog video output), VS (in digital video output) 11 : Fixed to L level (in analog video output), CSYNC (in digital video output)
	DCK1_SEL	[2 : 1]	Select output signal from DCK$_1$ pin (in analog video output) 00 : CSYNC 01 : CBLNK 1X : Fixed to L level
	DCK2_SEL	[0]	Select output signal from DCK$_2$ pin (in analog video output) 0 : Fluorescent signal 1 : Fixed to L level
04h	SW_CTRL	[7 : 0]	Electronic shutter control (EEMDS, EEMD$_1$, EEME$_2$, EEMD$_3$), mirror video output (MIR [MSB]), internal register for exposure-standard (BLC) and white balance (WB$_2$, WB$_1$ [LSB]) are set when selecting digital output mode with MODE_OUT_SIG (address 02h). Shutter control of EEMD$_2$ and EEMD$_3$ is set by the register of SW_CTRL and that of EEMDS and EEMD$_1$ is set by pin 41 and pin 42 when setting "001" and "010" with MODE_OUT_SIG (address 02h).

ADDRESS	NAME	BIT	CONTENTS
05h	MIN_SH_SEL	[7]	Select minimum shutter speed 0 : 1/60 s (1/50 s) 1 : 1/100 s (1/120 s)
	MAX_SH	[6 : 0]	Restriction in maximum shutter speed (When EEMDS, EEMD1, EEMD2, EEMD3 = 4' b1110)
06h	REF_IRIS1	[7 : 0]	Reference of exposure
07h	CTLD_AGC	[7 : 0]	Outside range of error of exposure reference (Hysteresis range of IRIS and PGA tweaking range)
08h	CTLD_0	[7 : 0]	Inside range of error of exposure reference (Exposure control is stopped in REF_IRIS±CTLD_0)
09h	REF_IRIS2	[7 : 0]	Exposure reference in condition against light (When BLC = H)
0Ah	CLIP_IRIS	[7 : 0]	Ceiling clip in accumulate exposure data
0Bh	UW_E1	[7 : 0]	Downward weight factor 1 in calculation of exposure. (upper of screen)
0Ch	UW_E2	[7 : 0]	Downward weight factor 2 in calculation of exposure.
0Dh	UW_E3	[7 : 0]	Downward weight factor 3 in calculation of exposure.
0Eh	UW_E4	[7 : 0]	Downward weight factor 4 in calculation of exposure.
0Fh	UW_E5	[7 : 0]	Downward weight factor 5 in calculation of exposure.
10h	UW_E6	[7 : 0]	Downward weight factor 6 in calculation of exposure.
11h	UW_E7	[7 : 0]	Downward weight factor 7 in calculation of exposure.
12h	UW_E8	[7 : 0]	Downward weight factor 8 in calculation of exposure. (lower of screen) Sum of UW_E1 to UW_E8 must be 256d.
13h	CW_E	[6 : 0]	Ratio of downward IRIS against center
14h	CWP_E	[5 : 0]	Center point, position of left-upper area.
15h	CWA_E	[5 : 0]	Center point, size of area.
16h	EE_DIV_STP	[6 : 4]	Select dividing value of shutter speed control.
	LPFE_O	[3 : 2]	Select LPF of IRIS data in PGA normal adjustment.
	LPFE_I	[1 : 0]	Select LPF of IRIS data in PGA tweak.
17h	P_HEE	[7 : 0]	Ratio of luminance H peak of IRIS data
18h	P_LEE	[7 : 0]	Ratio of luminance L peak of IRIS data
19h	MOD8	[4]	Select peak accumulation. 0 : Avg. of 8 pixels 1 : Avg. of 4 pixels
	IRIS_DLY	[3 : 2]	Reduction of IRIS control in normal operation. 00 : Operating always 01 : Operating each 2VD timing 10 : Operating each 4VD timing 11 : Operating each 8VD timing
	IRIS_DLY	[1 : 0]	Reduction of IRIS control in PGA tweak. 00 : Operating always 01 : Operating each 2VD timing 10 : Operating each 4 VD timing 11 : Operating each 8VD timing
1Ah	AG_DIV_STP	[7 : 5]	Select dividing value of PGA control.
	AG_GAIN	[4 : 0]	Number of steps in PGA gain
1Bh	MAX_AGC	[7 : 0]	Upper limitation of PGA control.
1Ch	REF_AGC	[7 : 0]	Lower limitation of PGA control (initial value of PGA at power-on).
1Dh	S_38M_GA	[7 : 0]	Fixed PGA gain [7 : 0 (LSB)]
1Eh	S_38M_GA_U	[3]	Fixed PGA gain when using IR3Y48A1 [8 (MSB)]
	S_38M_MX	[2 : 0]	IR3Y48A1 minimum gain [1 : 0] 00 : 0 01 : +6 dB 10 : +12 dB 11 : −2 dB

ADDRESS	NAME	BIT	CONTENTS
1Fh	S_38M_OFS	[7]	Offset auto adjustment. 0 : Auto 1 : Fixed (when using IR3Y48A1)
		[6 : 0]	Factor in fixed offset mode Fixed to 40h when using IR3Y48A1.
20h	CSEPR	[7 : 0]	R side factor of color separation (positive value)
21h	CSEPB	[7 : 0]	B side factor of color separation (positive value)
22h	CB_R	[7 : 0]	R side factor of carrier balance (complement of 2)
23h	CB_B	[7 : 0]	B side factor of carrier balance (complement of 2)
24h	C_GAM	[5 : 3]	Select characteristics of color gamma.
	YL_SEL	[2 : 1]	Manner of YL signal production ([2 : 1]) 00 : Avg. of 3 lines 01 : Each R, B line 1X : Fixed ratio
	C1_RB_SEL	[0]	Manner of RG signal production 0 : Use color separation factor (address 20h, 21h) 1 : Use fixed color separation factor.
25h	MODE_MAT	[7]	Matrix factor 0 : Unsigned 1 : Signed
	LC_ON_RB	[6]	1 : Operation against line crawl in color processing.
	YL_SUB	[5]	1 : Set YL to 0 in chrominance generation.
	UV_CTRL1	[4]	Switch order of UV digital output
	SEL_RB	[3]	Swap R and B after color separation.
	SEL_RB2	[2]	Swap R – Y and B – Y in output
	SPCTRL	[1]	Switch attributes of SP1 and SP2.
	IDCO	[0]	Switch attribute of color separation HG.
26h	MAX_WBR	[7 : 0]	Upper limit of R side range of AWB gain (9 bits data which includes 1 at LSB)
27h	MIN_WBR	[7 : 0]	Lower limit of R side range of AWB gain (9 bits data which includes 1 at LSB)
28h	MAX_WBB	[7 : 0]	Upper limit of B side range of AWB gain (9 bits data which includes 1 at LSB)
29h	MIN_WBB	[7 : 0]	Lower limit of B side range of AWB gain (9 bits data which includes 1 at LSB)
2Ah	JMP_OFF	[4]	0 : Normal 1 : Suppress AWB skipping
	AWB_HIGH	[3]	0 : Normal 1 : Force fast processing in small frame
	MAX_IQAREA	[2]	0 : Address 36h to 3Dh 1 : Fix WB frame to maximum.
	IQ_LPF	[1 : 0]	Select LPF of AWB I, Q. 00 : Avg. of 4 V 01 : Avg. of 2 V 1X : Non
2Bh	K_WBR_H	[7 : 0]	R side multiplier of capture speed in AWB fast processing.
2Ch	K_WBB_H	[7 : 0]	B side multiplier of capture speed in AWB fast processing.
2Dh	CMP_CT	[7 : 0]	Number of operations of white balance (each CMP_CT x VD timing)
2Eh	AWB_HCL	[7 : 0]	Initial value of AWBHCL
2Fh	AWB_LCL	[7 : 0]	Initial value of AWBLCL
30h	REF_WBPK	[7 : 0]	Reference data in calculation of intercept level of AWB accumulated luminance
31h	K_CL	[7 : 0]	H peak ratio in calculation of intercept level of AWB accumulated luminance
32h	K_WBCL	[7 : 0]	Multiplier in calculation of intercept level of AWB accumulated luminance
33h	INT_I_R_Y	[7]	AWB detected data 0 : I, Q 1 : R – Y, B – Y
	CW_IQ	[6 : 0]	Ratio of AWB weighted center and downward.

ADDRESS	NAME	BIT	CONTENTS
34h	CWPA_IQ	[7 : 0]	Position and area of AWB center.
35h	CTLD_AW0	[7 : 0]	Reset range of WB frame (compared with IRIS)
36h	AWB_IP_L	[7 : 0]	Outside, I-axis positive of AWB detect area (in fast processing)
37h	AWB_IM_L	[7 : 0]	Outside, I-axis negative of AWB detect area (in fast processing)
38h	AWB_QP_L	[7 : 0]	Outside, Q-axis positive of AWB detect area (in fast processing)
39h	AWB_QM_L	[7 : 0]	Outside, Q-axis negative of AWB detect area (in fast processing)
3Ah	AWB_IP_S	[7 : 0]	Inside, I-axis positive of AWB detect area (in normal processing)
3Bh	AWB_IM_S	[7 : 0]	Inside, I-axis negative of AWB detect area (in normal processing)
3Ch	AWB_QP_S	[7 : 0]	Inside, Q-axis positive of AWB detect area (in normal processing)
3Dh	AWB_QM_S	[7 : 0]	Inside, Q-axis negative of AWB detect area (in normal processing)
3Eh	AWB_IW_L	[6 : 0]	White area, I-axis, outside (for hysteresis).
3Fh	AWB_QW_L	[6 : 0]	White area, Q-axis, outside (for hysteresis).
40h	AWB_IW_S	[7 : 4]	White area, I-axis, inside (for targeted white area).
	AWB_QW_S	[3 : 0]	White area, Q-axis, inside (for targeted white area).
41h	AWB_C_I	[7 : 4]	WB convergence orientation, I-axis coordinate (complement of 2)
	AWB_C_Q	[3 : 0]	WB convergence orientation, Q-axis coordinate (complement of 2)
42h	WBR1	[7 : 0]	WB_1 R side constant (9 bits data which includes 0 at MSB)
43h	WBB1	[7 : 0]	WB_1 B side constant (9 bits data which includes 0 at MSB)
44h	WBR2	[7 : 0]	WB_2 R side constant (9 bits data which includes 0 at MSB)
45h	WBB2	[7 : 0]	WB_2 B side constant (9 bits data which includes 0 at MSB)
46h	WBR3	[7 : 0]	WB_3 R side constant (9 bits data which includes 0 at MSB)
47h	WBB3	[7 : 0]	WB_3 B side constant (9 bits data which includes 0 at MSB)
48h	REF_GA_R1M	[7 : 0]	Chrominance gain of R – Y negative direction when WB_1 is fixed or auto-controlled (present WBR factor ≤ WBR1).
49h	REF_GA_B1M	[7 : 0]	Chrominance gain of B – Y negative direction when WB_1 is fixed or auto-controlled (present WBR factor ≤ WBR1).
4Ah	REF_GA_R1P	[7 : 0]	Chrominance gain of R – Y positive direction when WB_1 is fixed or auto-controlled (present WBR factor ≤ WBR1).
4Bh	REF_GA_B1P	[7 : 0]	Chrominance gain of B – Y positive direction when WB_1 is fixed or auto-controlled (present WBR factor ≤ WBR1).
4Ch	REF_GA_R2M	[7 : 0]	Chrominance gain of R – Y negative direction when WB_2 is fixed or auto-controlled (present WBR factor ≤ WBR2).
4Dh	REF_GA_B2M	[7 : 0]	Chrominance gain of B – Y negative direction when WB_2 is fixed or auto-controlled (present WBR factor ≤ WBR2).
4Eh	REF_GA_R2P	[7 : 0]	Chrominance gain of R – Y positive direction when WB_2 is fixed or auto-controlled (present WBR factor ≤ WBR2).
4Fh	REF_GA_B2P	[7 : 0]	Chrominance gain of B – Y positive direction when WB_2 is fixed or auto-controlled (present WBR factor ≤ WBR2).
50h	REF_GA_R3M	[7 : 0]	Chrominance gain of R – Y negative direction when WB_3 is fixed or auto-controlled (present WBR factor ≤ WBR3).
51h	REF_GA_B3M	[7 : 0]	Chrominance gain of B – Y negative direction when WB_3 is fixed or auto-controlled (present WBR factor ≤ WBR3).

ADDRESS	NAME	BIT	CONTENTS
52h	REF_GA_R3P	[7 : 0]	Chrominance gain of R – Y positive direction when WB_3 is fixed or auto-controlled (present WBR factor ≤ WBR3).
53h	REF_GA_B3P	[7 : 0]	Chrominance gain of B – Y positive direction when WB_3 is fixed or auto-controlled (present WBR factor ≤ WBR3).
54h	K_GA_R1M	[6 : 0]	Chrominance gain slope of R – Y negative direction in WB auto control (WBR1 < present WBR < WBR2)
55h	K_GA_B1M	[6 : 0]	Chrominance gain slope of B – Y negative direction in WB auto control (WBR1 < present WBR < WBR2)
56h	K_GA_R1P	[6 : 0]	Chrominance gain slope of R – Y positive direction in WB auto control (WBR1 < present WBR < WBR2)
57h	K_GA_B1P	[6 : 0]	Chrominance gain slope of B – Y positive direction in WB auto control (WBR1 < present WBR < WBR2)
58h	K_GA_R2M	[6 : 0]	Chrominance gain slope of R – Y negative direction in WB auto control (WBR2 < present WBR < WBR3)
59h	K_GA_B2M	[6 : 0]	Chrominance gain slope of B – Y negative direction in WB auto control (WBR2 < present WBR < WBR3)
5Ah	K_GA_R2P	[6 : 0]	Chrominance gain slope of R – Y positive direction in WB auto control (WBR2 < present WBR < WBR3)
5Bh	K_GA_B2P	[6 : 0]	Chrominance gain slope of B – Y positive direction in WB auto control (WBR2 < present WBR < WBR3)
5Ch	REF_MAT_R1M	[5 : 0]	Matrix correction factor of R – Y negative direction when WB_1 is fixed or autocontrolled (present WBR factor ≤ WBR1).
5Dh	REF_MAT_B1M	[5 : 0]	Matrix correction factor of B – Y negative direction when WB_1 is fixed or autocontrolled (present WBR factor ≤ WBR1).
5Eh	REF_MAT_R1P	[5 : 0]	Matrix correction factor of R – Y positive direction when WB_1 is fixed or autocontrolled (present WBR factor ≤ WBR1).
5Fh	REF_MAT_B1P	[5 : 0]	Matrix correction factor of B – Y positive direction when WB_1 is fixed or autocontrolled (present WBR factor ≤ WBR1).
60h	REF_MAT_R2M	[5 : 0]	Matrix correction factor of R – Y negative direction when WB_2 is fixed or autocontrolled (present WBR factor = WBR2).
61h	REF_MAT_B2M	[5 : 0]	Matrix correction factor of B – Y negative direction when WB_2 is fixed or autocontrolled (present WBR factor = WBR2).
62h	REF_MAT_R2P	[5 : 0]	Matrix correction factor of R – Y positive direction when WB_2 is fixed or autocontrolled (present WBR factor = WBR2).
63h	REF_MAT_B2P	[5 : 0]	Matrix correction factor of B – Y positive direction when WB_2 is fixed or autocontrolled (present WBR factor = WBR2).
64h	REF_MAT_R3M	[5 : 0]	Matrix correction factor of R – Y negative direction when WB_3 is fixed or autocontrolled (present WBR factor = WBR3).
65h	REF_MAT_B3M	[5 : 0]	Matrix correction factor of B – Y negative direction when WB_3 is fixed or autocontrolled (present WBR factor = WBR3).
66h	REF_MAT_R3P	[5 : 0]	Matrix correction factor of R – Y positive direction when WB_3 is fixed or autocontrolled (present WBR factor = WBR3).

ADDRESS	NAME	BIT	CONTENTS
67h	REF_MAT_B3P	[5 : 0]	Matrix correction factor of B – Y positive direction when WB_3 is fixed or autocontrolled (present WBR factor = WBR3).
68h	K_MAT_R1M	[7 : 0]	Matrix correction slope factor of R – Y negative direction in WB auto control (WBR1 < present WBR < WBR2)
69h	K_MAT_B1M	[7 : 0]	Matrix correction slope factor of B – Y negative direction in WB auto control (WBR1 < present WBR < WBR2)
6Ah	K_MAT_R1P	[7 : 0]	Matrix correction slope factor of R – Y positive direction in WB auto control (WBR1 < present WBR < WBR2)
6Bh	K_MAT_B1P	[7 : 0]	Matrix correction slope factor of B – Y positive direction in WB auto control (WBR1 < present WBR < WBR2)
6Ch	K_MAT_R2M	[7 : 0]	Matrix correction slope factor of R – Y negative direction in WB auto control (WBR2 < present WBR < WBR3)
6Dh	K_MAT_B2M	[7 : 0]	Matrix correction slope factor of B – Y negative direction in WB auto control (WBR2 < present WBR < WBR3)
6Eh	K_MAT_R2P	[7 : 0]	Matrix correction slope factor of R – Y positive direction in WB auto control (WBR2 < present WBR < WBR3)
6Fh	K_MAT_B2P	[7 : 0]	Matrix correction slope factor of B – Y positive direction in WB auto control (WBR2 < present WBR < WBR3)
70h	CKIL_OFF	[6]	1 : Color killer OFF
	COL_Y	[5 : 0]	Start point of luminance color suppression in maximum PGA gain.
71h	COL_S	[7 : 0]	Start point of low luminance color suppression (PGA gain).
72h	COL_H	[5 : 0]	Low luminance color suppression gain.
73h	CKI_HCL	[7 : 0]	Start level of high luminance color suppression.
74h	CKI_LCL	[7 : 0]	Start level of low luminance color suppression.
75h	CKI_HLGA	[7 : 4]	High luminance color suppression gain.
		[3 : 0]	Low luminance color suppression gain.
76h	CKI_HLTI	[5 : 3]	Timing adjustment of high luminance color suppression : –2 to +2
		[2 : 0]	Timing adjustment of low luminance color suppression : –2 to +2
77h	CKI_HECL	[7 : 0]	Start point of horizontal edge color suppression.
78h	CKI_EVCL	[7 : 0]	Start point of vertical edge color suppression.
79h	CKI_EGA	[7 : 4]	Gain of horizontal edge color suppression.
		[3 : 0]	Gain of vertical edge color suppression.
7Ah	NSUP_R	[7 : 4]	R – Y signal low level suppression
	NSUP_B	[3 : 0]	B – Y signal low level suppression
7Bh	LC_ON_YL	[7]	1 : Execute measure against line crawl in processing luminance signal.
	Y_GAM	[6 : 4]	Select characteristics of luminance gamma.
	SEL_LPF_Y	[3]	Select characteristics of luminance LPF.
	Y_SEL	[2]	Switch luminance signal processing 0 : Use only 1H 1 : 3-line process
	VAPT_OFF	[1]	1 : Vertical aperture is OFF
	HAPT_OFF	[0]	1 : Horizontal aperture is OFF
7Ch	HAPT_SEL	[7]	Switch characteristics of horizontal aperture. 0 : (–1 + Z1) (1 – Z2) 1 : (–1 + Z1) (1 – Z1)
	APT_HTIM	[6 : 5]	Timing of horizontal aperture : –1 to +1
	APT_HGA	[4 : 0]	Initial value of APT_HGA (gain of horizontal edge signal)

ADDRESS	NAME	BIT	CONTENTS
7Dh	APT_HCL	[6 : 0]	Suppression level of horizontal edge signal.
7Eh	APT_VGA	[4 : 0]	Initial value of APT_VGA (gain of vertical edge signal)
7Fh	APT_VCL	[6 : 0]	Suppression level of vertical edge signal.
80h	APT_S	[7 : 0]	Start point of edge signal suppression (PGA gain).
81h	APT_H	[5 : 0]	Gain of edge signal suppression.
82h	APT_Y	[5 : 0]	Start point of edge signal suppression in maximum PGA gained luminance.
83h	CKI_HCL2	[7 : 0]	Luminance suppression point of high luminance aperture.
84h	CKI_ETI	[6]	Select level of edge signal, used in internal calculation. 1 : 1/4 times
		[5 : 3]	Delete timing of horizontal edge : –2 to +2
		[2 : 0]	Delete timing of vertical edge : –2 to +2
85h	LC_K1	[7 : 0]	Difference of 0H, 2H signal allowed level, for judgment of line crawl.
86h	LC_K2	[7 : 0]	Difference of R, B signal allowed level, for judgment of line crawl.
87h	LC_MAX	[7 : 0]	Judgment of luminance level, for judgment of line crawl.
88h	SETUP	[6]	Switch CBLK level.
		[5 : 0]	Adjustment of setup level (complement of 2).
89h	BAS_R	[7]	Sign of burst level R – Y 1 : – direction 0 : + direction
		[6 : 0]	Burst level R – Y.
8Ah	BAS_B	[7]	Sign of burst level B – Y 1 : – direction 0 : + direction
		[6 : 0]	Burst level B – Y (sign + absolute value).
8Bh	OUTGA	[6]	1 : Mute in encoder.
		[5]	1 : Stop adding SYNC to analog output.
		[4 : 0]	Gain of analog output (1 time at 10h).
8Ch	SYNCLEV	[7 : 0]	Adjustment of SYNC level.
8Dh	MUTE_OUT	[7]	1 : Disable output mute at power-on.
		[6 : 0]	Period of mute (MUTE_OUT x 2 vertical period)
8Eh	SEL_FH	[7]	Switch attribute of FH 1 : Inverted
	SEL_FR	[6]	Switch attribute of FR 1 : Inverted
	SEL_ADCK	[5 : 3]	ADCK phase adjustment When using 270 k, 320 k-pixel CCDs 000 : standard to 101 : 300° (delayed from "000" to "101" every 60°.) When using 410 k, 470 k-pixel CCDs 000 : standard to 101 : 270° (delayed from "000" to "101" every 45°.)
	SEL_FS	[2 : 0]	FS phase adjustment 000 : standard to 111 : 14 ns delay (delayed from "000" to "111" every 2 ns.)
8Fh	SEL_FH2	[7 : 6]	FH_2 phase adjustment 00 : standard 01 : 1 ns delay 10 : 2 ns delay 11 : 3 ns delay
	SEL_FCDS	[5 : 3]	FCDS phase adjustment 000 : standard to 111 : 14 ns delay (delayed from "000" to "111" every 2 ns.)
	SEL_RS	[2 : 0]	RS phase adjustment 000 : standard to 111 : 14 ns delay (delayed from "000" to "111" every 2 ns.)
90h	STANDBY	[6]	1 : Standby
		[5 : 0]	Period of return from standby (STANDBY x vertical period)

ADDRESS	NAME	BIT	CONTENTS
91h	KNEE	[7]	1 : Invert OBCP clock
	INV_DCK2	[6]	1 : Invert DCK_2
	INV_DCK1	[5]	1 : Invert DCK_1
	BUSY_SEL	[4]	1 : Reset auto control factor, when EEPSL is at H.
	EI_ON_SEL	[3]	1 : Enable KEI pulse function.
	HRI_SEL	[2]	1 : Invert HRES (minus attribute)
	VRI_SEL	[1]	1 : Invert VRES (minus attribute)
	IN_VRES	[0]	Select vertical reset timing. 0 : Reset at CSYNC pulse timing. 1 : Reset at VD pulse timing.
92h	KEI_KEISU	[7 : 0]	Gain of PGA which produces KEI pulse.
93h	ENCIN_PH	[3]	Latch encoder clock inverted.
		[2]	1 : Enable DFF.
	VARI_ENC	[1 : 0]	Delay adjustment of addition of luminance and color modulation. (Delay of color signal) 00 : 0 clock delay to 11 : 3 clocks delay (delayed from "00" to "11" every 1 clock .) 1 clock : Original clock
94h	ANA_VARI	[6 : 4]	Delay adjustment of addition of luminance and color modulation. (Delay of luminance signal) 101 : −3 clocks delay to 011 : 3 clocks delay (delayed from "101" to "011" every 1 clock .) 1 clock : Pixel CK (complement of 2)
	VARI_Y	[3 : 0]	Timing adjustment of luminance processing. 1001 : −7 clocks delay to 0111 : 7 clocks delay (delayed from "1001" to "0111" every 1 clock.) 1 clock : Pixel CK (complement of 2)
95h	BUNSYU8_SEL	[7]	Output 1/8 of original clock from DCK_1.
	TEST	[6]	Test mode. Set 0 in normal operation. (The LR38603 does not read EEPROM and registers are set by serial data.)
	STDBY	[5]	Make D/A converter standby.
	CHG_CKIL	[4]	Swap R and B of color killer.
	CHG_WB	[3]	Swap R and B of white balance.
	CHG_MTX	[2]	Swap R and B of matrix input.
	CHG_CCD4	[1]	Swap U and V of digital output.
	HG_YL_SEL	[0]	Swap YL line selection for each R and B.
96h	REF_AW	[7 : 0]	Factor for white detect correction
97h	REF_BW	[7 : 0]	Factor for white detect correction
98h	REF_CW	[7 : 0]	Factor for white detect correction
99h	REF_DW	[7 : 0]	Factor for white detect correction
9Ah	REF_AB	[7 : 0]	Factor for black detect correction
9Bh	REF_BB	[7 : 0]	Factor for black detect correction
9Ch	REF_CB	[7 : 0]	Factor for black detect correction

ADDRESS	NAME	BIT	CONTENTS
9Dh	REF_DB	[7 : 0]	Factor for black detect correction
9Eh	AWNC_SEL	[5 : 0]	ON/OFF control signal for each condition.
9Fh	APT_O_LIM	[7 : 0]	Limiter of aperture output.
A0h	WN00H	[7 : 0]	Lower bits of horizontal coordinate 1 of white defect.
A1h	WN00V	[7 : 0]	Lower bits of vertical coordinate 1 of white defect.
A2h	WN00HV	[3 : 0]	[3 : 2] Upper bits of vertical coordinate 1 of white defect. [1 : 0] Upper bits of horizontal coordinate 1 of white defect.
A3h	WN01H	[7 : 0]	Lower bits of horizontal coordinate 2 of white defect.
A4h	WN01V	[7 : 0]	Lower bits of vertical coordinate 2 of white defect.
A5h	WN01HV	[3 : 0]	[3 : 2] Upper bits of vertical coordinate 2 of white defect. [1 : 0] Upper bits of horizontal coordinate 2 of white defect.
A6h	WN02H	[7 : 0]	Lower bits of horizontal coordinate 3 of white defect.
A7h	WN02V	[7 : 0]	Lower bits of vertical coordinate 3 of white defect.
A8h	WN02HV	[3 : 0]	[3 : 2] Upper bits of vertical coordinate 3 of white defect. [1 : 0] Upper bits of horizontal coordinate 3 of white defect.
A9h	WN03H	[7 : 0]	Lower bits of horizontal coordinate 4 of white defect.
AAh	WN03V	[7 : 0]	Lower bits of vertical coordinate 4 of white defect.
ABh	WN03HV	[3 : 0]	[3 : 2] Upper bits of vertical coordinate 4 of white defect. [1 : 0] Upper bits of horizontal coordinate 4 of white defect.
ACh	WN04H	[7 : 0]	Lower bits of horizontal coordinate 5 of white defect.
ADh	WN04V	[7 : 0]	Lower bits of vertical coordinate 5 of white defect.
AEh	WN04HV	[3 : 0]	[3 : 2] Upper bits of vertical coordinate 5 of white defect. [1 : 0] Upper bits of horizontal coordinate 5 of white defect.
AFh	WN05H	[7 : 0]	Lower bits of horizontal coordinate 6 of white defect.
B0h	WN05V	[7 : 0]	Lower bits of vertical coordinate 6 of white defect.
B1h	WN05HV	[3 : 0]	[3 : 2] Upper bits of vertical coordinate 6 of white defect. [1 : 0] Upper bits of horizontal coordinate 6 of white defect.
B2h	WN06H	[7 : 0]	Lower bits of horizontal coordinate 7 of white defect.
B3h	WN06V	[7 : 0]	Lower bits of vertical coordinate 7 of white defect.
B4h	WN06HV	[3 : 0]	[3 : 2] Upper bits of vertical coordinate 7 of white defect. [1 : 0] Upper bits of horizontal coordinate 7 of white defect.
B5h	WN07H	[7 : 0]	Lower bits of horizontal coordinate 8 of white defect.
B6h	WN07V	[7 : 0]	Lower bits of vertical coordinate 8 of white defect.
B7h	WN07HV	[3 : 0]	[3 : 2] Upper bits of vertical coordinate 8 of white defect. [1 : 0] Upper bits of horizontal coordinate 8 of white defect.
C0h	TST_SEL31	[7 : 0]	Test address (Set 00h)
C1h	TST_SEL32	[7 : 0]	Test address (Set 00h)
C2h	TST_SEL33	[0]	Test address (Set 00h)
C3h	TST_SEL1A	[7 : 0]	Test address (Set 00h)
C4h	TST_SEL1B	[7 : 0]	Test address (Set 00h)
C5h	TST_SEL1C	[7 : 0]	Test address (Set 00h)

ADDRESS	NAME	BIT	CONTENTS
C6h	TST_SEL1D	[1 : 0]	Test address (Set 00h)
C7h	TST_SEL1V1	[7 : 0]	Test address (Set 00h)
C8h	TST_SEL1V2	[7 : 0]	Test address (Set 00h)
C9h	TST_SEL1V3	[7 : 0]	Test address (Set 00h)
CAh	TST_SEL1V4	[7 : 0]	Test address (Set 00h)
CBh	TST_C2_OB3	[6 : 0]	Test address (Set 00h)
CCh	TST_C2_OB4	[6 : 0]	Test address (Set 00h)
CDh	TST_C2_DL1	[7 : 0]	Test address (Set 00h)
CEh	TST_C2_DL2	[7 : 0]	Test address (Set 00h)
CFh	TST_C2_YL	[5 : 0]	Test address (Set 00h)
D0h	TST_C2_GAMMA1	[7 : 0]	Test address (Set 00h)
D1h	TST_SSG_SEL	[2]	Test address (Set 00h)
	TST_C2_GAMMA2	[1 : 0]	Test address (Set 00h)
D2h	TST_C6_00	[7 : 0]	Test address (Set 00h)
D3h	TST_C6_01	[7 : 0]	Test address (Set 00h)
D4h	TST_C6_02	[6 : 0]	Test address (Set 00h)
D5h	TST_C4_IO0	[7 : 0]	Test address (Set 00h)
D6h	TST_C4_IO1	[4 : 0]	Test address (Set 00h)
D7h	TST_C4_IO2	[7 : 0]	Test address (Set 00h)
D8h	TST_C4_S0	[7 : 0]	Test address (Set 00h)
D9h	TST_C4_S1	[7 : 0]	Test address (Set 00h)
DAh	TST_C4_S2	[0]	Test address (Set 00h)
DBh	TST_C5_T0	[7 : 0]	Test address (Set 00h)
DCh	TST_C5_T1	[7 : 0]	Test address (Set 00h)
DDh	TST_C5_T2	[5 : 0]	Test address (Set 00h)
DEh	TST_SEL71	[7 : 0]	Test address (Set 00h)
DFh	TST_SEL72	[1 : 0]	Test address (Set 00h)
E0h	TEST_C8_00	[7 : 0]	Test address (Set 00h)
E1h	TEST_C8_01	[7 : 0]	Test address (Set 00h)
E2h	TEST_C8_02	[7 : 0]	Test address (Set 00h)
E3h	TEST_C8_03	[7 : 0]	Test address (Set 00h)
E4h	TEST_C8_04	[7 : 0]	Test address (Set 00h)
E5h	TEST_C8_05	[7 : 0]	Test address (Set 00h)
E6h	TEST_C8_06	[7 : 0]	Test address (Set 00h)
E7h	TEST_C8_07	[7 : 0]	Test address (Set 00h)
E8h	TEST_C8_08	[7 : 0]	Test address (Set 00h)
E9h	TEST_C8_09	[6 : 0]	Test address (Set 00h)
F0h	TST_REG1	[7 : 0]	Test address (Set 00h)
F1h	TST_REG2	[7 : 0]	Test address (Set 00h)
F2h	TST_REG3	[7 : 0]	Test address (Set 00h)
F3h	TST_REG4	[7 : 0]	Test address (Set 00h)

ADDRESS	NAME	BIT	CONTENTS
F4h	TST_REG5	[7 : 0]	Test address (Set 00h)
F5h	TST_REG6	[7 : 0]	Test address (Set 00h)
F6h	TST_REG7	[5 : 0]	Test address (Set 00h)
F7h	TST_REG8	[7 : 0]	Test address (Set 00h)
F8h	TST_REG9	[7 : 0]	Test address (Set 00h)
F9h	TST_REGA	[7 : 0]	Test address (Set 00h)
FAh	TST_REGB	[7 : 0]	Test address (Set 00h)
FBh	TST_SEL_REG	[5 : 0]	Test address (Set 00h)
FCh	WT_DAT30	[7 : 0]	Test address (Set 00h)
FDh	WT_DAT31	[6 : 0]	Test address (Set 00h)
FEh	TST_C5_WT3	[5 : 0]	Test address (Set 00h)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{DD}	−0.3 to +4.3	V
Input voltage	V_I	−0.3 to V_{DD} + 0.3	V
Output voltage	V_O	−0.3 to V_{DD} + 0.3	V
Storage temperature	T_{STG}	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input voltage	V_{DD}	3.0	3.3	3.6	V
Output voltage	T_{OPR}	−20	+25	+70	°C
Input clock	F_{CK}		28.6		MHz

ELECTRICAL CHARACTERISTICS 1

(V_{DD} = 3.3 V±10%, T_A = −20 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "High" voltage	V_{IH}		$0.8V_{DD}$			V	1
Input "Low" voltage	V_{IL}				$0.2V_{DD}$	V	
Input "High" voltage	V_{IH}		$0.8V_{DD}$			V	2
Input "Low" voltage	V_{IL}				$0.2V_{DD}$	V	
Hysteresis voltage	V_{HIS}		0.2			V	
Input "High" current	$\|I_{IH1}\|$	$V_{IN} = V_{DD}$			1.0	μA	3
Input "Low" current	$\|I_{IL1}\|$	V_{IN} = 0 V			1.0	μA	
Input "High" current	$\|I_{IH2}\|$	$V_{IN} = V_{DD}$			2.0	μA	4
Input "Low" current	$\|I_{IL2}\|$	V_{IN} = 0 V	10	33	70	μA	
Input "High" current	$\|I_{IH3}\|$	$V_{IN} = V_{DD}$			2.0	μA	5
Input "Low" current	$\|I_{IL3}\|$	V_{IN} = 0 V	40	100	300	μA	
Input "High" current	$\|I_{IH4}\|$	$V_{IN} = V_{DD}$	10	33	70	μA	6
Input "Low" current	$\|I_{IL4}\|$	V_{IN} = 0 V			2.0	μA	
Output "High" voltage	V_{OH1}	I_{OH} = +4 mA	$0.8V_{DD}$			V	7
Output "Low" voltage	V_{OL1}	I_{OL} = −4 mA			$0.2V_{DD}$	V	
Output "High" voltage	V_{OH3}	I_{OH} = +12 mA	$0.8V_{DD}$			V	8
Output "Low" voltage	V_{OL3}	I_{OL} = −12 mA			$0.2V_{DD}$	V	
Output "High" voltage	V_{OH4}	I_{OH} = +2 mA	$0.8V_{DD}$			V	9
Output "Low" voltage	V_{OL4}	I_{OL} = −3 mA			$0.2V_{DD}$	V	

NOTES :

1. Applied to inputs/outputs (IO4MU, IO4MD) and inputs (IC, ICU, ICD, OSCI).
2. Applied to input (ICSU), input/output (IO4MSU).
3. Applied to input (IC, OSCI).
4. Applied to inputs (ICU, ICSU), input/output (IO4MSU).
5. Applied to input/output (IO4MU).
6. Applied to input (ICD), input/output (IO4MD).
7. Applied to inputs/outputs (IO4MU, IO4MD), output (OBF4M).
8. Applied to output (OBF12M).
9. Applied to output (OSCO).

ELECTRICAL CHARACTERISTICS 2

(V_{DD} = 3.3±10%, T_A = –20 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Resolution	RES			9		Bit	1
Error of linearity	EL	V_{REF} = 1.0 V			±5.0	LSB	1
Error of differential linearity	ED	R_{REF} = 4.8 kΩ			±1.0	LSB	1
Full scaled current	IFS	R_{OUT} = 75 Ω		13		mA	1
Output impedance	R_{OUT}			75		Ω	1
Reference voltage	V_{REF}			1.0		V	2
Reference resistance	R_{REF}			4.8		kΩ	3

NOTES :

1. Applied to pin (VIDEO).
2. Applied to pin (V_{REF}).
3. Applied to pin (I_{REF}).

AUTOMATIC CAMERA FUNCTION CONTROL

Automatic Electronic Exposure Control

Electronic shutter speed is controlled so that the exposure control data approach the data of REF_IRIS1 (address 06h).

Under BLC mode, the data of REF_IRIS2 (address 09h) are available instead of REF_IRIS1.

If the exposure control data are less than the data of CTLD_AGC (address 07h), an electronic shutter speed is held. And then PGA gain is controlled so that the exposure control data will be less than the data of CTLD_0 (Address 08h).

If the exposure control data are greater than the data of CTLD_AGC (address 07h), exposure control starts again.

Electronic Shutter Speed Setting

Electronic shutter speeds below can be selected by either hardware or coefficient data.

EEMDS	EEMD1	EEMD2	EEMD3	ELECTRONIC SHUTTER SPEED	
				NTSC	PAL
0	0	0	0	1/60 s	1/50 s
0	0	0	1	1/100 s	1/120 s
0	0	1	0	1/250 s	1/250 s
0	0	1	1	1/500 s	1/500 s
0	1	0	0	1/1 000 s	1/1 000 s
0	1	0	1	1/2 000 s	1/2 000 s
0	1	1	0	1/5 000 s	1/5 000 s
0	1	1	1	1/10 000 s	1/10 000 s
1	0	0	0	1/20 000 s	1/20 000 s
1	0	0	1	1/50 000 s	1/50 000 s
1	0	1	0	1/100 000 s	1/100 000 s
1	0	1	1	1/30 s	1/25 s
1	1	0	0	1/15 s	1/12.5 s
1	1	0	1	1/7.5 s	1/6.25 s
1	1	1	0	AUTO 1/60 s to MAX_SH (address 05h)	AUTO 1/50 s to MAX_SH (address 05h)
1	1	1	1	AUTO 1/60 s to 1/100 000 s	AUTO 1/50 s to 1/100 000 s

A slower shutter speed of less than 1/60 s (1/50 s of PAL) can make images whose interval is every two fields, every four fields, etc.

VD pulse is also converted to the same frequency as the output image rate.

Electronic exposure control data come from the following equation using averaged luminance levels of 64 areas in one image, made by DSP.

Electronic exposure control data =
[{Weighted data 1 ① x (64 – CW_E (address 13h))
+ Weighted data 2 ② x CW_E}/64
x (256 – P_HEE (address 17h) – P_LEE (address 18h))
+ Top level ③ x P_HEE + Bottom level ④ x P_LEE]/256

Y_{11}	Y_{12}	Y_{13}	Y_{14}	Y_{15}	Y_{16}	Y_{17}	Y_{18}
Y_{21}	Y_{22}	Y_{23}	Y_{24}	Y_{25}	Y_{26}	Y_{27}	Y_{28}
Y_{31}	Y_{32}	Y_{33}	Y_{34}	Y_{35}	Y_{36}	Y_{37}	Y_{38}
Y_{41}	Y_{42}	Y_{43}	Y_{44}	Y_{45}	Y_{46}	Y_{47}	Y_{48}
Y_{51}	Y_{52}	Y_{53}	Y_{54}	Y_{55}	Y_{56}	Y_{57}	Y_{58}
Y_{61}	Y_{62}	Y_{63}	Y_{64}	Y_{65}	Y_{66}	Y_{67}	Y_{68}
Y_{71}	Y_{72}	Y_{73}	Y_{74}	Y_{75}	Y_{76}	Y_{77}	Y_{78}
Y_{81}	Y_{82}	Y_{83}	Y_{84}	Y_{85}	Y_{86}	Y_{87}	Y_{88}

① Weighted data 1
This comes from the following equation weighting in horizontal.
Weighting factors are the data from UW_E1 (address 0Bh) to UW_E8 (address 12h).

Weighted data 1 =
{(Y_{11} + Y_{12} + ··· + Y_{18})/8 x UW_E1 (address 0Bh)
+ (Y_{21} + Y_{22} + ··· + Y_{28})/8 x UW_E2 (address 0Ch)
:
+ (Y_{81} + Y_{82} + ··· + Y_{88})/8 x UW_E8 (address 12h)}/256

The sum from UW_E1 to UW_E8 shall be 256.

② Weighted data 2
Weighting area can be set by the data of CWP_E (address 14h), CWA_E (address 15h).
Weighting position can be set by the data of CWP_E.
Weighting area size can be set by the data of CWA_E.
Weighted data come from averaged data in chosen area.

③ Top level : The highest luminance data in one image by averaging either 4 pixels or 8 pixels in horizontal.

④ Bottom level : The lowest luminance data in one image by averaging either 4 pixels or 8 pixels in horizontal.

Auto White Balance Control

If white balance control data are less than the data of AWB_IW_S and AWB_QW_S (address 40h), then AWB stops.
If white balance control data are less than the data of AWB_IW_L (address 3Eh) and AWB_QW_L (address 3Fh) AWB is made active so that white balance control data are less than the data of AWB_IW_S and AWB_QW_S.
When the data are greater than AWB_IW_L and AWB_QW_L, AWB will be active again.

White balance data come from the following equation using averaged I and Q data of 16 areas in one image.

I_{11}	I_{12}	I_{13}	I_{14}
I_{21}	I_{22}	I_{23}	I_{24}
I_{31}	I_{32}	I_{33}	I_{34}
I_{41}	I_{42}	I_{43}	I_{44}

Q_{11}	Q_{12}	Q_{13}	Q_{14}
Q_{21}	Q_{22}	Q_{23}	Q_{24}
Q_{31}	Q_{32}	Q_{33}	Q_{34}
Q_{41}	Q_{42}	Q_{43}	Q_{44}

White balance data =
{Weighted data 3 ① x (64 – CW_IQ (address 33h))
+ weighted data 4 ② x CW_IQ}/64

① Weighted data 3
I (or Q) data come from the following equation.

Weighted data 3 =
$\{(I_{11} + I_{12} + I_{13} + I_{14})/4 + (I_{21} + I_{22} + I_{23} + I_{24})/4 + + (I_{31} + I_{32} + I_{33} + I_{34})/4 + (I_{41} + I_{42} + I_{43} + I_{44})/4\}/4$

② Weighted data 4
Weighting area can be chosen by CWPA_IQ (address 34h).
Weighted data come from averaged data in chosen area.

③ White balance area setting
The sum of I and Q can be regulated by the luminance level and the color level.
Setting available luminance level range :
High level :
AWB_HCL (address 2Eh) + [{K_CL (address 31h) x H peak level + (256 – K_CL) x Exposure control data}/256 – REF_WBPK (address 30h)] x K_WBCL (address 32h)

Low level :
AWB_LCL (address 2Fh) + [{K_CL (address 31h) x H peak level + (256 – K_CL) x Exposure control data}/256 – REF_WBPK (address 30h)] x K_WBCL (address 32h)

Setting target zone :
AWB_IP_L (address 36h), AWB_IM_L (address 37h)
AWB_QP_L (address 38h), AWB_QM_L (address 39h)

If white balance data are less than the data of AWB_IW_S and AWB_QW_S (address 40h) the target zone of auto white balance changes to the zone by the data below.

Setting target zone :
AWB_IP_S (address 3Ah), AWB_IM_S (address 3Bh)
AWB_QP_S (address 3Ch), AWB_QM_S (address 3Dh)

Auto Color Matrix and Level Compensation

Color matrix compensation can be done by
R – Y = R – Y±(Data1 x B – Y)
B – Y = B – Y±(Data2 x R – Y)

Color level compensation can be done by
R – Y = R – Y x Data3
B – Y = B – Y x Data4

The above data come from the following equation along the variation of color temperature.

MODE1 : Present WBR factor < WBR1
MODE2 : WBR1 ≤ present WBR factor < WBR2
MODE3 : WBR2 ≤ present WBR factor < WBR3
MODE4 : WBR3 ≤ present WBR factor

MODE1 and MODE_MAT (address 25h) = 0
Data1 = REF_MAT_R1M (address 5Ch)
Data2 = REF_MAT_B1M (address 5Dh)
Data3 = REF_GA_R1M (address 48h)
Data4 = REF_GA_B1M (address 49h)

MODE1 and MODE_MAT = 1
Data1 = REF_MAT_R1M (address 5Ch) : B – Y < 0
REF_MAT_R1P (address 5Eh) : B – Y ≥ 0
Data2 = REF_MAT_B1M (address 5Dh) : R – Y < 0
REF_MAT_B1P (address 5Fh) : R – Y ≥ 0
Data3 = REF_GA_R1M (address 48h) : R – Y < 0
REF_GA_R1P (address 4Ah) : R – Y ≥ 0
Data4 = REF_GA_B1M (address 49h) : B – Y < 0
REF_GA_B1P (address 4Bh) : B – Y ≥ 0

MODE2 and MODE_MAT = 0

Data1 = REF_MAT_R1M + K_MAT_R1M (address 68h) x (WBR – WBR1)/32

Data2 = REF_MAT_B1M + K_MAT_B1M (address 69h) x (WBR – WBR1)/32

Data3 = REF_GA_R1M + K_GA_R1M (address 54h) x (WBR – WBR1)/32

Data4 = REF_GA_B1M + K_GA_B1M (address 55h) x (WBR – WBR1)/32

MODE2 and MODE_MAT = 1

Data1 = REF_MAT_R1M + K_MAT_R1M (address 68h) x (WBR – WBR1)/32 : B – Y < 0
REF_MAT_R1P + K_MAT_R1P (address 6Ah) x (WBR – WBR1)/32 : B – Y ≥ 0

Data2 = REF_MAT_B1M + K_MAT_B1M (address 69h) x (WBR – WBR1)/32 : R – Y < 0
REF_MAT_B1P + K_MAT_B1P (address 6Bh) x (WBR – WBR1)/32 : R – Y ≥ 0

Data3 = REF_GA_R1M + K_GA_R1M (address 54h) x (WBR – WBR1)/32 : R – Y < 0
REF_GA_R1P + K_GA_R1P (address 56h) x (WBR – WBR1)/32 : R – Y ≥ 0

Data4 = REF_GA_B1M + K_GA_B1M (address 55h) x (WBR – WBR1)/32 : B – Y < 0
REF_GA_B1P + K_GA_B1P (address 57h) x (WBR – WBR1)/32 : B – Y ≥ 0

MODE3 and MODE_MAT = 0

Data1 = REF_MAT_R2M (address 60h) + K_MAT_R2M (address 6Ch) x (WBR – WBR1)/32

Data2 = REF_MAT_B2M (address 61h) + K_MAT_B2M (address 6Dh) x (WBR – WBR1)/32

Data3 = REF_GA_R2M (address 4Ch) + K_GA_R2M (address 58h) x (WBR – WBR1)/32

Data4 = REF_GA_B2M (address 4Dh) + K_GA_B2M (address 59h) x (WBR – WBR1)/32

MODE3 and MODE_MAT = 1

Data1 = REF_MAT_R2M (address 60h) + K_MAT_R2M (address 6Ch) x (WBR – WBR1)/32 : B – Y < 0
REF_MAT_R2P (address 62h) + K_MAT_R2P (address 6Eh) x (WBR – WBR1)/32 : B – Y ≥ 0

Data2 = REF_MAT_B2M (address 61h) + K_MAT_B2M (address 6Dh) x (WBR – WBR1)/32 : R – Y < 0
REF_MAT_B2P (address 63h) + K_MAT_B2P (address 6Fh) x (WBR – WBR1)/32 : R – Y ≥ 0

Data3 = REF_GA_R2M (address 4Ch) + K_GA_R2M (address 58h) x (WBR – WBR1)/32 : R – Y < 0
REF_GA_R2P (address 4Eh) + K_GA_R2P (address 5Ah) x (WBR – WBR1)/32 : R – Y ≥ 0

Data4 = REF_GA_B2M (address 4Dh) + K_GA_B2M (address 59h) x (WBR – WBR1)/32 : B – Y < 0
REF_GA_B2P (address 4Fh) + K_GA_B2P (address 5Bh) x (WBR – WBR1)/32 : B – Y ≥ 0

MODE4 and MODE_MAT = 0

Data1 = REF_MAT_R3M (address 64h)

Data2 = REF_MAT_B3M (address 65h)

Data3 = REF_GA_R3M (address 50h)

Data4 = REF_GA_B3M (address 51h)

MODE4 and MODE_MAT = 1

Data1 = REF_MAT_R3M (address 64h) : B – Y < 0
REF_MAT_R3P (address 66h) : B – Y ≥ 0

Data2 = REF_MAT_B3M (address 65h) : R – Y < 0
REF_MAT_B3P (address 67h) : R – Y ≥ 0

Data3 = REF_GA_R3M (address 50h) : R – Y < 0
REF_GA_R3P (address 52h) : R – Y ≥ 0

Data4 = REF_GA_B3M (address 51h) : B – Y < 0
REF_GA_B3P (address 53h) : B – Y ≥ 0

Color Level Suppression Under Lower Illumination

Working PGA gain can control both R – Y level and B – Y level by the following equation.

R – Y (B – Y) level
= {32 – (working PGA gain – COL_S (address 71h)) x COL_H (address 72h)}/32

When (working PGA gain – COL_S (address 71h)) ≤ 0, ( ) = 0.

Aperture Level Suppression Under Lower Illumination

Working PGA gain can control both the horizontal aperture level and the vertical aperture level by the following equation.

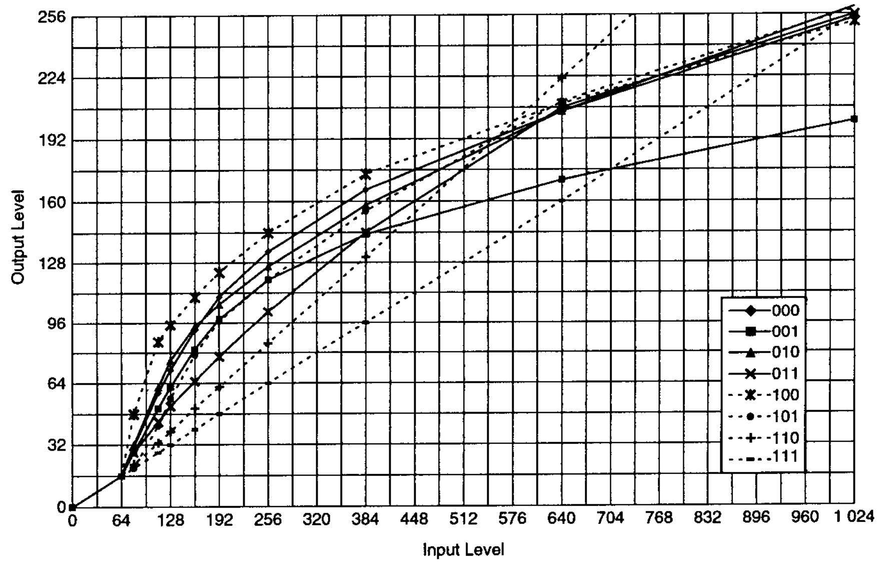
Horizontal aperture level
= APT_HGA (address 7Ch) x {32 – (working PGA gain – APT_S (address 80h)) x APT_H (address 81h)}/32
Vertical aperture level
= APT_VGA (address 7Eh) x {32 – (working PGA gain – APT_S (address 80h)) x APT_H (address 81h)}/32

When (working PGA gain – APT_S (address 80h)) ≤ 0 , ( ) = 0.

Gamma Characteristic Option

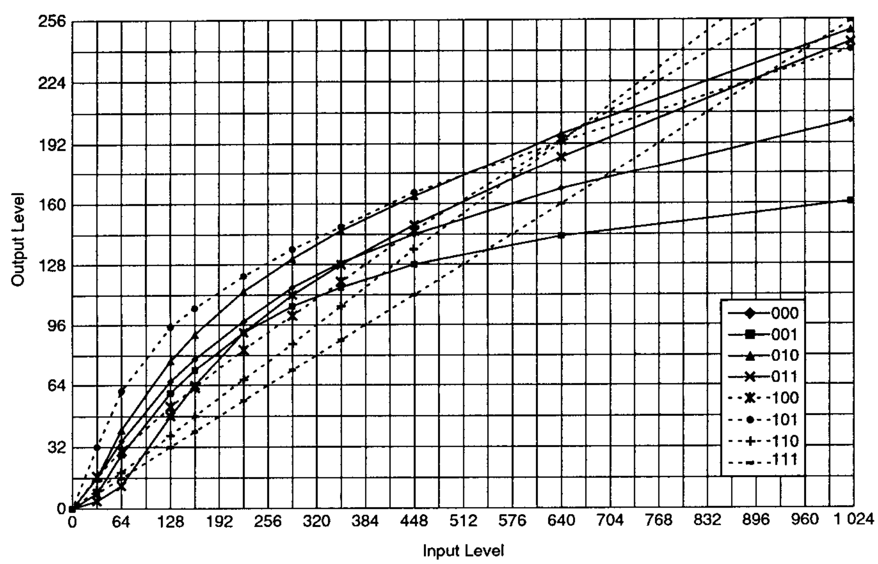
- Luminance signal gamma option

Y_GAM (address 7Bh) can choose one output of below 8 responses.



- Color signal gamma option

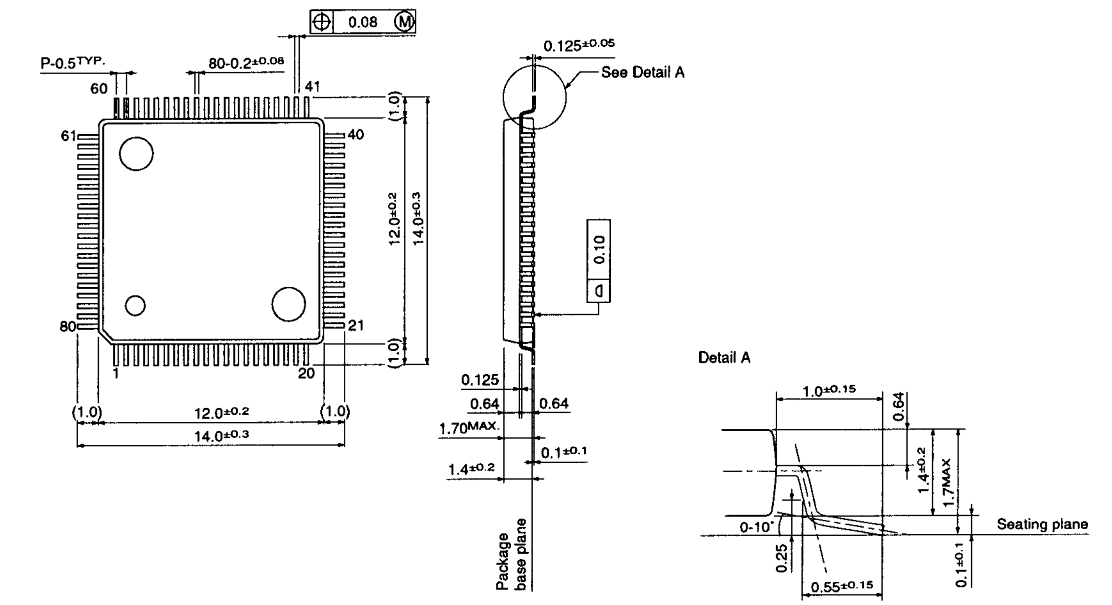
C_GAM (address 24h) can choose one output from 8 responses below.



PACKAGE OUTLINES

80 LQFP (P-LQFP080-1212)

(Unit : mm)



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