19-2717; Rev 0; 1/03

EVALUATION KIT AVAILABLE

Compact 155Mbps to 3.2Gbps Limiting Amplifier

MAX3748

General Description

The MAX3748 multirate limiting amplifier functions as a data quantizer for SONET, Fibre Channel, and Gigabit Ethernet optical receivers. The amplifier accepts a wide range of input voltages and provides constant-level current-mode logic (CML) output voltages with controlled edge speeds.

A received-signal-strength indicator (RSSI) is available when the MAX3748 is combined with the MAX3744 SFP transimpedance amplifier (TIA). A receiver consisting of the MAX3744* and the MAX3748 can provide up to 19dB RSSI dynamic range. Additional features include a programmable loss-of-signal (LOS) detect, an optional disable function (DISABLE), and an output signal polarity reversal (OUTPOL). Output disable can be used to implement squelch.

The combination of the MAX3748 and the MAX3744 allows for the implementation of all the small-form-factor SFF-8472 digital diagnostic specifications using a standard 4-pin TO-46 header. The MAX3748 is packaged in a 3mm × 3mm 16-pin QFN package with an exposed pad.

*Future product—contact factory for availability.

Applications

Gigabit Ethernet SFF/SFP Transceiver Modules

Fibre Channel SFF/SFP Transceiver Modules

Multirate OC-3 to OC-48-FEC SFF/SFP Transceiver Modules

Features

- **SFP Reference Design Available**
- **16-Pin QFN Package with 3mm × 3mm Footprint**
- **Single +3.3V Supply Voltage**
- **86ps Rise and Fall Time**
- **Loss of Signal with Programmable Threshold**
- **RSSI Interface (with MAX3744 TIA)**
- **Output Disable**
- **Polarity Select**
- **8.5ps$_{P-P}$ Deterministic Jitter (3.2Gbps)**

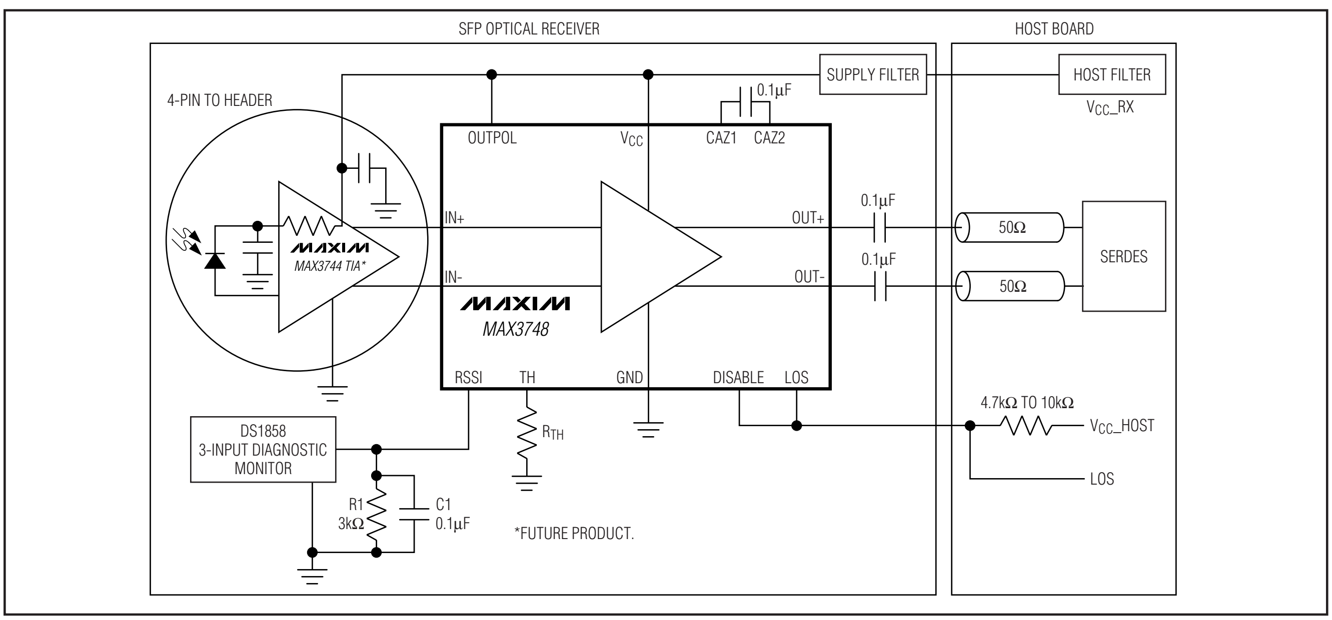
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PACKAGE CODE
MAX3748ETE	-40°C to +85°C	16 QFN-EP*	T1633-3

*EP = Exposed pad.

Functional Diagram and Pin Configuration appear at end of data sheet.
Typical Operating Circuits continued at end of data sheet.

Typical Operating Circuits



Compact 155Mbps to 3.2Gbps Limiting Amplifier

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC}) ....-0.5V to +6.0V
Voltage at IN+, IN- ....(V_{CC} - 2.4V) to (V_{CC} + 0.5V)
Voltage at DISABLE, OUTPOL, RSSI,
CAZ1, CAZ2, LOS, TH............................-0.5V to (V_{CC} + 0.5V)
Current into LOS ....-1mA to +9mA
Differential Input Voltage (IN+ - IN-) 2.5V
Continuous Current at CML Outputs
(OUT+, OUT-) ....-25mA to +25mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin QFN (derate 17.7mW above +70°C) 1.4W
Operating Junction Temperature Range (T_J)....-55°C to +150°C
Storage Ambient Temperature Range (T_S)........-55°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.97V to 3.63V, ambient temperature = -40°C to +85°C, CML output load is 50Ω to V_{CC}, C_{AZ} = 0.1µF, typical values are at +25°C, V_{CC} = 3.3V, unless otherwise specified. The data input transition time is controlled by a 4th-order Bessel filter with f_{-3dB} = 0.75 × 2.667GHz for all data rates of 2.667Gbps and below, and with f_{-3dB} = 0.75 × 3.2GHz for a data rate of 3.2Gbps.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Single-Ended Input Resistance		Single ended to V_{CC}	42	50	58	Ω
Input Return Loss		Differential, f < 3GHz, DUT is powered on		13		dB
Input Sensitivity	V_{IN-MIN}	(Note 1)			5	mV_{P-P}
Input Overload	V_{IN-MAX}	(Note 1)	1200			mV_{P-P}
Single-Ended Output Resistance		Single ended to V_{CC}	42	50	58	Ω
Output Return Loss		Differential, f < 3GHz, DUT is powered on		10		dB
Differential Output Voltage			600	780	1200	mV_{P-P}
Differential Output Signal when Disabled		Outputs AC-coupled, V_{IN-MAX} applied to input (Note 2)			10	mV_{P-P}
Deterministic Jitter (Notes 2, 3)	DJ	K28.5 pattern at 3.2Gbps		8.5	25	ps_{P-P}
		2^{23}- 1 PRBS equivalent pattern at 2.7Gbps (Note 4)		9.3	30	
		K28.5 pattern at 2.1Gbps		7.8	25	
		2^{23}- 1 PRBS equivalent pattern at 155Mbps		25	50	
Random Jitter (Note 5)		Input = $5mV_{P-P}$		6.5		ps_{RMS}
		Input = $10mV_{P-P}$		3		
Data Output Transition Time		20% to 80% (Note 2)		86	115	ps
Input-Referred Noise				185		$µV_{RMS}$
Low-Frequency Cutoff		C_{AZ} = open		70		kHz
		C_{AZ} = 0.1µF		0.8		
Power-Supply Current	I_{CC}	(Note 6)		32	49	mA
		LOS disabled			37	
Power-Supply Noise Rejection	PSNR	f < 2MHz		26		dB
LOSS OF SIGNAL at 2.5Gbps (Notes 2, 7)						
LOS Hysteresis		10log ($V_{DEASSERT}/V_{ASSERT}$)	1.25	2.2		dB
LOS Assert/Deassert Time		(Note 8)	2		100	µs
Low LOS Assert Level		R_{TH} = 20kΩ	2.8	4.1		mV_{P-P}
Low LOS Deassert Level		R_{TH} = 20kΩ		6.7	11.6	mV_{P-P}
Medium LOS Assert Level		R_{TH} = 280Ω	10.3	15.2		mV_{P-P}

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.97V to 3.63V, ambient temperature = -40°C to +85°C, CML output load is 50Ω to V_{CC}, C_{AZ} = 0.1µF, typical values are at +25°C, V_{CC} = 3.3V, unless otherwise specified. The data input transition time is controlled by a 4th-order Bessel filter with f_{-3dB} = 0.75 × 2.667GHz for all data rates of 2.667Gbps and below, and with f_{-3dB} = 0.75 × 3.2GHz for data rate of 3.2Gbps.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Medium LOS Deassert Level		R_{TH} = 280Ω			25	38.6	mV_{P-P}
High LOS Assert Level		R_{TH} = 80Ω		22.8	38.3		mV_{P-P}
High LOS Deassert Level		R_{TH} = 80Ω			65.2	99.3	mV_{P-P}
LOSS OF SIGNAL at 155Mbps (Note 7)							
LOS Hysteresis		10log ($V_{DEASSERT}/V_{ASSERT}$)			2.1		dB
LOS Assert/Deassert Time		(Note 8)			20		µs
Low LOS Assert Level		R_{TH} = 20kΩ			3.5		mV_{P-P}
Low LOS Deassert Level		R_{TH} = 20kΩ			5.6		mV_{P-P}
Medium LOS Assert Level		R_{TH} = 280Ω			13.3		mV_{P-P}
Medium LOS Deassert Level		R_{TH} = 280Ω			21.2		mV_{P-P}
High LOS Assert Level		R_{TH} = 80Ω			33.3		mV_{P-P}
High LOS Deassert Level		R_{TH} = 80Ω			55.5		mV_{P-P}
RSSI							
RSSI Current Gain (Note 9)	A_{RSSI}	$A_{RSSI} = I_{RSSI}/I_{CM\_RSSI}$			0.03		
Input-Referred RSSI Current Stability		I_{RSSI}/A_{RSSI} (Note 10)	I_{CM_INPUT} < 6.6mA	-31		+33	µA
			I_{CM_INPUT} > 6.6mA	-73		+90	
TTL/CMOS I/O							
LOS Output High Voltage	V_{OH}	R_{LOS} = 4.7kΩ to10kΩ to V_{CC_host} (3V)		2.4			V
LOS Output Low Voltage	V_{OL}	R_{LOS} = 4.7kΩ to10kΩ to V_{CC_host} (3.6V)				0.4	V
LOS Output Current		R_{LOS} = 4.7kΩ to10kΩ to V_{CC_host} (3.3V); IC is powered down				40	µA
DISABLE Input High	V_{IH}			2.0			V
DISABLE Input Low	V_{IL}					0.8	V
DISABLE Input Current		R_{LOS} = 4.7kΩ to 10kΩ to V_{CC_host}				10	µA

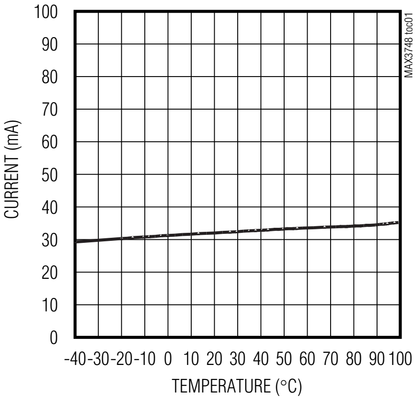
Note 1: Between sensitivity and overload, all AC specifications are met.
Note 2: Guaranteed by design and characterization.
Note 3: The deterministic jitter caused by this filter is not included in the DJ generation specifications (input).
Note 4: 2^{23} - 1 PRBS pattern was substituted by K28.5 pattern to determine the high-speed portion of the deterministic jitter. The low-speed portion of the DJ (baseline wander) was obtained by measuring the eye width difference between outputs generated using K28.5 and 2^{23} - 1 PRBS patterns.
Note 5: Random jitter was measured without using a filter at the input.
Note 6: The supply current measurement excludes the CML output currents by connecting the CML outputs to a separate V_{CC} (see Figure 1).
Note 7: Unless otherwise specified, the pattern for all LOS detect specifications is 2^{23} - 1 PRBS.
Note 8: The signal at the input is switched between two amplitudes, Signal_ON and Signal_OFF, as shown in Figure 2.
Note 9: I_{CM_INPUT} is the input common mode. I_{RSSI} is the current at the RSSI output.
Note 10: Stability is defined as variation over temperature and power supply with respect to the typical gain of the part.

Compact 155Mbps to 3.2Gbps Limiting Amplifier

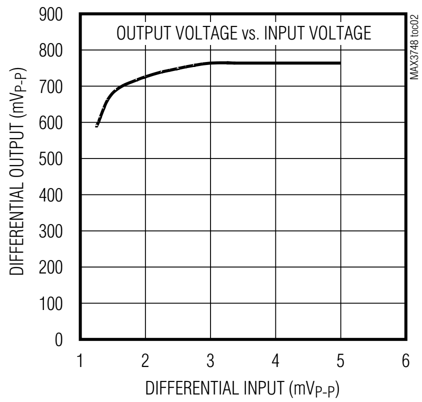
Typical Operating Characteristics

(T_A = +25°C and V_{CC} = +3.3V, unless otherwise specified.)

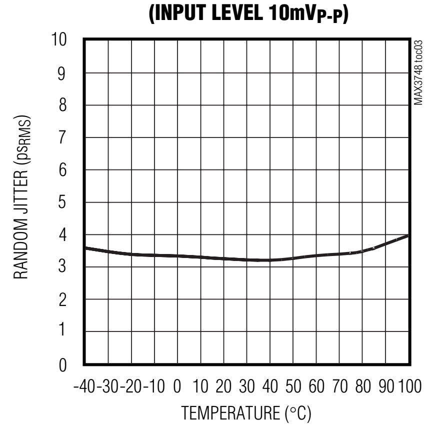
SUPPLY CURRENT vs. TEMPERATURE



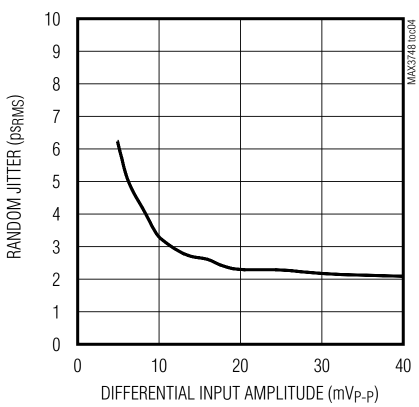
TRANSFER FUNCTION



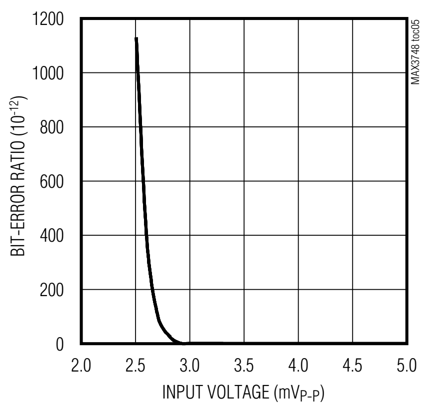
RANDOM JITTER vs. TEMPERATURE (INPUT LEVEL 10mVP-P)



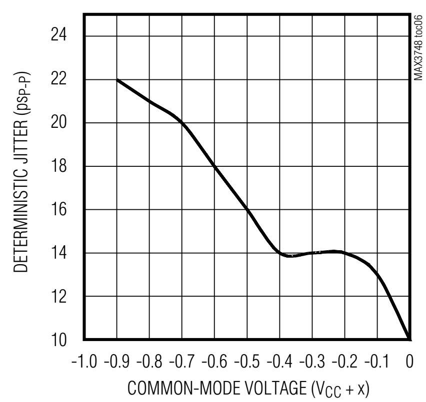
RANDOM JITTER vs. INPUT AMPLITUDE



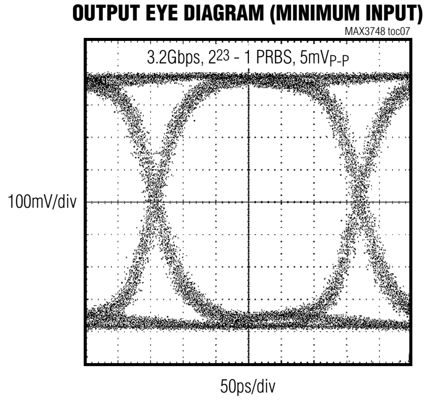
BIT-ERROR RATIO vs. INPUT VOLTAGE



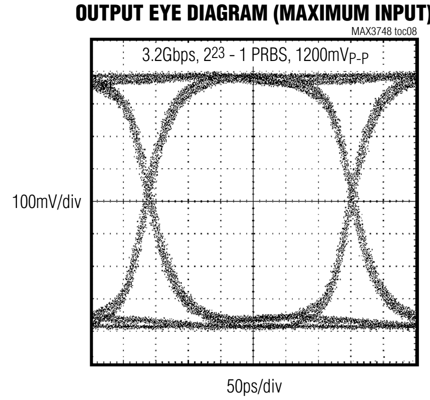
DETERMINISTIC JITTER vs. INPUT COMMON-MODE VOLTAGE (V_{CC} TO V_{CC} - 0.8V)



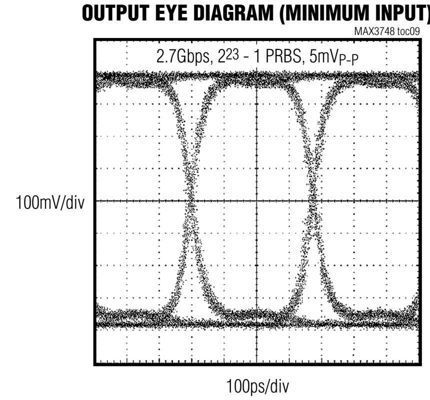
OUTPUT EYE DIAGRAM (MINIMUM INPUT)



OUTPUT EYE DIAGRAM (MAXIMUM INPUT)



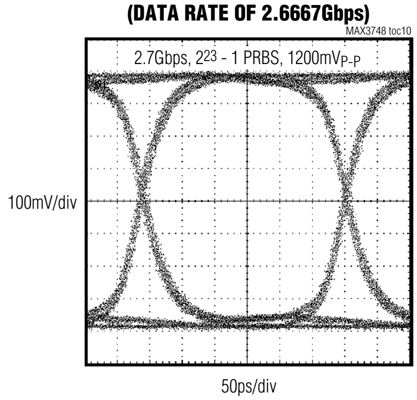
OUTPUT EYE DIAGRAM (MINIMUM INPUT)



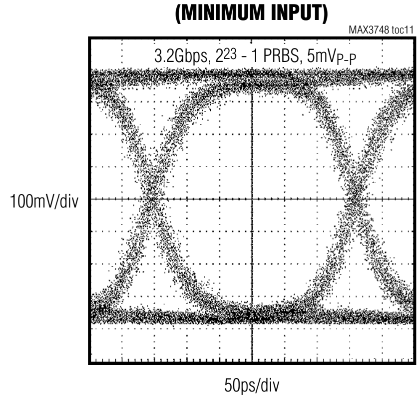
Typical Operating Characteristics (continued)

(T_A = +25°C and V_{CC} = +3.3V, unless otherwise specified.)

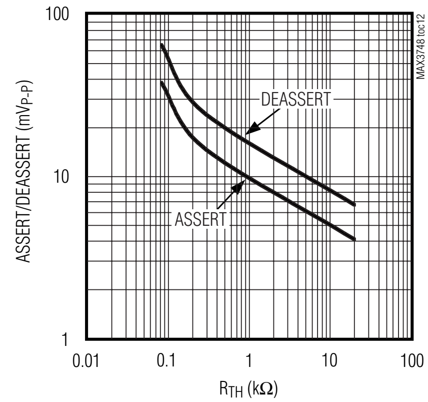
OUTPUT EYE DIAGRAM WITH MAXIMUM INPUT (DATA RATE OF 2.6667Gbps)



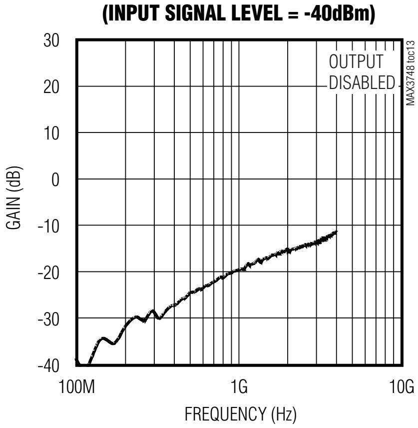
OUTPUT EYE DIAGRAM AT +100°C (MINIMUM INPUT)



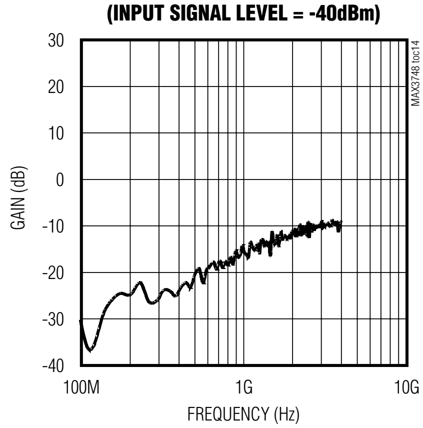
ASSERT/DEASSERT LEVELS vs. R_{TH}



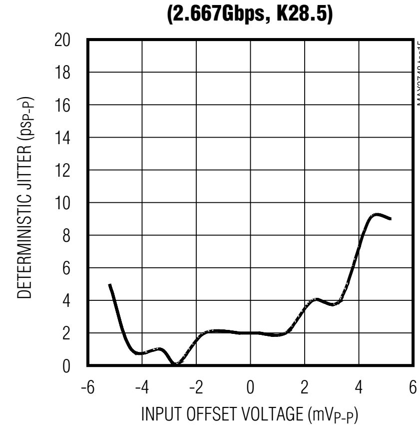
INPUT RETURN GAIN vs. FREQUENCY (SDD11) (INPUT SIGNAL LEVEL = -40dBm)



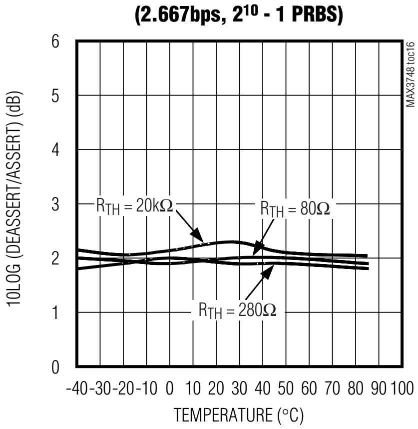
OUTPUT RETURN GAIN vs. FREQUENCY (SDD22) (INPUT SIGNAL LEVEL = -40dBm)



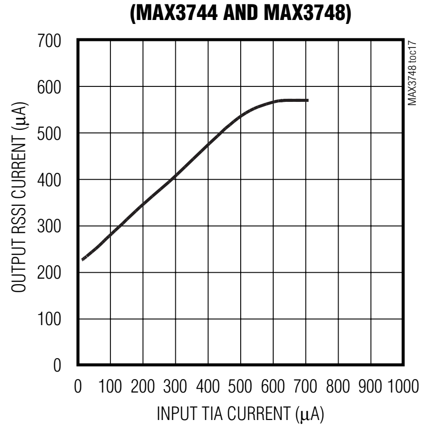
DETERMINISTIC JITTER vs. INPUT OFFSET VOLTAGE (2.667Gbps, K28.5)



LOS HYSTERESIS vs. TEMPERATURE (2.667bps, 2^{10} - 1 PRBS)



RSSI CURRENT GAIN vs. INPUT TIA CURRENT (MAX3744 AND MAX3748)



Compact 155Mbps to 3.2Gbps Limiting Amplifier

Pin Description

PIN	NAME	FUNCTION
1, 4, 12	V_{CC}	Supply Voltage
2	IN+	Noninverted Input Signal, CML
3	IN-	Inverted Input Signal, CML
5	TH	Loss-of-Signal Threshold Pin. Resistor to ground (R_{TH}) sets the LOS threshold. Connecting this pin to V_{CC} disables the LOS circuitry and reduces power consumption.
6	DISABLE	Disable Input, CMOS/TTL. The data outputs are held static when this pin is asserted high. The LOS function remains active when the outputs are disabled, CMOS. This pin does not include ESD protection. If routed through the DS1858/DS1859 controller IC, no additional ESD protection is required. Protection can be provided with external diodes.
7	LOS	Noninverted Loss-of-Signal Output. LOS is asserted high when the signal drops below the assert threshold set by the TH input. The output is open collector (Figure 5). This pin does not include ESD protection. If routed through the DS1858/DS1859 controller IC, no additional ESD protection is required. Protection can be provided with external diodes.
8, 16	GND	Supply Ground
9	OUTPOL	Output Polarity Control Input. Connect to GND for an inversion of polarity through the limiting amplifier and connect to V_{CC} for normal operation.
10	OUT-	Inverted Data Output, CML
11	OUT+	Noninverted Data Output, CML
13	RSSI	Received-Signal-Strength Indicator. This current output can be used to obtain a ground-referenced voltage proportional to photodiode current with the MAX3744 by connecting an external resistor between this pin and GND.
14	CAZ2	Offset Correction Loop Capacitor Connection. A capacitor connected between this pin and CAZ1 extends the time constant of the offset correction loop. Typical value of C_{AZ} is 0.1µF. The offset correction is disabled when the CAZ1 and CAZ2 pins are shorted together.
15	CAZ1	Offset Correction Loop Capacitor Connection. A capacitor connected between this pin and CAZ2 extends the time constant of the offset correction loop. Typical value of C_{AZ} is 0.1µF. The offset correction is disabled when the CAZ1 and CAZ2 pins are shorted together.
EP	Exposed paddle	Connect the exposed paddle to board ground for optimal electrical and thermal performance.

Detailed Description

The limiting amplifier consists of an input buffer, a multistage amplifier, offset correction circuitry, an output buffer, power-detection circuitry, and signal-detect circuitry (see *Functional Diagram*).

Input Buffer

The input buffer is shown in Figure 3. It provides 50Ω termination for each input signal IN+ and IN-. The MAX3748 can be DC- or AC-coupled to a TIA (TIA output offset degrades receiver performance if DC-coupled). The CML input buffer is optimized for the MAX3744 TIA.

Gain Stage

The high-bandwidth gain stage provides approximately 53dB of gain.

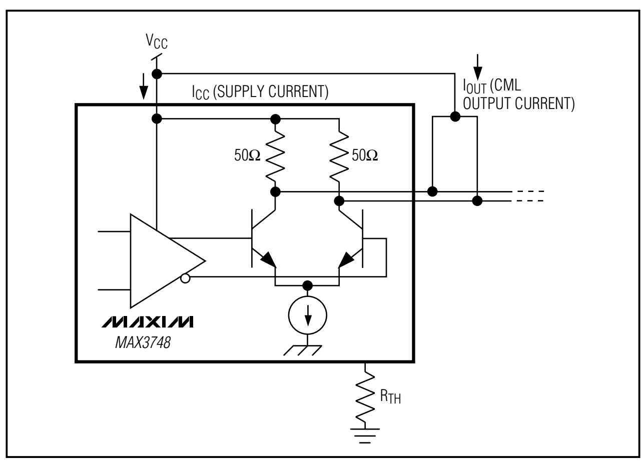


Figure 1. Power-Supply Current Measurement

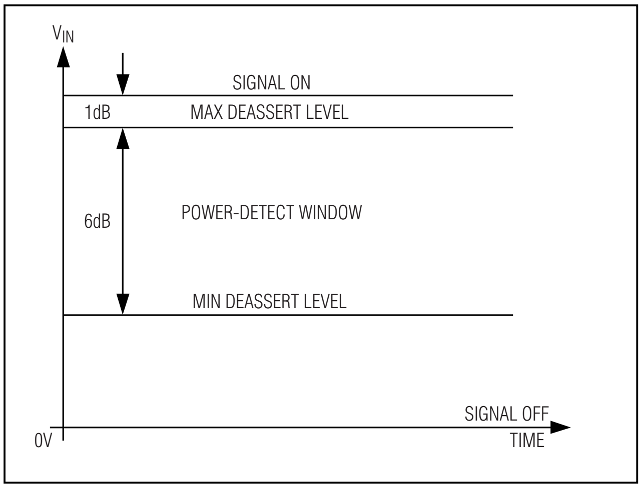


Figure 2. LOS Deassert Threshold Set 1dB Below the Minimum by Receiver Sensitivity (for Selected R_{TH})

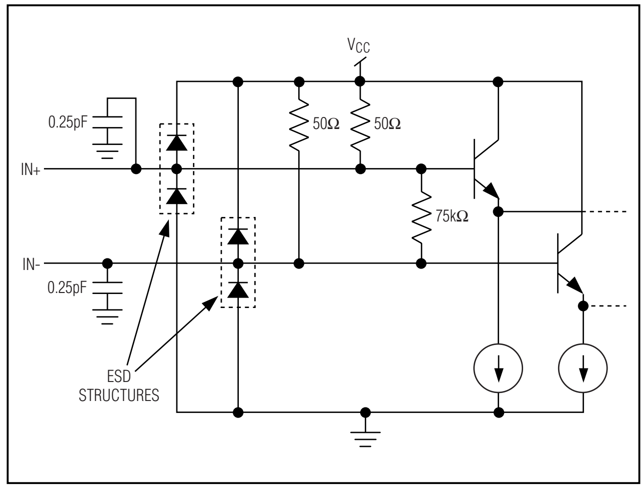


Figure 3. CML Input Buffer

Offset Correction Loop

The MAX3748 is susceptible to DC offsets in the signal path because it has high gain. In communication systems using NRZ data with a 50% duty cycle, pulse-width distortion present in the signal or generated in the transimpedance amplifier appears as an input offset and is reduced by the offset correction loop. For Gigabit Ethernet and Fibre-Channel applications, no capacitor is required. For SONET applications, C_{AZ} = 0.1µF is recommended. This capacitor determines the lower 3dB frequency of the data path.

CML Output Buffer

The MAX3748 limiting amplifier's CML output provides high tolerance to impedance mismatches and inductive connectors. The output current is approximately 18mA. The output is disabled by connecting the DISABLE pin to V_{CC}. If the LOS pin is connected to the DISABLE pin, the outputs OUT+ and OUT- are at a static voltage (squelch) whenever the input signal level drops below the LOS threshold. The output buffer can be AC- or DC-coupled to the load (Figure 4).

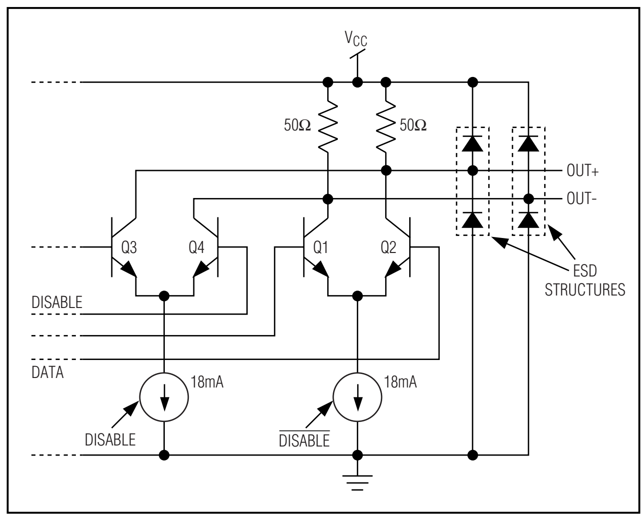


Figure 4. CML Output Buffer

Power-Detect and Loss-of-Signal Indicator

The MAX3748 is equipped with an LOS circuitry, which indicates when the input signal is below a programmable threshold, set by resistor R_{TH} at the TH pin (see *Typical Operating Characteristics* for appropriate resistor sizing). An averaging peak-power detector compares the input signal amplitude with this threshold and feeds the signal detect information to the LOS output, which is open collector. Two control voltages, V_{ASSERT} and $V_{DEASSERT}$, define the LOS assert and deassert levels. To prevent LOS chatter in the region of the programmed threshold, approximately 2dB of hysteresis is built into the LOS assert/deassert function. Once asserted, LOS is not deasserted until the input amplitude rises to the required level ($V_{DEASSERT}$) (Figure 5).

Compact 155Mbps to 3.2Gbps Limiting Amplifier

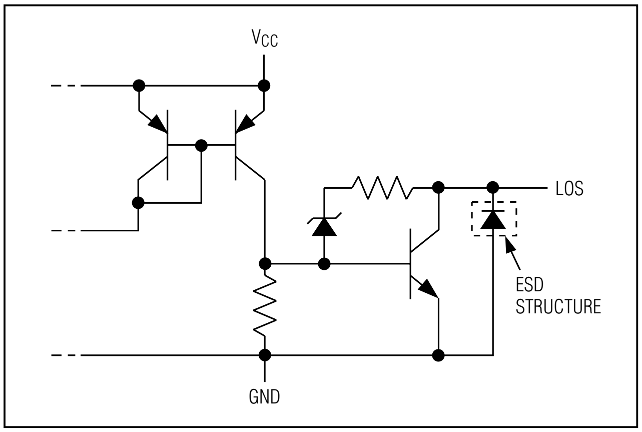


Figure 5. LOS Output Circuit

Design Procedure

Program the LOS Assert Threshold

External resistor R_{TH} programs the LOS threshold. See the Assert/Deassert Levels vs. R_{TH} graph in the *Typical Operating Characteristics* to select the appropriate resistor.

Select the Coupling Capacitor

When AC-coupling is desired, coupling capacitors C_{IN} and C_{OUT} should be selected to minimize the receiver's deterministic jitter. Jitter is decreased as the input low-frequency cutoff (f_{IN}) is decreased:

$$f_{IN} = 1 / [2\pi(50)(C_{IN})]$$

For ATM/SONET or other applications using scrambled NRZ data, select (C_{IN}, C_{OUT}) ≥ 0.1µF, which provides f_{IN} < 32kHz. For Fibre Channel, Gigabit Ethernet, or other applications using 8B/10B data coding, select (C_{IN}, C_{OUT}) ≥ 0.01µF, which provides f_{IN} < 320kHz. Refer to Application Note HFAN-1.1: *Choosing AC-Coupling Capacitors*.

Select the Offset-Correction Capacitor

The capacitor between CAZ1 and CAZ2 determines the time constant of the signal path DC offset cancellation loop. To maintain stability, it is important to keep a one-decade separation between f_{IN} and the low-frequency cutoff (f_{OC}) associated with the DC offset cancellation circuit. For ATM/SONET or other applications using scrambled NRZ data, f_{IN} < 32kHz, so f_{OCMAX} < 3.2kHz. Therefore, C_{AZ} = 0.1µF (f_{OC} = 2kHz). For Fibre Channel or Gigabit Ethernet applications, leave pins CAZ1 and CAZ2 open.

RSSI Implementation

The SFF-8472 Digital Diagnostic specification requires monitoring of input receive power. The MAX3748 and MAX3744 receiver chipset allows for the monitoring of the average receive power by measuring the average DC current of the photodiode.

The MAX3744 preamp measures the average photodiode current and provides the information to the output common mode. The MAX3748 RSSI detect block senses the common-mode DC level of input signals IN+ and IN- and provides a ground-referenced output signal (RSSI) proportional to the photodiode current. The advantage of this implementation is that it allows the TIA to be packaged in a low-cost conventional 4-pin TO-46 header.

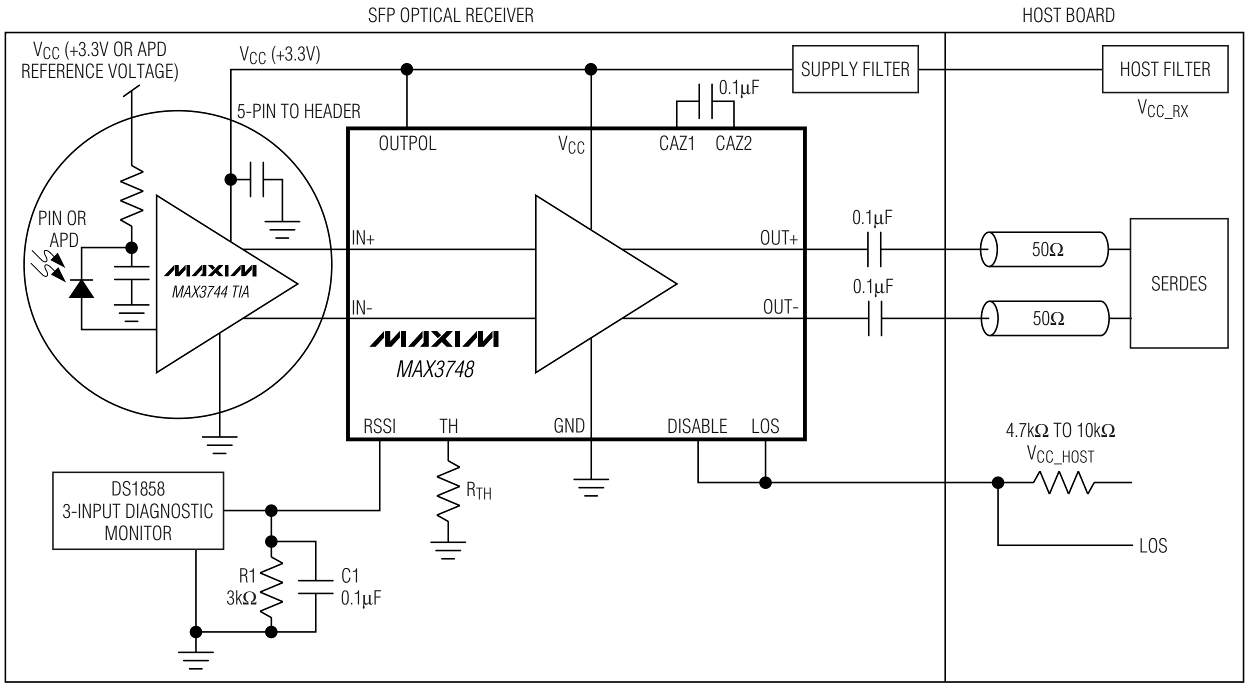
The MAX3748 RSSI output is connected to an analog input channel of the DS1858/DS1859 SFP controller to convert the analog information into a 16-bit word. The DS1858/DS1859 provide the receive-power information to the host board of the optical receiver through a 2-wire interface. The DS1859 allows for internal calibration of the receive-power monitor.

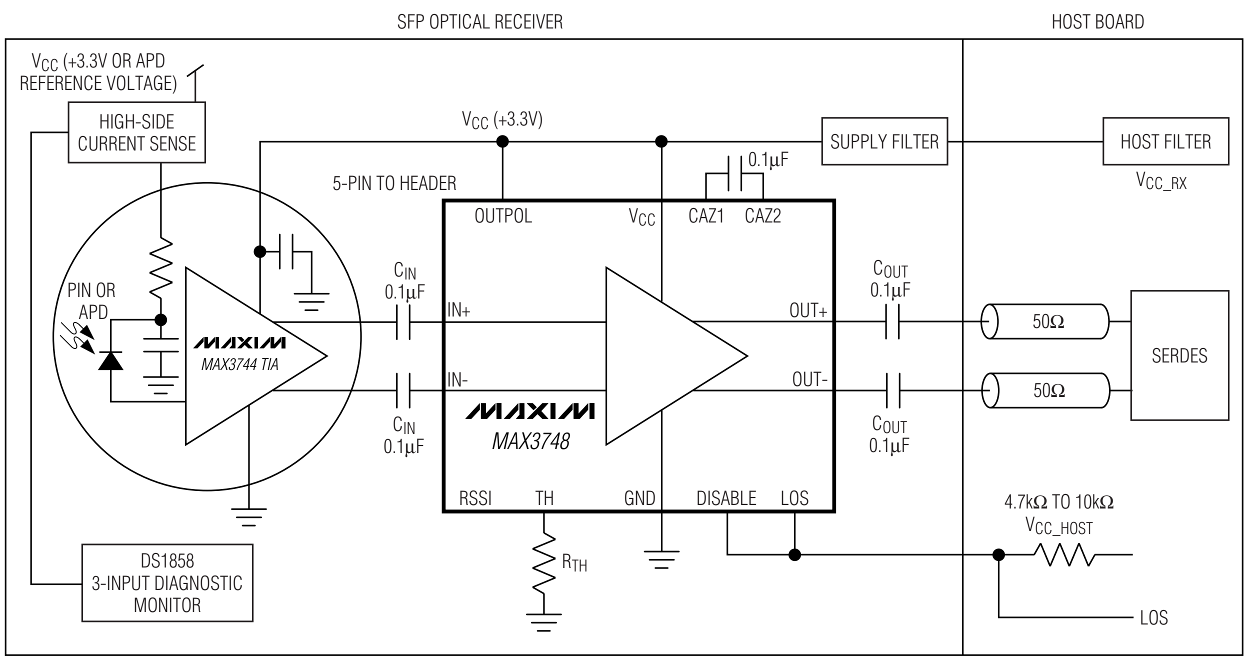
The MAX3744 and the MAX3748 have been optimized to achieve RSSI stability of 2.5dB within the range of 6µA to 500µA of average input photodiode current. To achieve the best accuracy, Maxim recommends receive power calibration at the low end (6µA) and the high end (500µA) of the required range; see the RSSI Current Gain graph in the *Typical Operating Characteristics*.

Connecting to the DS1858/DS1859

For best use of the RSSI monitor, capacitor C1 and resistor R1 shown in the first *Typical Application Circuit* need to be placed as close as possible to the Dallas diagnostic monitor with the ground of C1 and R1 the same as the DS1858/DS1859 ground. Capacitor C1 suppresses system noise on the RSSI signal. R1 = 3kΩ and C1 = 0.1µF is recommended.

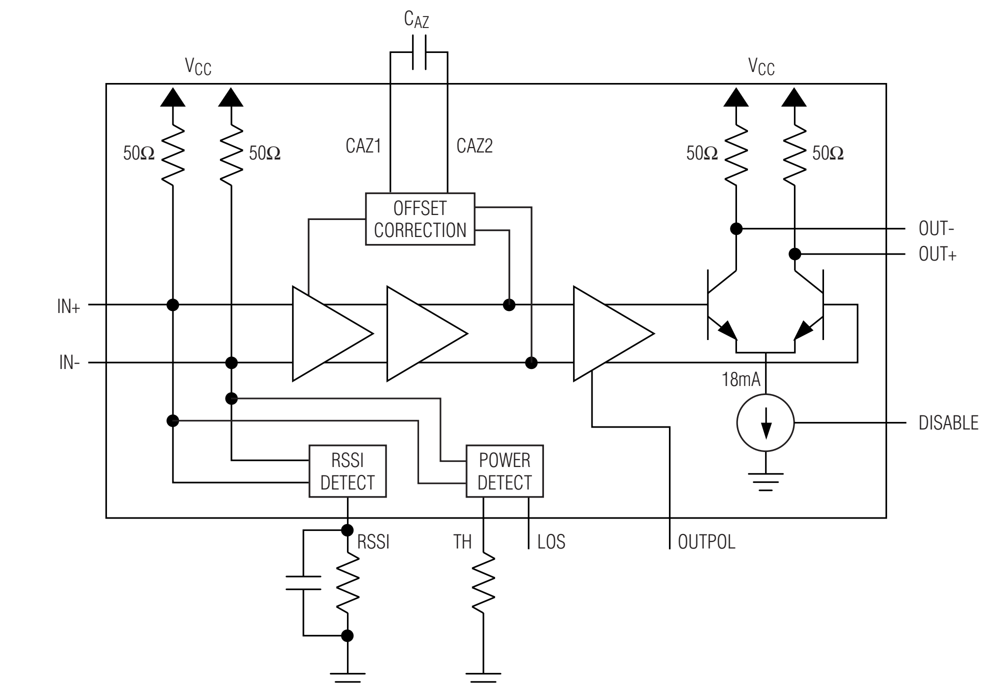
Typical Operating Circuits (continued)



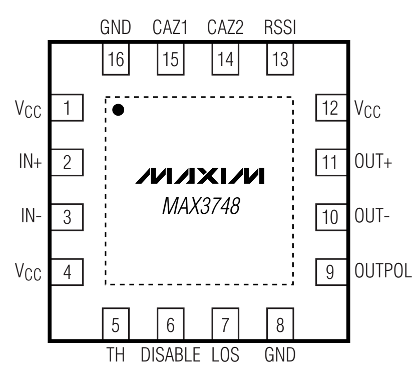


Compact 155Mbps to 3.2Gbps Limiting Amplifier

Functional Diagram



Pin Configuration



3mm x 3mm QFN

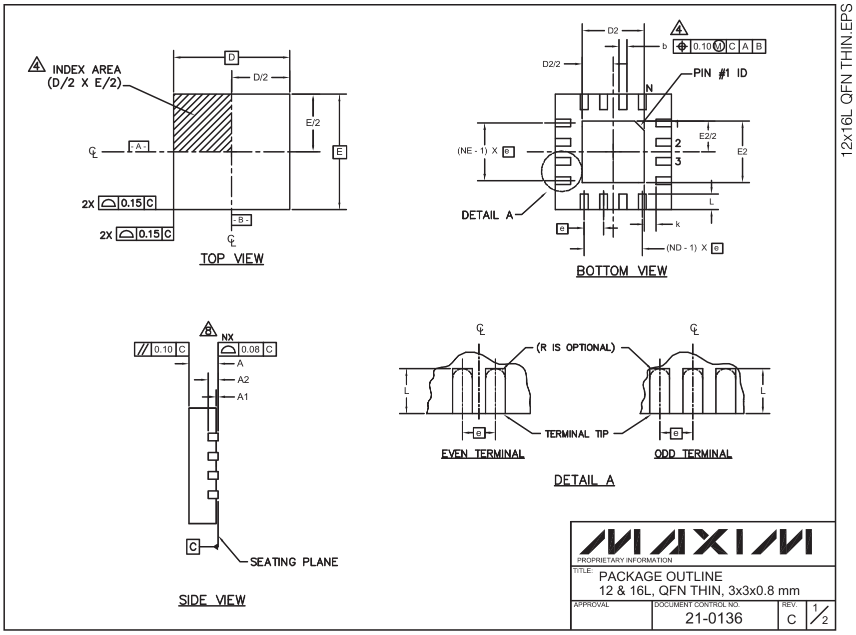
Chip Information

TRANSISTOR COUNT: 1468

PROCESS: SiGe Bipolar

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



PKG	12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80
b	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10
e	0.50 BSC.			0.50 BSC.		
L	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16		
ND	3			4		
NE	3			4		
A1	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	-

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.

PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
12 & 16L, QFN THIN, 3x3x0.8 mm
APPROVAL | DOCUMENT CONTROL NO. 21-0136 | REV. C | 2/2