19-4767; Rev 2; 1/99

EVALUATION KIT MANUAL FOLLOWS DATA SHEET

+3.3V, 2.488Gbps, SDH/SONET 1:16 Deserializer with LVDS Outputs

General Description

The MAX3885 deserializer is ideal for converting 2.488Gbps serial data to 16-bit wide, 155Mbps parallel data in SDH/SONET applications. Operating from a single +3.3V supply, this device accepts PECL serial clock and data inputs, and delivers low-voltage differential-signal (LVDS) clock and data outputs for interfacing with high-speed digital circuitry. It also provides an LVDS synchronization input that enables data realignment and reframing. The MAX3885 is available in the extended temperature range (-40°C to +85°C) in a 64-pin TQFP package.

Features

- **Single +3.3V Supply**
- **2.488Gbps Serial to 155Mbps Parallel Conversion**
- **660mW Operating Power**
- **LVDS Data Outputs and Synchronization Inputs**
- **Self-Biasing PECL Inputs Ease AC Coupling**
- **Synchronization Inputs for Data Realignment and Reframing**

Applications

2.488Gbps SDH/SONET Transmission Systems

Add/Drop Multiplexers

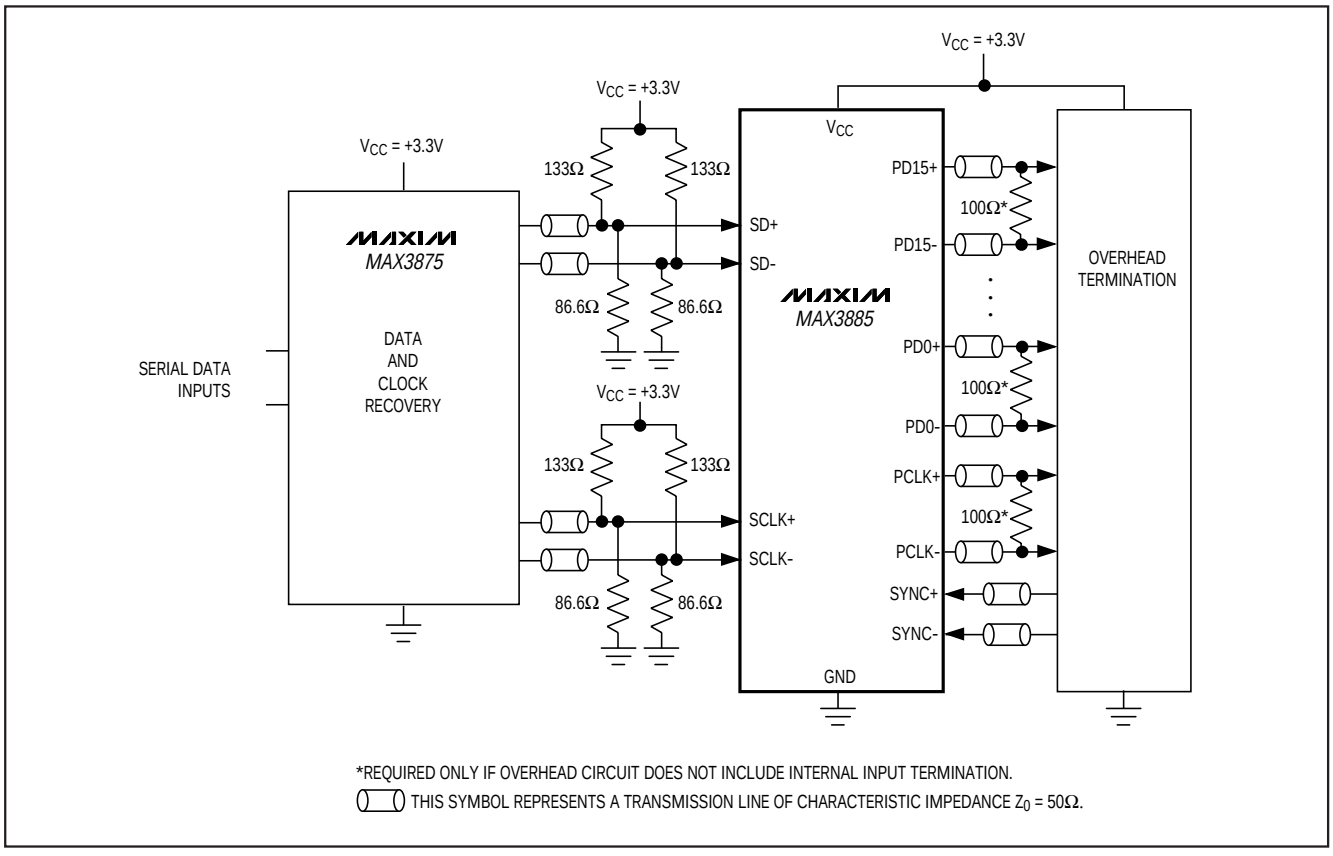
Digital Cross Connects

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3885ECB	-40°C to +85°C	64 TQFP

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



*REQUIRED ONLY IF OVERHEAD CIRCUIT DOES NOT INCLUDE INTERNAL INPUT TERMINATION.

THIS SYMBOL REPRESENTS A TRANSMISSION LINE OF CHARACTERISTIC IMPEDANCE Z_0 = 50Ω.

+3.3V, 2.488Gbps, SDH/SONET 1:16 Deserializer with LVDS Outputs

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V_{CC}).....-0.5V to +7.0V
Input Voltage Level (all inputs).....-0.5V to (V_{CC} + 0.5V)
Output Current LVDS outputs 10mA
Continuous Power Dissipation (T_A = +85°C)
TQFP (derate 24mW/°C above +85°C).....1000mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-60°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential loads = 100Ω ±1%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}			200	280	mA
PECL INPUTS (SD+/-, SCLK+/-)						
Input High Voltage	V_{IH}		V_{CC} - 1.16		V_{CC} - 0.88	V
Input Low Voltage	V_{IL}		V_{CC} - 1.81		V_{CC} - 1.48	V
Input High Current	I_{IH}	$V_{IN} = V_{IH(MAX)}$	-900		900	µA
Input Low Current	I_{IL}	$V_{IN} = V_{IL(MIN)}$	-900		900	µA
LVDS INPUTS AND OUTPUTS (SYNC+/-, PCLK+/-, PD_+/-)						
Input Voltage Range	V_I	Differential input voltage = 100mV	0		2.4	V
Differential Input Threshold	V_{IDTH}	Common-mode voltage = 50mV	-100		100	mV
Threshold Hysteresis	V_{HYST}			78		mV
Differential Input Resistance	R_{IN}		85	100	115	Ω
Output High Voltage	V_{OH}				1.475	V
Output Low Voltage	V_{OL}		0.925			V
Differential Output Voltage	$\|V_{OD}\|$	Figure 1	250		400	mV
Change in Magnitude of Differential Output Voltage for Complementary States	$\Delta\|V_{OD}\|$				±25	mV
Output Offset Voltage	V_{OS}		1.125		1.275	V
Change in Magnitude of Output Offset Voltage for Complementary States	ΔV_{OS}				±25	mV
Single-Ended Output Resistance	R_O		40	95	140	Ω
Change in Magnitude of Single-Ended Output Resistance for Complementary Outputs	ΔR_O			±2.5	±10	%

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential loads = 100Ω ±1%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Note 1, Figure 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Serial Clock Frequency	f_{SCLK}		2.488			GHz
Serial Data Setup Time	t_{SU}		100			ps
Serial Data Hold Time	t_H		100			ps
Parallel Clock-to-Data Output Delay	t_{CLK-Q}		200	450	900	ps

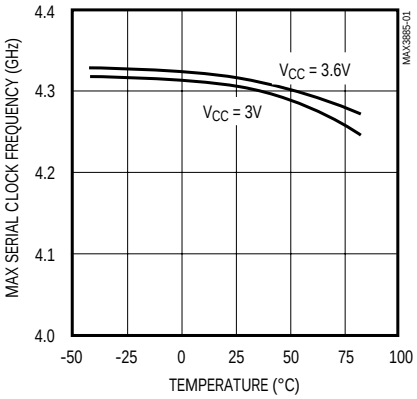
Note 1: AC Characteristics guaranteed by design and characterization.

+3.3V, 2.488Gbps, SDH/SONET 1:16 Deserializer with LVDS Outputs

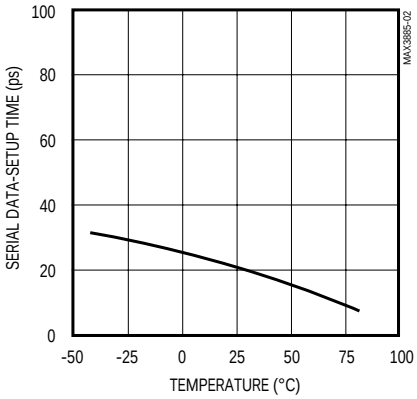
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

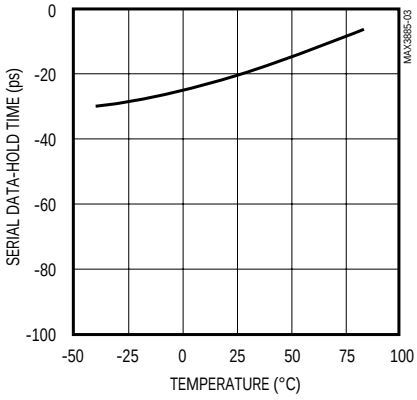
MAXIMUM SERIAL CLOCK FREQUENCY vs. TEMPERATURE



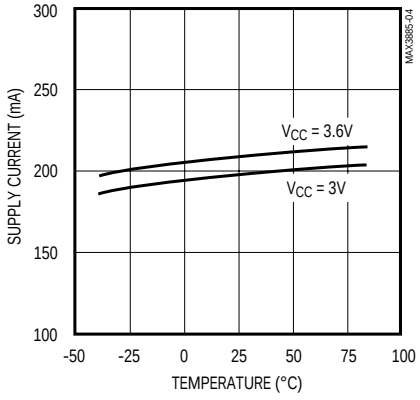
SERIAL DATA-SETUP TIME vs. TEMPERATURE



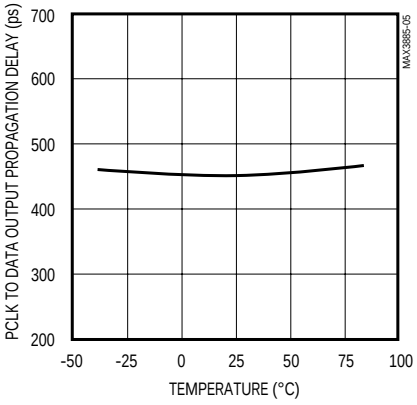
SERIAL DATA-HOLD TIME vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE



PARALLEL CLOCK TO DATA OUTPUT PROPAGATION DELAY vs. TEMPERATURE



+3.3V, 2.488Gbps, SDH/SONET 1:16 Deserializer with LVDS Outputs

Pin Description

PIN	NAME	FUNCTION
1, 2, 8, 16, 17, 24, 32, 33, 41, 48, 49, 57, 64	GND	Ground
3, 5, 7, 9, 11, 13, 25, 34, 42, 47, 56	V_{CC}	+3.3V Supply Voltage
4	SD+	Serial Data Noninverting PECL Input. Data is clocked on the SCLK signal's positive transition.
6	SD-	Serial Data Inverting PECL Input. Data is clocked on the SCLK signal's positive transition.
10	SCLK+	Serial Clock Noninverting PECL Input
12	SCLK-	Serial Clock Inverting PECL Input
14	SYNC-	Synchronizing Pulse Inverting LVDS Input. Pulse the SYNC signal high for at least four SCLK periods to shift the data alignment by dropping one bit.
15	SYNC+	Synchronizing Pulse Noninverting LVDS Input. Pulse the SYNC signal high for at least four SCLK periods to shift the data alignment by dropping one bit.
18	PCLK-	Parallel Clock Inverting LVDS Output
19	PCLK+	Parallel Clock Noninverting LVDS Output
20, 22, 26, 28, 30, 35, 37, 39, 43, 45, 50, 52, 54, 58, 60, 62	PD0- to PD15-	Parallel Data Inverting LVDS Outputs. Data is updated on the negative transition of the PCLK signal.
21, 23, 27, 29, 31, 36, 38, 40, 44, 46, 51, 53, 55, 59, 61, 63	PD0+ to PD15+	Parallel Data Noninverting LVDS Outputs. Data is updated on the negative transition of the PCLK signal.

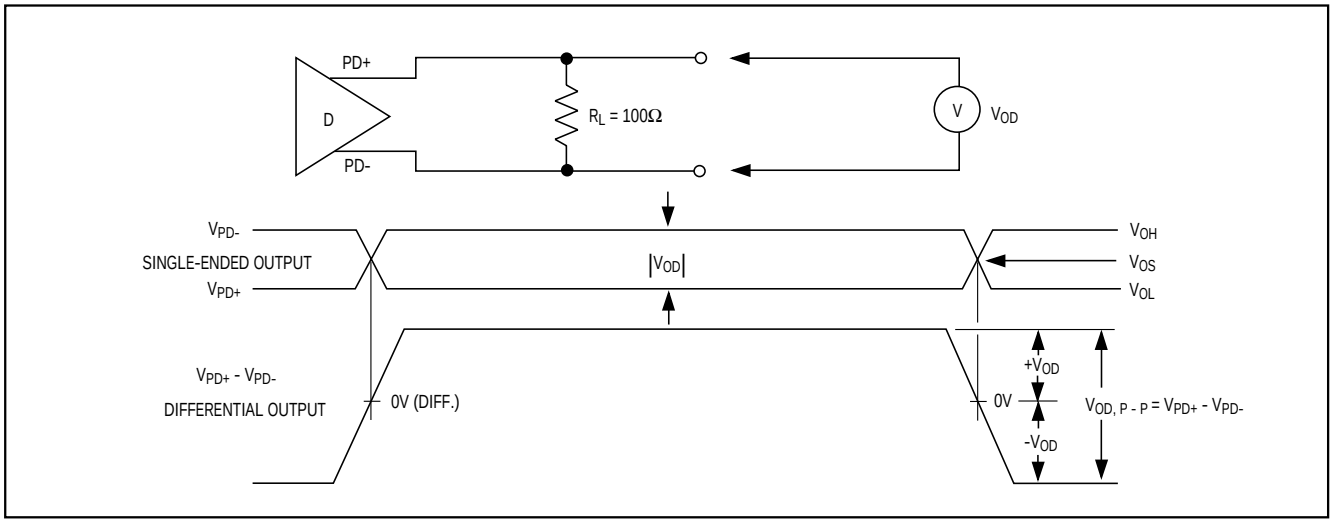


Figure 1. Driver Output Levels

Detailed Description

The MAX3885 deserializer uses a 16-bit shift register, 16-bit parallel output register, 4-bit counter, PECL input buffers, and low-voltage differential-signal (LVDS) input/output buffers to convert 2.488Gbps serial data to 16-bit wide, 155Mbps parallel data (Figure 2). The input shift register continuously clocks incoming data on the positive transition of the serial clock (SCLK) input signal. The 4-bit counter generates a parallel-output clock (PCLK) by dividing the serial-clock frequency by 16. The PCLK signal clocks the parallel-output register. During normal operation, the counter divides the SCLK frequency by 16, causing the output register to latch every 16 bits of incoming serial data. The synchronization inputs (SYNC+, SYNC-) realign and reframe data. When the SYNC signal is pulsed high for at least four SCLK cycles, the parallel output data is delayed by one SCLK cycle. This realignment is guaranteed to occur within two complete PCLK cycles of the SYNC signal's positive transition. As a result, the first incoming bit of data during that PCLK cycle is dropped, shifting the alignment between PCLK and data by one bit. See Figure 3 for the timing diagram and Figure 4 for the timing parameters diagram.

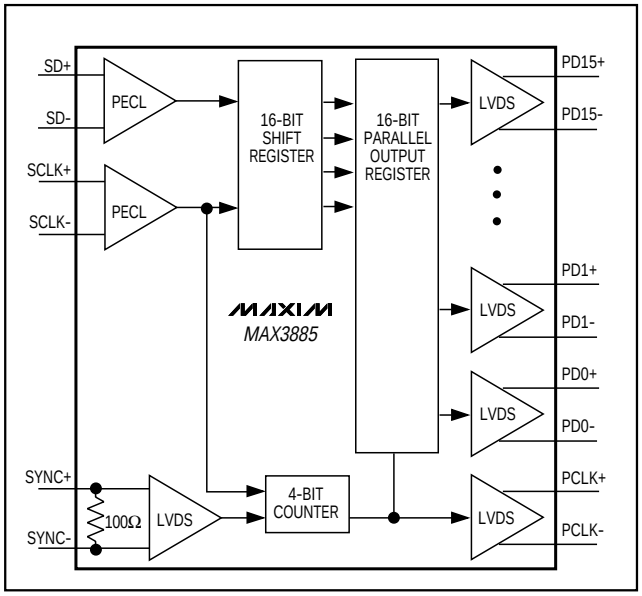


Figure 2. Functional Diagram

Low-Voltage Differential-Signal (LVDS) Inputs and Outputs

The MAX3885 features LVDS inputs and outputs for interfacing with high-speed digital circuitry. The LVDS standard is based on the IEEE 1596.3 LVDS specification. This technology uses 500mVp-p to 800mVp-p differential low-voltage swings to achieve fast transition times, minimize power dissipation, and improve noise immunity. The parallel clock and data LVDS outputs (PCLK+, PCLK-, PD_+, PD_-) require 100Ω differential

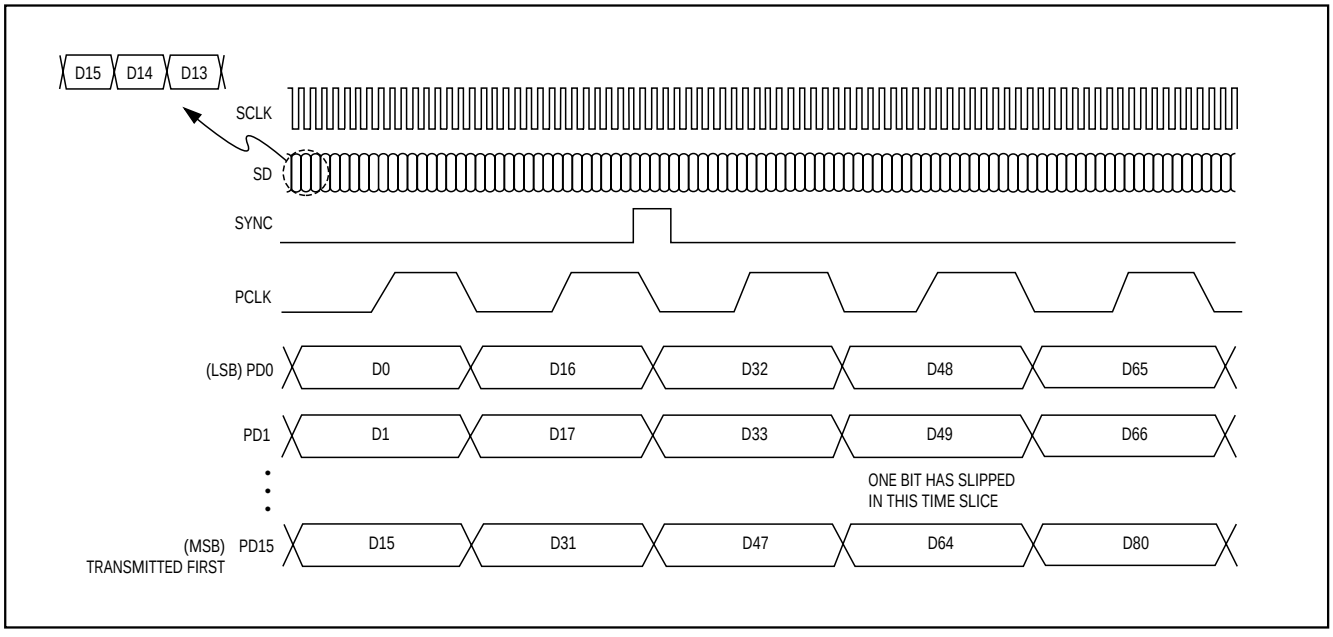


Figure 3. Timing Diagram

+3.3V, 2.488Gbps, SDH/SONET 1:16 Deserializer with LVDS Outputs

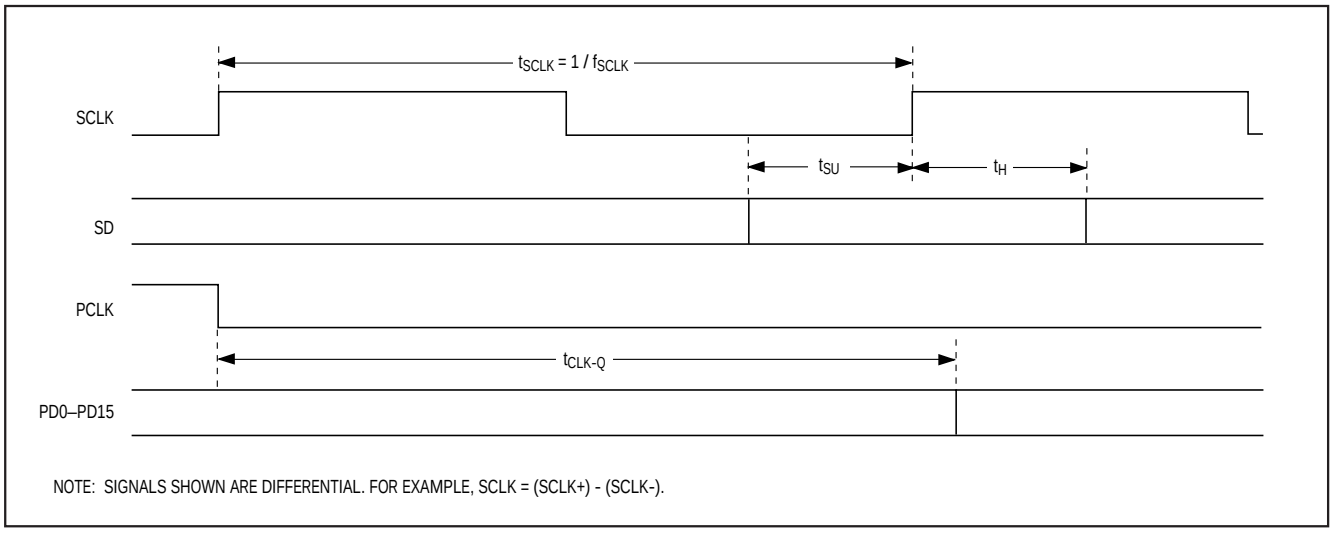


Figure 4. Timing Parameters

DC termination between the inverting and noninverting outputs for proper operation. Do not terminate these outputs to ground. The synchronization LVDS inputs (SYNC+, SYNC-) are internally terminated with 100Ω differential input resistance and, therefore, do not require external termination.

PECL Inputs

Because of the self-biasing resistor networks, the serial data and clock PECL inputs (SD+, SD-, SCLK+, SCLK-) require 53Ω termination to V_{CC} - 2V when interfacing with a PECL source (see *Alternative PECL Input Termination*). This results in an equivalent input resistance of 50Ω.

Applications Information

Alternative PECL Input Termination

Figure 5 shows alternative PECL input-termination methods. Use Thevenin-equivalent termination when a V_{CC} - 2V termination voltage is not available. When interfacing with an ECL-output device, the MAX3885's internal self-biasing allows easy ECL AC-coupling termination.

Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies and keep ground connections short. Use multiple vias where possible. Also, use controlled impedance transmission lines to interface with the MAX3885 high-speed inputs and outputs.

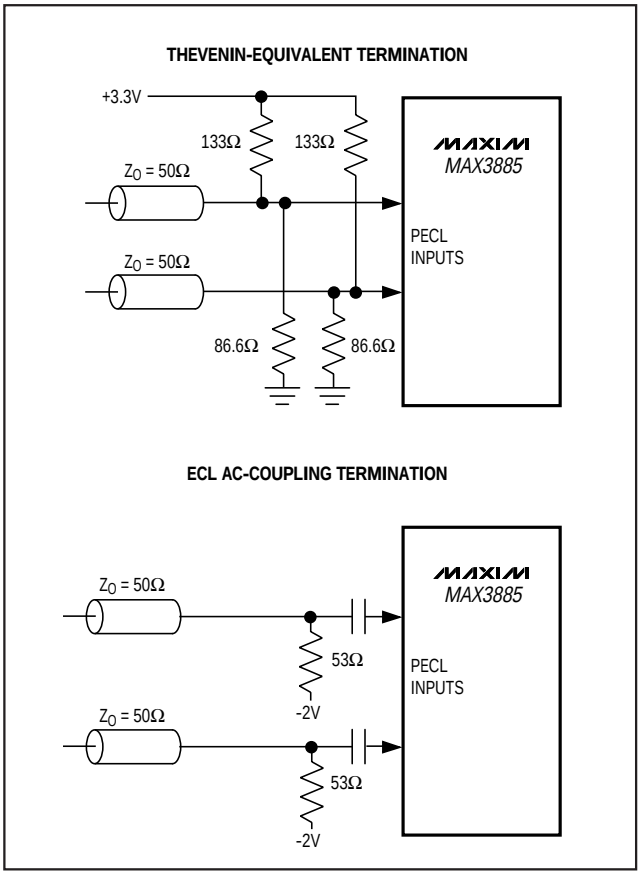
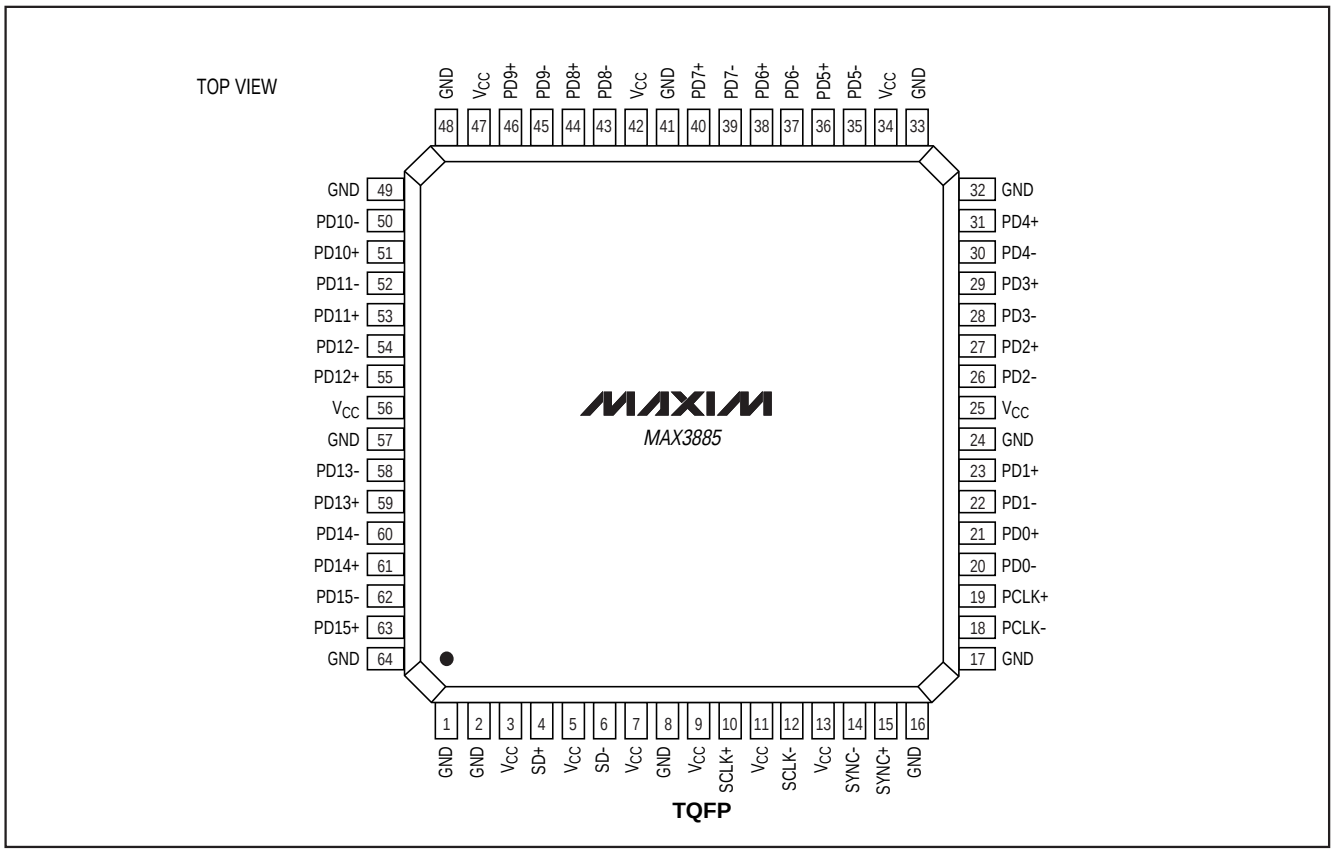


Figure 5. Alternative PECL Input Termination

Pin Configuration



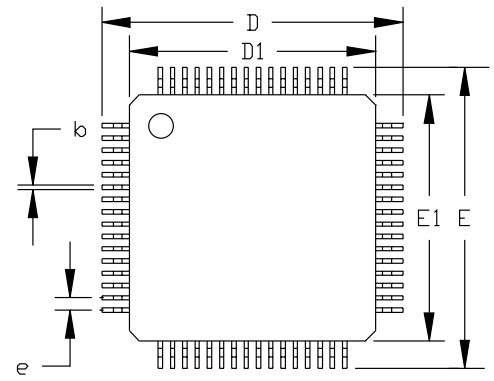
Chip Information

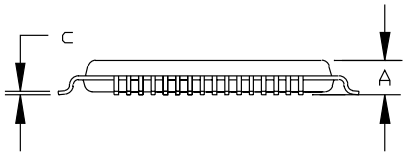
TRANSISTOR COUNT: 2820

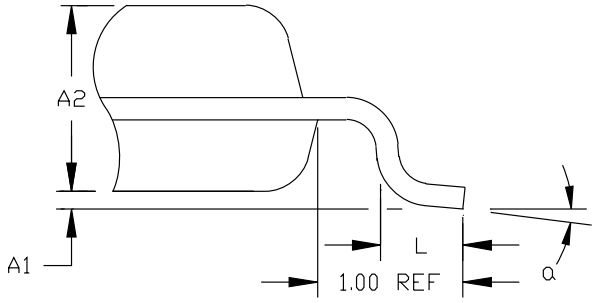
+3.3V, 2.488Gbps, SDH/SONET 1:16 Deserializer with LVDS Outputs

Package Information

TQFPPO.EPS







JEDEC VARIATION						
	BC		BE		BJ	
	32 LEAD		48 LEAD		64 LEAD	
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
A	---	1.60	---	1.60	---	1.60
A_1	0.05	0.15	0.05	0.15	0.05	0.15
A_2	1.35	1.45	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10	12.00 BSC.	
D_1	7.00 BSC.		7.00 BSC.		10.00 BSC.	
E	8.90	9.10	8.90	9.10	12.00 BSC.	
E_1	7.00 BSC.		7.00 BSC.		10.00 BSC.	
e	0.8 BSC.		0.5 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27	0.17	0.27
c	0.09	0.20	0.09	0.20	0.09	0.20
α	0°	7°	0°	7°	0°	7°

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS BC, BE AND BJ.

MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, TQFP

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0054	C	1/1