Features

- Meets jitter requirements for AT&T TR62411 Stratum 4 and Stratum 4 Enhanced for DS1 interfaces, and for ETSI ETS300 011 for E1 interfaces
- Provides C1.5, $\overline{C3}$, C2, $\overline{C4}$, C8 and $\overline{C16}$ output clock signals
- Provides 3 kinds of 8kHz framing signals
- Selectable 1.544MHz, 2.084MHz or 8kHz input reference signals
- Operates in either Normal or Free-Run states
- Enhanced in jitter and duty cycle comparing with PT7A4401B
- Package: 28-pin PLCC (PT7A4401CJ)

Applications

- Synchronization and timing control for multitrunk T1 and E1 systems
- ST-BUS clock and frame pulse sources

Introduction

PT7A4401C is functionally enhanced version of PT7A4401B. It has better jitter performance and C16 whose output duty cycle is independent of 20MHz master clock.

The PT7A4401C employs a digital phase-locked loop (DPLL) to provide timing and synchronizing signals for multitrunk T1 and E1 primary rate transmission links. It generates the ST-BUS clock and framing signals that are phase-locked to input reference signals of either 2.048MHz, 1.544MHz or 8kHz.

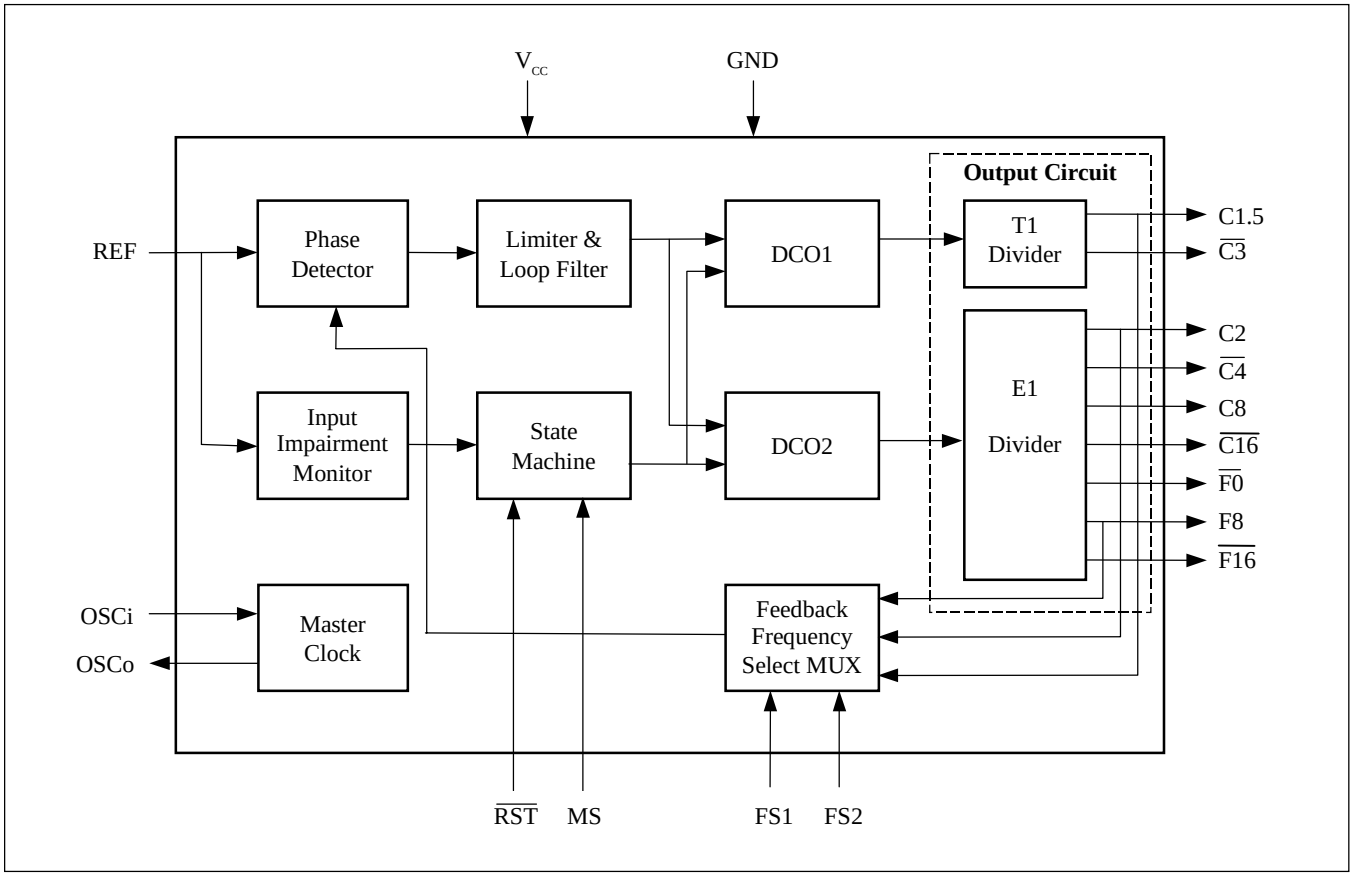
The PT7A4401C is compliant with AT&T TR62411 Stratum 4 and Stratum 4 Enhanced, and ETSI ETS 300 011. It meets the requirements for jitter tolerance, jitter transfer, intrinsic jitter, frequency accuracy, capture range and phase slope, etc.

Contents

Contents **Page**

Block Diagram

Figure 1. Block Digram



Pin Information

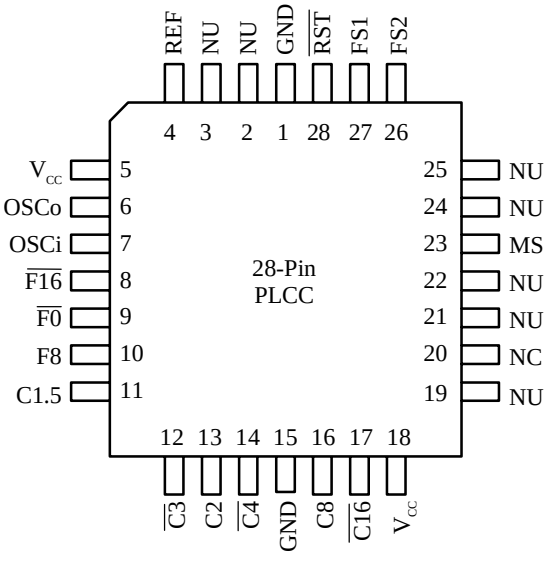
Pin Assignment

Table 1. Pin Assignment

Groups	Symbols	Functions
Chip Clock	OSCi, OSCo	Clock
Power & Ground	V_{CC}, GND	Power
Clock and Framing Output	C1.5, $\overline{C3}$, C2, $\overline{C4}$, C8, $\overline{C16}$, $\overline{F0}$, F8, $\overline{F16}$	Clock and Framing Signals
Control Signals	MS, FS1, FS2, $\overline{RST}$	Control
Reference Input	REF	Reference Clock

Pin Configuration

Figure 2. Pin Configuration



Top View

Pin Description

Table 2. Pin Description

Pin	Name	Type	Description
1, 15	GND	Ground	**Ground (0V)**
2, 3, 19, 21, 22, 24, 25	NU	I	**Not Used** (should be connected to ground)
4	REF	I	**Reference Input (TTL compatible**): Input reference signals
5, 18	V_{cc}	Power	**Power Supply (+5V)**
6	OSCo	O	**Oscillator Master Clock Output (CMOS):** Output of 20MHz master clock
7	OSCi	I	**Oscillator Master Clock Input (CMOS):** Input of 20MHz master clock (can be connected directly to a clock source)
8	$\overline{F16}$	O	**Frame Pulse Output (CMOS Compatible**): 8kHz framing output pulse that indicates the start of the ST-BUS frame. The pulse width is based upon the period of the 16.384MHz synchronization clock.
9	$\overline{F0}$	O	**Frame Pulse Output (CMOS Compatibl**e): 8kHz output framing pulse that indicates the start of the active ST-BUS frame. The pulse width is based upon the period of the 4.096MHz synchronization clock.
10	F8	O	**Frame Pulse Output (CMOS Compatible**): 8kHz output framing pulse that indicates the start of the active ST-BUS frame. The pulse width is based upon the period of the 8.192MHz synchronization clock.
11	C1.5	O	**1.544MHz Clock (CMOS Compatible)**
12	$\overline{C3}$	O	**3.088MHz Clock (CMOS Compatible)**
13	C2	O	**2.048MHz Clock (CMOS Compatible)**
14	$\overline{C4}$	O	**4.096MHz Clock (CMOS Compatible)**
16	C8	O	**8.192MHz Clock (CMOS Compatible)**
17	$\overline{C16}$	O	**16.384MHz Clock (CMOS Compatible)**
20	NC	O	**Not Connected:** Make no connection to this pin.
23	MS	I	**Mode Select (TTL Compatible):** This input selects the operation mode of the device, i.e., Normal or Freerun. Refer to Table 4.
26	FS2	I	**Frequency Select 2 (TTL Compatible):** This input, together with FS1, selects the frequency of the input reference signal, either 8kHz, 1.544MHz or 2.048MHz. Refer to Table 3.
27	FS1	I	**Frequency Select 1 (TTL Compatible):** Refer to the pin description of FS2.
28	$\overline{RST}$	I	**Reset (CMOS Input Schmitt Trigger):** Reset the device when at low level. The reset is needed when power-up or when frequency select input change to ensure proper operation. The time constant for a power-up reset circuit must be a min. of five times the rise time of the power supply. In normal operation, the $\overline{RST}$ pin must be held low for a min. of 300 ns to reset the device. When $\overline{RST}$ at low level, all outputs are fixed at HIGH.

Functional Description

Overall Operation

The PT7A4401C is a multitrunk synchronizer that provides the clock and frame signals for T1 and E1 primary rate digital transmission links.

It basically consists of the Master Clock Circuit, Digital Phase-Locked Loop (DPLL), Input Impairment Monitor and Output Circuit.

The DPLL circuit is employed to provide synchronization of the output signals.

Referring to the block diagram on Page 3, the detailed functions of the PT7A4401C are described as follows.

Master Clock

As its master clock, the PT7A4401C uses either an external clock source or an external crystal and a few discrete components with its internal oscillator.

Major Digital Phase-Locked Loop (DPLL) Block

The major DPLL blocks are the Phase Detector, Limiter, Loop Filter, and Digitally Controlled Oscillators (DCO1 and DCO2).

The input signal is sent to the Phase Detector for comparison with the feedback Signal from the Feedback Frequency Select MUX. An error signal corresponding to their instantaneous phase difference is produced and sent to the Limiter.

The Limiter amplifies this error signal to ensure that the DPLL responds to all input transient conditions with a maximum output phase slope of 5ns per 125µs. This performance easily meets the maximum phase slope of 7.6ns per 125µs or 81ns per 1.326ms specified by AT&T TR62411.

The Loop Filter is a 1.9Hz low pass filter for all three reference frequency selections: 8kHz, 1.544MHz and 2.048MHz. This filter ensures that the jitter transfer requirements in ETS 300-011 and AT&T TR62411 are met.

The Error Signal, after being limited and filtered, is sent to two Digitally Controlled variable frequency Oscillators (DCO1 and DCO2). Based upon the processed error value, the DCOs will generate the corresponding digital output signals to the Output Circuit to produce 12.352MHz and 16.384MHz signals.

The DCO synchronization method depends upon the PT7A4401C operating state, as follows:

In Normal state, each DCO generates an output signal which is frequency and phase locked to the input reference signal.

In Auto-Holdover state, each DCO generates an output signal whose frequency is equal to what it was for a 30ms period shortly before the end of the last Normal State.

In Free-Run state, the DCOs are free running with an accuracy equal to the accuracy of the OSCi 20MHz source.

Output Circuit

Signals from the two DCOs are sent to the Output Circuit to generate two clock signals, 12.352MHz and 16.384MHz, which are divided in the T1 and E1 Dividers respectively to provide needed clock and frame signals.

The T1 Divider uses the 12.352MHz signal to generate two clock signals, C1.5 and $\overline{C3}$. They have a nominal 50% duty cycle.

The E1 Divider uses the 16.384MHz signal to generate four clock signals and three frame signals, i.e., C2, $\overline{C4}$, C8, $\overline{C16}$, F0, F8 and $\overline{F16}$. The frame signals are generated directly from the C16 signal.

The C2, $\overline{C4}$ and C8 signals have a nominal 50% duty cycle, and C16's duty cycle is about 50% if the master clock has a 50% duty cycle.

All the frame and clock outputs are locked to each other for all operating states. They have limited driving capability and should be buffered when driving high capacitance loads.

Feedback Frequency Selection MUX

The feedback frequency is selected by FS1 and FS2 (as shown in Table 3) to match the particular incoming reference frequency (1.544MHz, 2.048MHz or 8kHz). A reset ($\overline{RST}$) must be performed after every frequency select input change.

Input Impairment Monitor

This circuit monitors the input signal to the DPLL and automatically enables Auto-Holdover state when the incoming signal is completely lost, or if its frequency is outside the Auto-holdover capture range (either a small or large amount). When the incoming signal returns to normal, the DPLL will be returned to Normal State.

Table 3. Input Frequency Selection

FS2	FS1	Input Frequency
0	0	Reserved
0	1	8kHz
1	0	1.544MHz
1	1	2.048MHz

State Machine

If the value of MS is 1, the "Free-Run" state of operation is forced. If the value of MS is 0, the state of operation is either "Normal" or "Auto-Holdover", depending upon the state of the Input Impairment Monitor. See Table 4.

Table 4. Operation State Selection

MS	Operation State
0	Normal
1	Freerun

States of Operation

Typically, the PT7A4401C operates in either the Normal or Free-Run state. However, when the input signal is temporarily missing or its frequency is temporarily out of specification, it operates in Auto-Holdover State (Refer to Table 7).

Normal State

In Normal State, the output signals of the PT7A4401C are synchronized with the input reference signal by the DPLL.

Free-Run State

Typically, the Free-Run State is used immediately following system power-up before network synchronization is achieved, or when a master clock is otherwise required.

In Free-Run State, the outputs of the PT7A4401C are uncorrelated with the input reference signal (and the stored information concerning the output reference signals). Instead, these output signals are based solely on the master clock frequency (OSCi).

Auto-Holdover State

The Auto-Holdover State will be automatically initiated when incoming reference signal disappears or its frequency moves outside the Auto-holdover capture range (Table 7), by either a small or large amount.

In Auto-Holdover State, the PT7A4401C output signals are not synchronized with the external input reference signal. Instead, they are generated by using the information stored 30 ms to 60ms before the incoming reference signal became unusable.

While in Normal State, a numerical value related to the output reference frequency is stored alternately in two memory locations every 30ms. Whenever the device is switched into Auto-Holdover State, the value in memory between 30ms and 60ms is used to set the output frequency of the device.

Applications Information

Master Clock

The PT7A4401C uses either an external clock source or an external crystal and a few passive components with its internal oscillator as the master timing source.

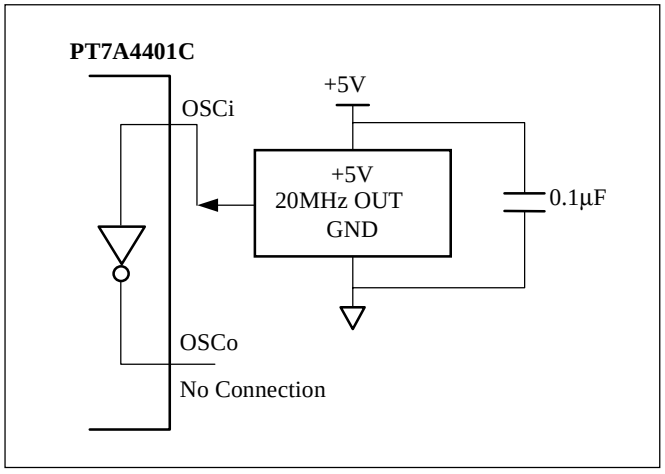
In Free-Run State, the frequency tolerance of the PT7A4401C output clocks are equal to the frequency tolerance of the timing source. In a given application, if an accurate Free-Run State is not required, the tolerance of the master timing source may be 100ppm. If required, the tolerance must be no worse than 32 ppm.

The capture range of PT7A4401C must also be considered when deciding the accuracy of the master timing source. The sum of the accuracy of the master timing source and the capture range of the PT7A4401C will always equal 230ppm. For example, if the master timing source is 100ppm, the capture range will be 130ppm.

• Clock Oscillator

If using an external clock source, its output pin should be connected directly (not AC coupled) to the OSCi pin of the PT7A4401C, and the OSCo pin can be left open as shown in Figure 3 or connected as an output pin.

Figure 3. Clock Oscillator Connection



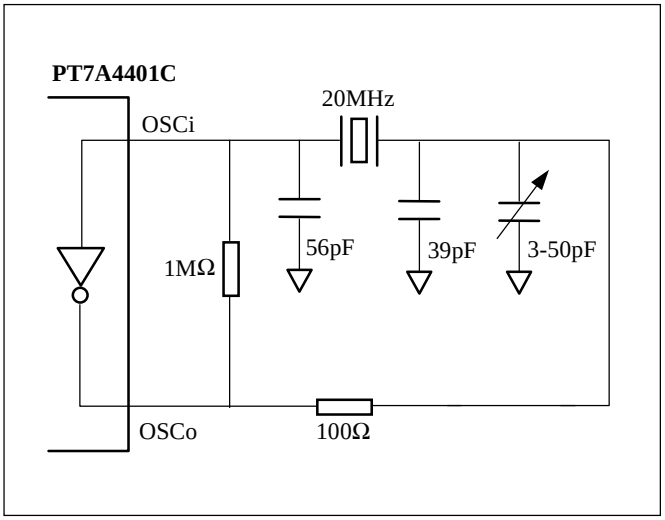
When selecting the clock oscillator, following specifications should be considered. They are

- absolute frequency
- frequency change over temperature
- output rise and fall time
- output level
- duty cycle

• Crystal Oscillator

If a crystal and passive components operating together with the PT7A4401C oscillator are selected as the master timing source, they should be connected as shown in Figure 4. It should be possible to adjust the trimmer capacitor so that the frequency is well within the 32 ppm tolerance; however, only the proper specification of components will insure this tolerance over the necessary temperature range.

Figure 4. Crystal Oscillator Connection



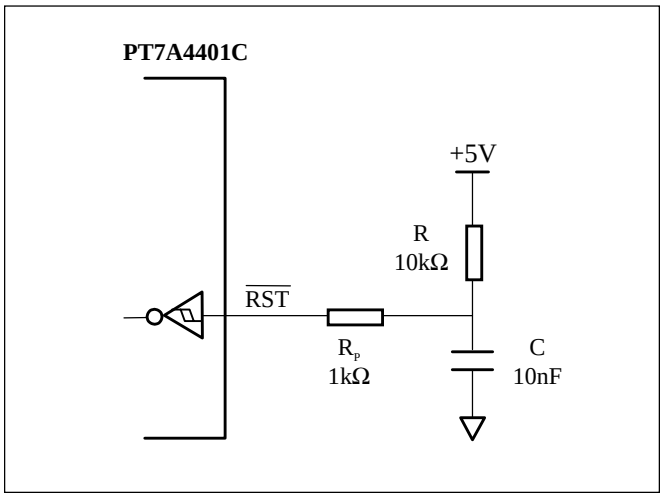
The crystal specification is as follows:

- Frequency:	20MHz
- Tolerance:	as required
- Oscillation Mode:	Fundamental
- Resonance Mode:	Parallel
- Load Capacitance:	32pF
- Maximum Series Resistance:	35Ω
- Approximate Drive Level:	1mW

Reset Circuit

A simple power-up reset circuit with about a 50µs reset active (low) time is shown in Figure 5. Resistor R_P is used for protection only. The reset time is not critical but should be greater than 300ns.

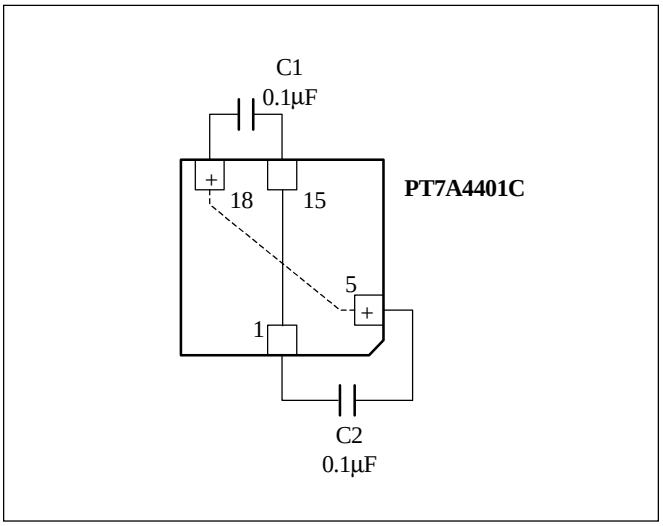
Figure 5. Power-up Reset Circuit



Power Supply Decoupling

The PT7A4401C has two V_{CC} pins and two GND pins. Power decoupling capacitors should be included as shown in Figure 6.

Figure 6. Power Supply Decoupling



Detailed Specifications

Definitions of Critical Performance Specifications

Intrinsic Jitter: Intrinsic jitter is the jitter produced by the synchronizing circuit. It is measured by applying a reference signal with no jitter to the input of the device, and measuring its output jitter. Intrinsic jitter may also be measured when the device is in a non-synchronizing mode--such as free running or auto-holdover--by measuring the output jitter of the device. Intrinsic jitter is usually measured with various band limiting filters depending on the applicable standards.

Jitter Tolerance: Jitter tolerance is a measure of the ability of a PLL to operate properly (i.e., remain in lock and/or regain lock in the presence of large jitter magnitudes at various jitter frequencies) when jitter is present on its reference. The applicable standard specifies how much jitter to apply to the reference when testing for jitter tolerance.

Jitter Transfer: Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device with respect to a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standard.

Its 3 possible input frequencies and 9 outputs gives the PT7A4401C 27 possible jitter transfer combinations. However, only three cases of the jitter transfer specifications are given in the AC Electrical Characteristics; as the remaining combinations can be derived from them.

For the PT7A4401C, jitter attenuation is determined by the internal 1.9Hz low pass loop filter and phase slope limiter. The phase slope limiter limits the output phase slope to 5ns/125µs. Therefore, if the input signal exceeds this rate, such as for very large amplitude low frequency input jitter, the maximum output phase slope will be limited (i.e., attenuated) to 5ns/125µs.

It should be noted that 1UI at 1.544MHz (644ns) is not equal to 1UI at 2.048MHz (488ns). A transfer value using different input and output frequencies must be calculated in common units (e.g., seconds) as shown in the following example.

Example - When the T1 input jitter is 20UI (T1 UI Units) and the T1 to T1 jitter attenuation is 18dB, the T1 and E1 output jitter can be calculated as follows:

$$J_{T1o} = J_{T1i} \times 10^{\left(\frac{-A}{20}\right)} = 20 \times 10^{\left(\frac{-18}{20}\right)} = 2.5UI$$

$$J_{E1o} = J_{T1o} \times \left(\frac{1UIT1}{1UIE1}\right) = J_{T1o} \times \left(\frac{644ns}{488ns}\right) = 3.3UI$$

Using the above method, the jitter attenuation can be calculated for all combinations of inputs and outputs based upon the three jitter transfer functions provided.

Note that the resulting jitter transfer functions for all combinations of inputs (8kHz, 1.544MHz, 2.048MHz) and outputs (8kHz, 1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, 16.384MHz) for a given input signal (jitter frequency and jitter amplitude) are the same.

As intrinsic jitter is always present, jitter attenuation will appear to be lower for small input jitter signals than for large ones. Consequently, accurate jitter transfer function measurements are usually made with large input jitter signals (e.g., 75% of the specified maximum jitter tolerance).

Frequency Accuracy: Frequency accuracy is defined as the absolute tolerance of an output clock signal when it is operating in a free running mode (not locked to an external reference). For the PT7A4401C, Free-Run accuracy is equal to the Master Clock (OSCi) accuracy.

Auto-Holdover Accuracy: Auto-Holdover accuracy is defined as the absolute tolerance of an output clock signal, when it is not locked to an external reference signal, but is operating using storage techniques. For the PT7A4401C the storage value is determined while the device is in Normal State and locked to an external reference signal. The absolute Master Clock (OSCi) accuracy of the PT7A4401C does not affect Auto-Holdover accuracy, but the change in OSCi accuracy while in Auto-Holdover State does.

Lock Range: If the PT7A4401C DPLL is already in a state of synchronization ("lock") with the incoming reference signal, it is able to track this signal to maintain lock as its frequency varies over a certain range, called the Lock Range. The size of Lock Range is related to the range of the Digitally Controlled Oscillators and is equal to 230ppm minus the accuracy of the master clock (OSCi). For example, a 32ppm master clock results in a Lock Range of 198ppm.

Capture Range: If the PT7A4401C DPLL is not at present in a state of synchronization (lock) with the incoming reference signal, it is able to initiate (acquire) lock only if the signal's frequency is within a certain range, called the Capture Range. For any PLL, no portion of the Capture Range can fall outside the Lock Range, and, in general, the Capture Range is more narrow than the Lock Range. However, owing to the design of its Phase Detector, the PT7A4401C's Capture Range is equal to its Lock Range.

Phase Slope: Phase slope is measured in seconds per second and is defined as the rate at which a given signal changes phase with respect to an ideal signal of constant frequency. The given signal is typically the output signal. The ideal signal has a constant frequency that is nominally equal in value to that of the final output signal or final input signal.

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Ambient Temperature with Power Applied ..... -40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V_{CC} Only) ..... -0.3 to 7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only) .. -0.3 to 7.0V
DC Input Voltage ..... -0.3 to 7.0V
DC Output Current 120mA
Power Dissipation 900mW

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Table 5. Recommended Operating Conditions

Sym	Description	Test Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage	Over Recommended Operating Conditions	4.5	5.0	5.5	V
T_A	Operating Temperature		-40	25	85	°C

Note:
Typical figures are at 25°C and are for design aid only; not production tested.

DC Electrical and Power Supply Characteristics

Table 6. DC Electrical and Power Supply Characteristics

Sym	Description	Test Conditions	Min	Typ	Max	Units
I_{CCO}	Quiescent Power Supply Current	OSCi = 0V, Note 2			500	µA
I_{CC}	Supply Current				50	mA
I_{CC}		OSCi = Crystal, Note 2			60	mA
V_{IH}	TTL HIGH Input Voltage-All pins except OSCi, $\overline{RST}$		2.0			V
V_{IL}	TTL LOW Input Voltage-All pins except OSCi, $\overline{RST}$				0.8	V
V_{CIH}	CMOS HIGH Input Voltage-OSCi pin		$0.7V_{CC}$			V
V_{CIL}	CMOS LOW Input Voltage-OSCi pin				$0.3V_{CC}$	V
V_{SIH}	Schmitt HIGH Input Voltage-$\overline{RST}$ pins		3.6			V
V_{SIL}	Schmitt LOW Input Voltage-$\overline{RST}$ pins				1.5	V
V_{HYS}	Schmitt Hysteresis Voltage-$\overline{RST}$ pins			1.0		V
I_{IL}	Input Leakage Current	$V_I = V_{CC}$ or 0V			±10	µA
V_{OH}	HIGH Output Voltage	I_{OH} = 4mA	2.4			V
V_{OL}	LOW Output Voltage	I_{OL} = 4mA			0.8	V

Note:
1. V_{CC} = 5V,
2. MS = V_{CC} (Freerun), FS1 = V_{CC}, FS2 = GND, REF = GND, other inputs connected to GND.
3. All outputs are unloaded except for V_{OH} and V_{OL} measurement.

AC Electrical Characteristics

Performance

Table 7. Performance

Sym	Description		Test Conditions*	Min	Typ	Max	Units
	Freerun State Accuracy with OSCi at:	0ppm	3	0		0	ppm
		32ppm		-32		+32	ppm
		100ppm		-100		+100	ppm
	Capture Range With OSCi at:	0ppm	1, 4-6	-190		+230	ppm
		32ppm		-158		+198	ppm
		100ppm		-90		+130	ppm
	Phase Lock Time		1, 4-12			30	s
	Output Phase Slope		1-12, 25			45	µs/s

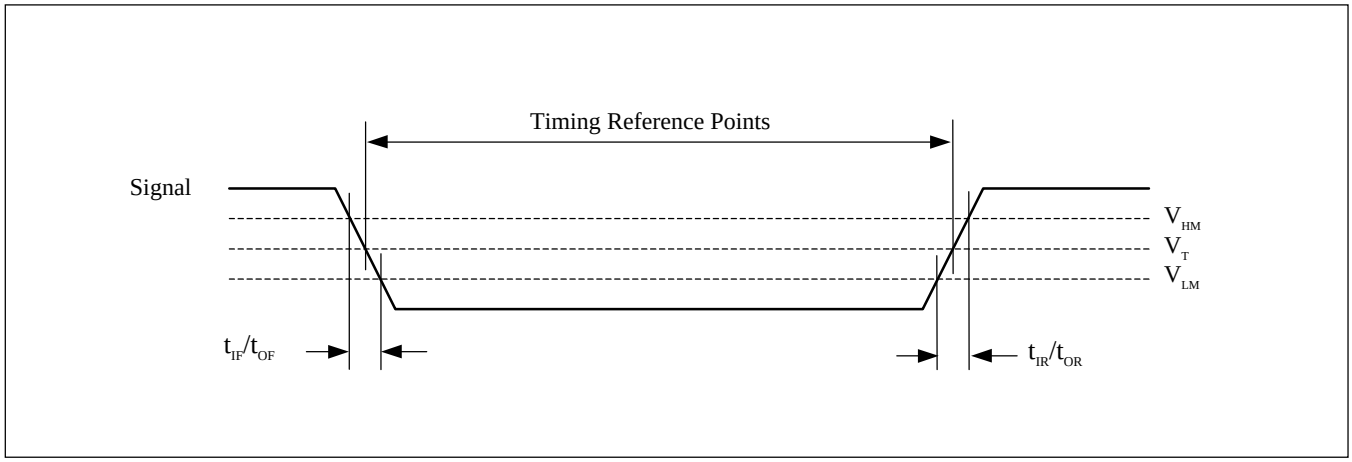
* Refer to the **Test Conditions** on Page 24 for details.

Voltage Levels for Timing Parameter Measurement

Table 8. Voltage Levels for Timing Parameter Measurement

Sym	Description	Schmitt (for $\overline{RST}$)	TTL	CMOS (for OSCi)	Units
V_T	Threshold Voltage	1.5	1.5	$0.5V_{CC}$	V
V_{HM}	Rising and Falling Threshold Voltage High	2.4	2.0	$0.7V_{CC}$	V
V_{LM}	Rising and Falling Threshold Voltage Low	0.8	0.8	$0.3V_{CC}$	V

Figure 7. Voltage Levels for Timing Parameter Measurement



Timing Characteristics

Table 9. Timing Characteristics

Sym	Description	Test Conditions*	Min	Typ	Max	Units
t_{RW}	Reference Input Pulse Width High or Low	1, 4-9, 37	100			ns
t_{IR}/t_{IF}	Reference Input Rising or Falling Time				10	ns
t_{R8D}	8kHz Reference Input to F8 Delay	1, 4-12, 19, 21, 36	-28		-1	ns
t_{R15D}	1.544MHz Reference Input to F8 Delay		337		363	ns
t_{R2D}	2.048MHz Reference Input to F8 Delay		217		238	ns
t_{F0D}	F8 to $\overline{F0}$ Delay	1-12, 19, 37	110		134	ns
t_{F16D}	F8 to $\overline{F16}$ Delay	1-12, 19	19		44	ns
t_{C15D}	F8 to C1.5 Delay	1-12, 19, 37	-45		-31	ns
t_{C3D}	F8 to $\overline{C3}$ Delay		-46		-31	ns
t_{C2D}	F8 to C2 Delay		-10		5	ns
t_{C4D}	F8 to $\overline{C4}$ Delay		-10		5	ns
t_{C8D}	F8 to C8 Delay		-10		5	ns
t_{C16D}	F8 to $\overline{C16}$ Delay		-10		5	ns
t_{C15W}	C1.5 Pulse Width High or Low		309		339	ns
t_{C3W}	$\overline{C3}$ Pulse Width High or Low		149		175	ns
t_{C2W}	C2 Pulse Width High or Low		230		258	ns
t_{C4W}	$\overline{C4}$ Pulse Width High or Low		111		133	ns
t_{C8W}	C8 Pulse Width High or Low		52		70	ns

* Refer to the **Test Conditions** on Page 24 for details.

Note:

1. Typical figures are at 25°C and are for design aid only; not production tested.
2. The maximum and minimum timing is measured under recommended temperature conditions and power supplies.
3. TTL voltage levels are used for timing parameter measurement.

Table 9. Timing Characteristics (Continued)

Sym	Description	Test Conditions*	Min	Typ	Max	Units
t_{C16WL}	$\overline{C16}$ Pulse Width Low	1-12, 19	26		37	ns
t_{F0WL}	$\overline{F0}$ Pulse Width Low	1-12, 19, 37	230		258	ns
t_{F8WH}	F8 Pulse Width High		111		133	ns
t_{F16WL}	$\overline{F16}$ Pulse Width Low		52		70	ns
t_{ORF}	Output Clock and Frame Pulse Rising or Falling Time				9	ns
t_S	Input Controls Setup Time		100			ns
t_H	Input Controls Hold Time		100			ns

* Refer to the **Test Conditions** on Page 24 for details.

Note:

1. Typical figures are at 25°C and are for design aid only; not production tested.
2. The maximum and minimum timing is measured under recommended temperature conditions and power supplies.
3. TTL voltage levels are used for timing parameter measurement.

Figure 8. Setup and Hold Timing of Input Controls

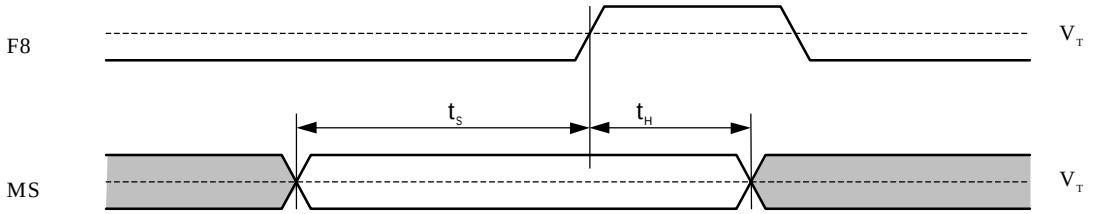
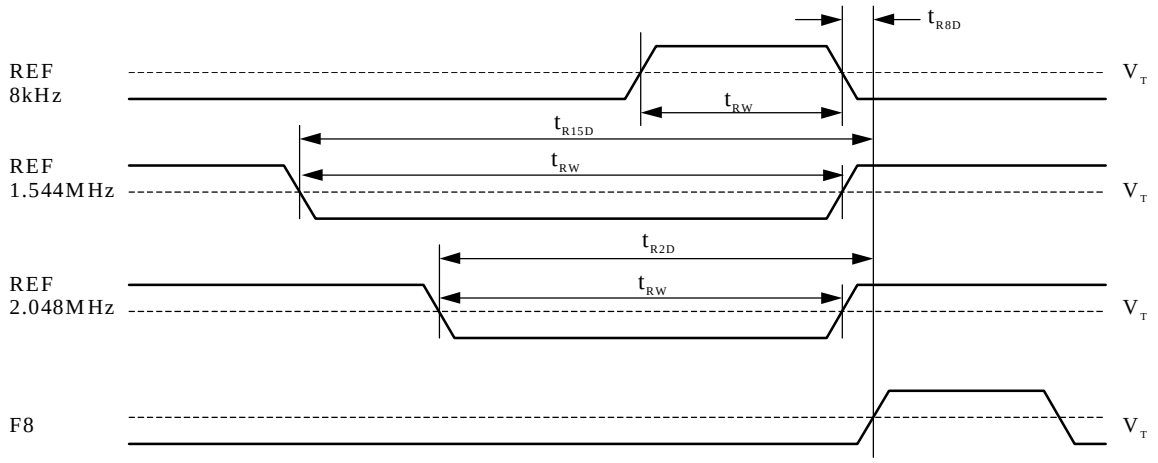
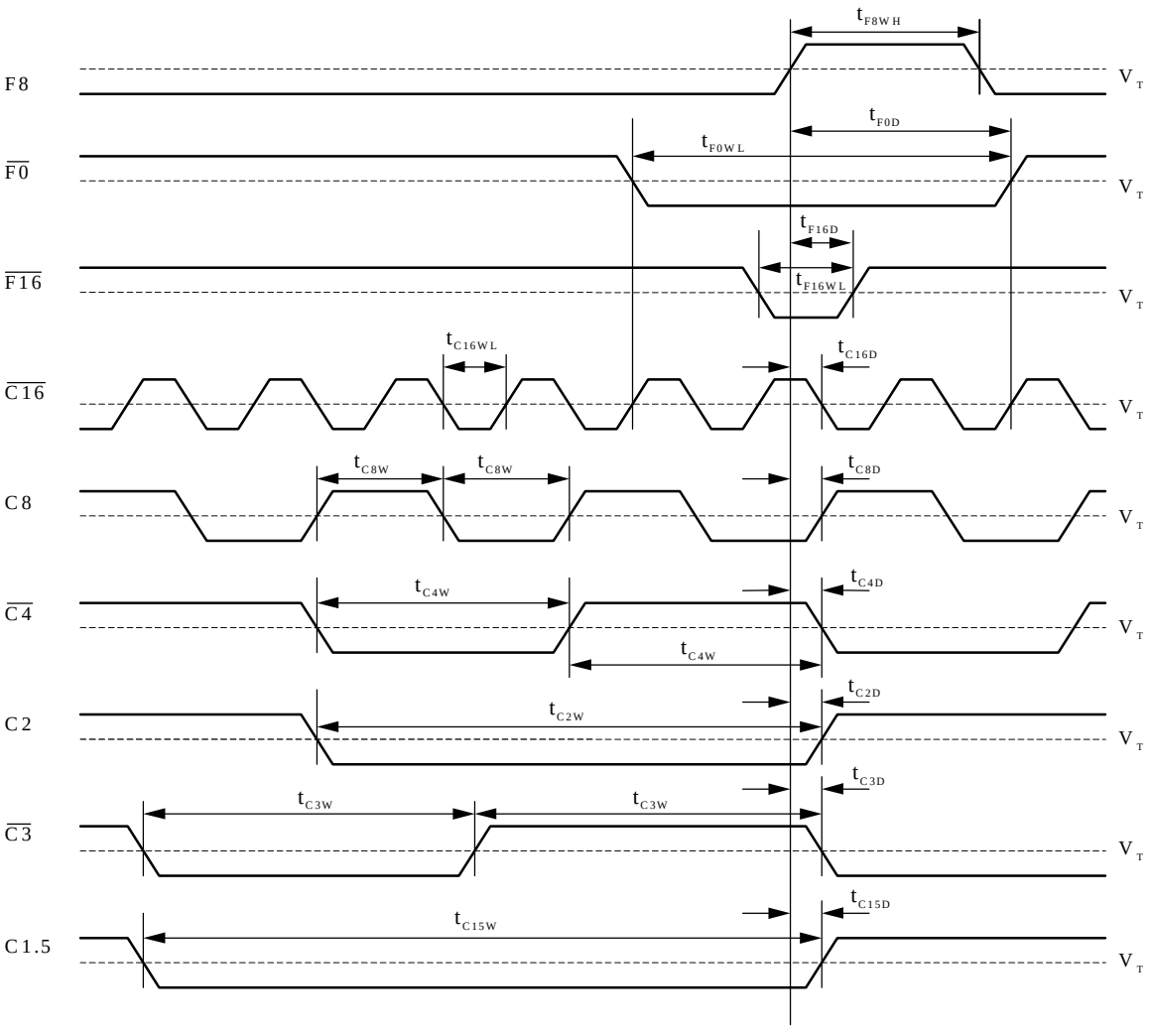


Figure 9. Timing Information for PT7A4401C



Note: Input to output delay values are valid after a $\overline{RST}$ with no further state changes.

Figure 10. Output Timing



Intrinsic Jitter Unfiltered

Table 10. Intrinsic Jitter Unfiltered

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Instrinsic Jitter at $\overline{F0}$ (8kHz)	1-12, 19-22, 26, 33		0.0001	0.0002	UIpp
	Instrinsic Jitter at F8 (8kHz)			0.0001	0.0002	UIpp
	Instrinsic Jitter at $\overline{F16}$ (8kHz)			0.0001	0.0002	UIpp
	Instrinsic Jitter at C1.5 (1.544MHz)	1-12, 19-22, 27, 33		0.016	0.030	UIpp
	Instrinsic Jitter at C2 (2.048MHz)	1-12, 19-22, 28, 33		0.020	0.040	UIpp
	Instrinsic Jitter at $\overline{C3}$ (3.088MHz)	1-12, 19-22, 29, 33		0.032	0.060	UIpp
	Instrinsic Jitter at $\overline{C4}$ (4.096MHz)	1-12, 19-22, 30, 33		0.047	0.080	UIpp
	Instrinsic Jitter at C8 (8.192MHz)	1-12, 19-22, 31, 33		0.09	0.16	UIpp
	Instrinsic Jitter at $\overline{C16}$ (16.384MHz)	1-12, 19-22, 32, 33		0.18	0.32	UIpp

* Refer to the **Test Conditions** on Page 24 for details.

C1.5 (1.544MHz) Instrinsic Jitter Filtered

Table 11. C1.5 (1.544MHz) Instrinsic Jitter Filtered

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Instrinsic Jitter (4Hz to 100kHz Filter)	1-12, 19-22, 27			0.015	UIpp
	Instrinsic Jitter (10Hz to 40kHz Filter)				0.010	UIpp
	Instrinsic Jitter (8kHz to 40kHz Filter)				0.010	UIpp
	Instrinsic Jitter (10Hz to 8kHz Filter)				0.005	UIpp

* Refer to the **Test Conditions** on Page 24 for details.

C2 (2.048MHz) Instrinsic Jitter Filtered

Table 12. C2 (2.048MHz) Instrinsic Jitter Filtered

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Instrinsic Jitter (4Hz to 100kHz Filter)	1-12, 19-22, 28			0.015	UIpp
	Instrinsic Jitter (10Hz to 40kHz Filter)				0.010	UIpp
	Instrinsic Jitter (8kHz to 40kHz Filter)				0.010	UIpp
	Instrinsic Jitter (10Hz to 8kHz Filter)				0.005	UIpp

* Refer to the **Test Conditions** on Page 24 for details.

8kHz Input to 8kHz Output Jitter Transfer

Table 13. 8kHz Input to 8kHz Output Jitter Transfer

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Jitter Attenuation for 1Hz with 0.01UIpp Input	1, 4, 7-12, 19, 20, 22, 26, 33	0		6	dB
	Jitter Attenuation for 1Hz with 0.54UIpp Input		6		16	dB
	Jitter Attenuation for 10Hz with 0.10UIpp Input		12		22	dB
	Jitter Attenuation for 60Hz with 0.10UIpp Input		28		38	dB
	Jitter Attenuation for 300Hz with 0.10UIpp Input		42			dB
	Jitter Attenuation for 3600Hz with 0.005UIpp Input		45			dB

* Refer to the **Test Conditions** on Page 24 for details.

1.544MHz Input to 1.544MHz Output Jitter Transfer

Table 14. 1.544MHz Input to 1.544MHz Output Jitter Transfer

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Jitter Attenuation for 1Hz with 20UIpp Input	1, 5, 7-12, 19, 20, 22, 27, 33	0		6	dB
	Jitter Attenuation for 1Hz with 104UIpp Input		6		16	dB
	Jitter Attenuation for 10Hz with 20UIpp Input		12		22	dB
	Jitter Attenuation for 60Hz with 20UIpp Input		28		38	dB
	Jitter Attenuation for 300Hz with 20UIpp Input		42			dB
	Jitter Attenuation for 10kHz with 0.3UIpp Input		45			dB
	Jitter Attenuation for 100kHz with 0.3UIpp Input		45			dB

* Refer to the **Test Conditions** on Page 24 for details.

2.048MHz Input to 2.048MHz Output Jitter Transfer

Table 15. 2.048MHz Input to 2.048MHz Output Jitter Transfer

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Jitter at Output for 1Hz 3.00UIpp Input	1,6,7-12,19,20,22,28,33			2.9	UIpp
		1,6,7-12,19,20,22,28,34			0.09	UIpp
	Jitter at Output for 3Hz 2.33UIpp Input	1,6,7-12,19,20,22,28,33			1.3	UIpp
		1,6,7-12,19,20,22,28,34			0.10	UIpp
	Jitter at Output for 5Hz 2.07UIpp Input	1,6,7-12,19,20,22,28,33			0.80	UIpp
		1,6,7-12,19,20,22,28,34			0.10	UIpp
	Jitter at Output for 10Hz 1.76UIpp Input	1,6,7-12,19,20,22,28,33			0.40	UIpp
		1,6,7-12,19,20,22,28,34			0.10	UIpp
	Jitter at Output for 100Hz 1.50UIpp Input	1,6,7-12,19,20,22,28,33			0.06	UIpp
		1,6,7-12,19,20,22,28,34			0.05	UIpp
	Jitter at Output for 2400Hz 1.50UIpp Input	1,6,7-12,19,20,22,28,33			0.04	UIpp
		1,6,7-12,19,20,22,28,34			0.03	UIpp
	Jitter at Output for 100kHz 0.20UIpp Input	1,6,7-12,19,20,22,28,33			0.04	UIpp
		1,6,7-12,19,20,22,28,34			0.02	UIpp

* Refer to the **Test Conditions** on Page 24 for details.

8kHz Input Jitter Tolerance

Table 16. 8kHz Input Jitter Tolerance

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Jitter Tolerance for 1Hz Input	1, 4, 7-12, 19, 20, 22-24, 26	0.80			UIpp
	Jitter Tolerance for 5Hz Input		0.70			UIpp
	Jitter Tolerance for 20Hz Input		0.60			UIpp
	Jitter Tolerance for 300Hz Input		0.20			UIpp
	Jitter Tolerance for 400Hz Input		0.15			UIpp
	Jitter Tolerance for 700Hz Input		0.08			UIpp
	Jitter Tolerance for 2400Hz Input		0.02			UIpp
	Jitter Tolerance for 3600Hz Input		0.01			UIpp

* Refer to the **Test Conditions** on Page 24 for details.

1.544MHz Input Jitter Tolerance

Table 17. 1.544MHz Input Jitter Tolerance

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Jitter Tolerance for 1Hz Input	1, 5, 7-12, 19, 20, 22-24, 27	150			UIpp
	Jitter Tolerance for 5Hz Input		140			UIpp
	Jitter Tolerance for 20Hz Input		130			UIpp
	Jitter Tolerance for 300Hz Input		35			UIpp
	Jitter Tolerance for 400Hz Input		25			UIpp
	Jitter Tolerance for 700Hz Input		15			UIpp
	Jitter Tolerance for 2400Hz Input		4			UIpp
	Jitter Tolerance for 10kHz Input		1			UIpp
	Jitter Tolerance for 100kHz Input		0.5			UIpp

* Refer to the **Test Conditions** on Page 24 for details.

2.048MHz Input Jitter Tolerance

Table 18. 2.048MHz Input Jitter Tolerance

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Jitter Tolerance for 1Hz Input	1, 6, 7-12, 19, 20, 22-24, 28	150			UIpp
	Jitter Tolerance for 5Hz Input		140			UIpp
	Jitter Tolerance for 20Hz Input		130			UIpp
	Jitter Tolerance for 300Hz Input		50			UIpp
	Jitter Tolerance for 400Hz Input		40			UIpp
	Jitter Tolerance for 700Hz Input		20			UIpp
	Jitter Tolerance for 2400Hz Input		5			UIpp
	Jitter Tolerance for 10kHz Input		1			UIpp
	Jitter Tolerance for 100kHz Input		1			UIpp

* Refer to the **Test Conditions** on Page 24 for details.

OSCi 20MHz Master Clock Input

Table 19. OSCi 20MHz Master Clock Input

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Tolerance	13, 16	0		0	ppm
		14, 17	-32		+32	ppm
		15, 18	-100		+100	ppm
	Duty Cycle		40		60	%
	Rise Time				10	ns
	Fall Time				10	ns

* Refer to the **Test Conditions** on Page 24 for details.

Notes:

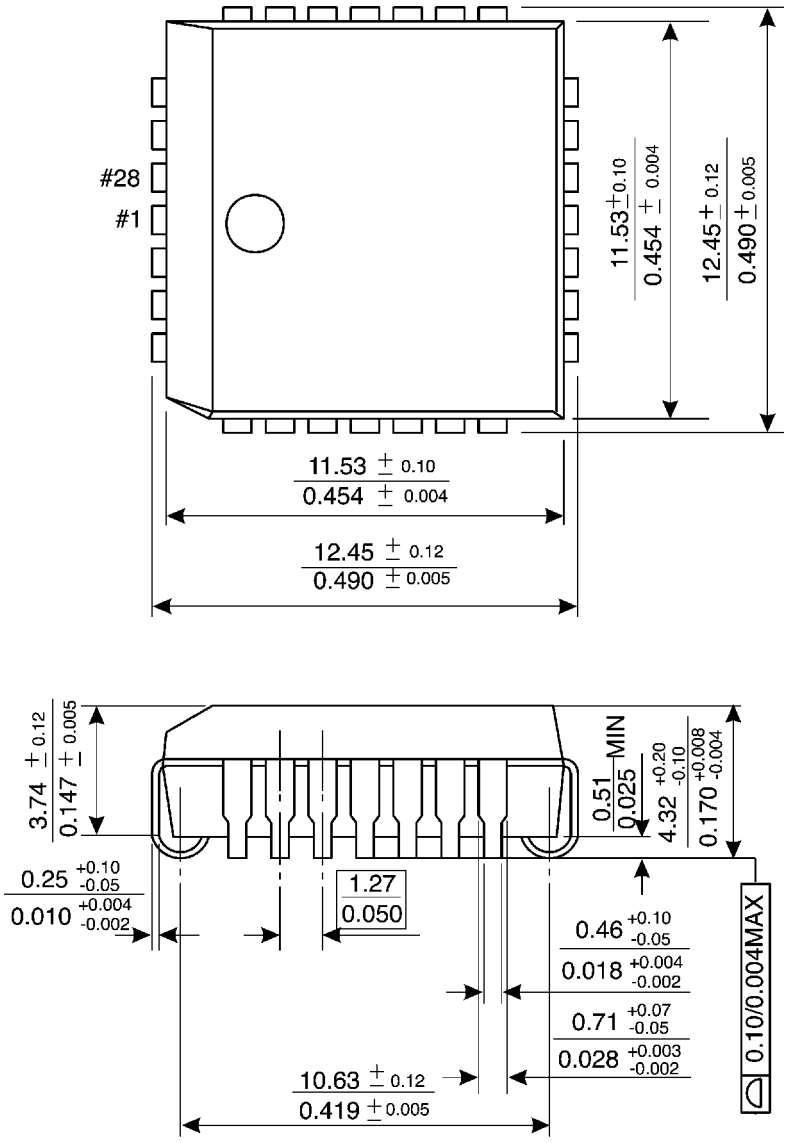
1. Voltages are with respect to ground (GND) unless otherwise stated.
2. Supply voltage and operation temperature are as per Recommended Operating Conditions.
3. Timing parameters are as per AC Electrical Characteristics - Voltage Levels for Timing Parameter Measurement.

Test Conditions:

1. Normal State selected.
2. Auto-Holdover State.
3. Freerun State selected.
4. 8kHz frequency source selected.
5. 1.544MHz frequency source selected.
6. 2.048MHz frequency source selected.
7. Master clock input OSCi at 20MHz ±0ppm.
8. Master clock input OSCi at 20MHz ±32ppm.
9. Master clock input OSCi at 20MHz ±100ppm.
10. Reference input at ±0ppm.
11. Reference input at ±32ppm.
12. Reference input at ±100ppm.
13. For Freerun State of ±0ppm.
14. For Freerun State of ±32ppm.
15. For Freerun State of ±100ppm.
16. For capture range of ±230ppm.
17. For capture range of ±198ppm.
18. For capture range of ±130ppm.
19. 25pF capacitive load.
20. OSCi Master Clock Jitter is less than 2ns p-p, or 0.04UI p-p where 1UI p-p = 1/20MHz.
21. Jitter on reference input is less than 7ns p-p.
22. Applied jitter is sinusoidal.
23. Minimum applied input jitter magnitude to regain synchronization.
24. Loss of synchronization is obtained at slightly higher input jitter amplitudes.
25. Within 10 ms of the state or input change
26. 1UIpp = 125µs for 8kHz signals.
27. 1UIpp = 648ns for 1.544MHz signals.
28. 1UIpp = 488ns for 2.048MHz signals.
29. 1UIpp = 323ns for 3.088MHz signals.
30. 1UIpp = 244ns for 4.096MHz signals.
31. 1UIpp = 122ns for 8.192MHz signals.
32. 1UIpp = 61ns for 16.384MHz signals.
33. No filter.
34. 40Hz to 100kHz bandpass filter.
35. With respect to reference input signal frequency.
36. After a $\overline{RST}$.
37. Master clock duty cycle 40% to 60%.
38. Prior to Auto-Holdover State, device was in Normal State and phase-locked.

Mechanical Specifications

Figure 11. 28-pin PLCC



Dimensions in Millimeters/Inches

Ordering Information

Table 20. Ordering Information

Part Number	Package
PT7A4401CJ	28-Pin PLCC

Notes

Pericom Technology Inc.

Email: support@pti.com.cn Web-Site: www.pti.com.cn, www.pti-ic.com

China: No. 20 Building, 3/F, 481 Guiping Road, Shanghai, 200233, China
Tel: (86)-21-6485 0576 Fax: (86)-21-6485 2181

Asia Pacific: Unit 1517, 15/F, Chevalier Commercial Centre, 8 Wang Hoi Rd, Kowloon Bay, Hongkong
Tel: (852)-2243 3660 Fax: (852)- 2243 3667

U.S.A.: 2380 Bering Drive, San Jose, California 95131, USA
Tel: (1)-408-435 0800 Fax: (1)-408-435 1100