

SPICE Device Model SUM110N08-07L Vishay Siliconix

N-Channel 75-V (D-S), 175°C MOSFET

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

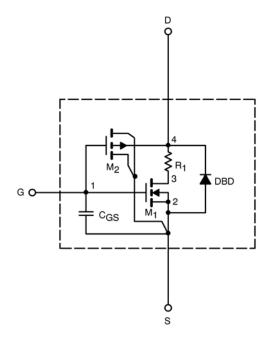
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125° C temperature ranges under the pulsed 0 to 10V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Conditions	Simulated Data	Measured Data	Unit
Static	<u> </u>		<u>, </u>		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.1		V
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	865		Α
Drain-Source On-State Resistance ^a		V_{GS} = 10 V, I_D = 30 A	0.0056	0.0055	Ω
		V_{GS} = 10 V, I_{D} = 30 A, T_{J} = 125°C	0.0089		
	r _{DS(on)}	V_{GS} = 10 V, I_{D} = 30 A, T_{J} = 175°C	0.011		
		V_{GS} = 4.5 V, I_{D} = 20 A	0.0076	0.0075	
Forward Voltage ^a	V_{SD}	I _F = 110 A, V _{GS} = 0 V	0.93	1	V
Dynamic ^b					
Input Capacitance	C _{iss}	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$	4700	4420	pF
Output Capacitance	Coss		678	700	
Reverse Transfer Capacitance	C _{rss}		330	310	
Total Gate Charge ^c	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_{D} = 110 A	82	81	nC
Gate-Source Charge ^c	Q_{gs}		20	20	
Gate-Drain Charge ^c	Q_{gd}		20	20	
Turn-On Delay Time ^c	t _{d(on)}	$V_{DD} = 30 \text{ V, } R_L = 0.47 \ \Omega$ $I_D \cong \ 110 \text{ A, } V_{GEN} = 10 \text{ V, } R_G = 2.5 \ \Omega$ $I_F = 110 \text{ A, } di/dt = 100 \text{ A/}\mu\text{s}$	19	15	ns
Rise Time ^c	t _r		12	20	
Turn-Off Delay Time ^c	$t_{d(off)}$		18	40	
Fall Time ^c	t _f		16	15	
Source-Drain Reverse Recovery Time	t _{rr}		31	55	

Notes

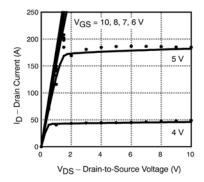
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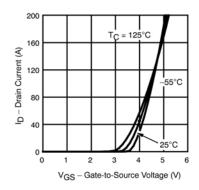
Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2%. Guaranteed by design, not subject to production testing. Independent of operating temperature.

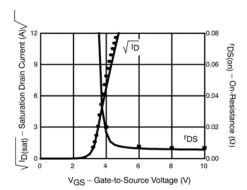


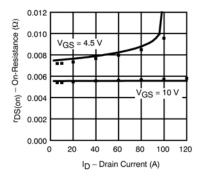
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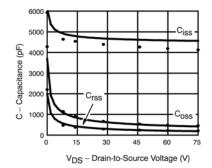
COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)

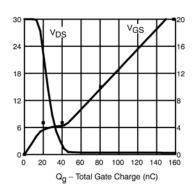












Note: Dots and squares represent measured data.