

MOS FIELD EFFECT TRANSISTOR 2SK3221

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK3221 is N channel DMOS FET device that features a low gate charge and excellent switching characteristics, and designed for high voltage applications such as switching power supply, AC adapter.

ORDERING INFORMATION

Part number	Package		
2SK3221	Isolated TO-220		

FEATURES

•Low gate charge $Q_G = 9 \text{ nC TYP}$. (VDD = 450 V, VGS = 10 V, ID = 2.0 A) •Gate voltage rating $\pm 30 \text{ V}$ •Low oN-state resistance $R_{DS(on)} = 4.4 \Omega$ (MAX.) (VGS = 10 V, ID = 1.0 A) •Avalanche capability ratings •Isolated TO-220 package

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to source voltage (V _{GS} = 0 V)	Vdss	600	V
Gate to source voltage (VDs = 0 V)	Vgss	±30	V
Drain current(DC) (Tc = 25°C)	ID(DC)	±2.0	А
Drain current(pulse) Note1	D(pulse)	±8.0	А
Total power dissipation (T _A = 25°C)	P _{T1}	2.0	W
Total power dissipation (Tc = 25°C)	PT2	25	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C
Single avalanche current ^{Note2}	IAS	2.0	А
Single avalanche energy ^{Note2}	EAS	2.7	mJ
Diode recovery dv/dt ^{Note3}	dv/dt	3.5	V/ns

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

- **2.** Starting T_{ch} = 25°C, V_{DD} = 150 V, R_G = 25 Ω , V_{GS} = 20 V \rightarrow 0 V
- 3. IF \leq 1.0 A, V_{clamp} = 600 V, di/dt \leq 100 A/ μ s, T_A = 25°C

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

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ELECTRICAL CHARACTERISTICS(T_A = 25°C)

Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain leakage current	ldss	Vds = 600 V, Vgs = 0 V			100	μA
Gate leakage current	lgss	$V_{GS} = \pm 30 \text{ V}, \text{ Vds} = 0 \text{ V}$			±10	μA
Gate cut-off voltage	VGS(off)	Vds = 10 V, Id = 1 mA	2.5		3.5	V
Forward transfer admittance	y _{fs}	Vds = 10 V, Id = 1.0 A	0.5			S
Drain to source on-state resistance	RDS(on)	Vgs = 10 V, Id = 1.0 A		3.3	4.4	Ω
Input capacitance	Ciss	VDS = 10 V		290		pF
Output capacitance	Coss	Vgs = 0 V		60		pF
Reverse transfer capacitance	Crss	f = 1 MHz		5		pF
Turn-on delay time	td(on)	VDD = 150 V, ID = 1.0 A		7		ns
Rise time	tr	VGS(on) = 10 V		2		ns
Turn-off delay time	td(off)	Rg = 10 Ω		20		ns
Fall time	tr			10		ns
Total gate charge	QG	Vdd = 450 V		9		nC
Gate to source charge	QGS	Vgs = 10 V		2.4		nC
Gate to drain charge	Qgd	ID = 2.0 A		2		nC
Diode forward voltage	VF(S-D)	IF = 2.0 A, VGS = 0 V		0.9		V
Reverse recovery time	Trr	IF = 2.0 A, VGS = 0 V		0.9		μs
Reverse recovery charge	Qrr	di/dt = 50 A/µs		2.0		μC

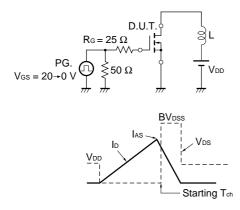
Test circuit 1 Avalanche capability

Test circuit 2 Switching time

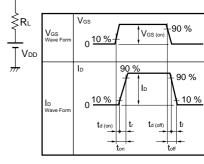
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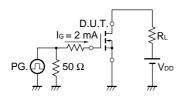
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Rg PG.(___) $R_G = 10 \Omega$ Vgs 0 τ τ=1*μ*s Duty Cycle ≦ 1 %



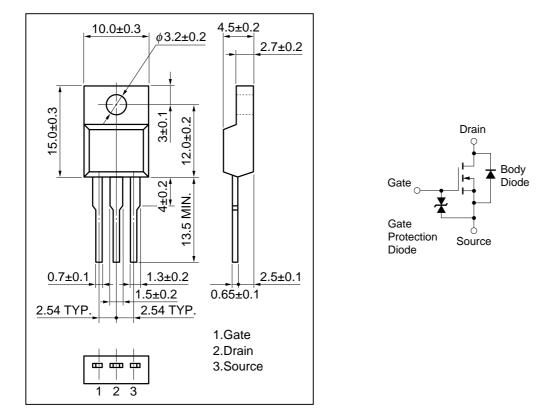
Test circuit 3 Gate charge



Preliminary Product Information

Package Drawing(Unit : mm)

Isolated TO-220 (MP-45F)



The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Anti-radioactive design is not implemented in this product.

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