ALPHA SEMICONDUCTOR
Excellence in Analog Power Products

AS3842/3843/3844/3845

Current Mode Controller

FEATURES

- 2.5V Bandgap Reference Trimmed to 1% and Temperature Compensated
- AS3842/3 Oscillators Trimmed for Precision Duty Cycle Clamp
- Improved Specs on ULVO and Hysteresis Provide More Predictable Start up and Shut-down
- Improved 5V Regulator Provides Better AC Noise Immunity
- Pin-to-Pin Compatible with UC3842/43/44/45
- Guaranteed Performance with I_{SENSE} Pulled Below Ground
- Over-Temperature Shutdown
- Current Mode Operation to 500kHz
- Low Start-up and Operating Current

APPLICATIONS

- Current-Mode, Off-Line, Switched-Mode Power Supplies
- Current-Mode, DC-to-DC Converters
- Step-Down "Buck" Regulators
- Step-Down "Boost" Regulators
- Flyback, Isolated Regulators
- Forward Converters
- Synchronous FET Converters

PRODUCT DESCRIPTION

The Alpha Semiconductor AS3842/3/4/5 family of control IC's are fixed frequency current mode pulse width modulation controllers. They provide all the features necessary to implement off-line or DC-to-DC converter applications with a minimal number of external components. These circuits include a precision bandgap reference trimmed for 1% accuracy at the error amp input, a trimmed oscillator discharge current for precise maximum duty control, a high gain error amplifier, a PWM comparator providing cycle-by-cycle current limit control and a high current totem pole output for driving power MOSFETs.

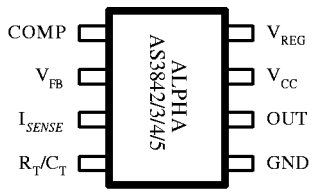
The AS3842 and AS3844 have under-voltage lockout thresholds of 16V (on) and 10V (off), making them ideal for off-line applications. The AS3843 and AS3845 have UVLO thresholds of 8.4V (on) and 7.6V (off), and require less than 0.5mA of startup current. The AS3842 and AS3843 operates at duty cycles near 100%. The AS3844/45 have a maximum duty cycle range from 0% to 50%, due to an internal flip-flop that blanks the output at every other clock cycle.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
AS3842/3/4/5N	8-Pin Plastic DIP	0°C to 105°C
AS3842/3/4/5D-8	8-Pin Plastic SOIC	0°C to 105°C

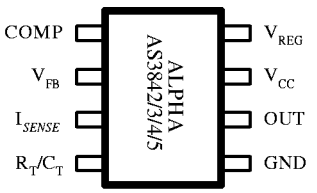
Pin Connections

PDIP (N)



Top View

µSOIC ™ (D)



Top View

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (I_{CC} < 30 mA) ..... Self-Limiting
Supply Voltage (Low Impedance Source)..... 30V
Output Current ..... ±1A
Output Energy (Capacitive Load)..... 5µJ
Analog Inputs (Pin 2, Pin 3) ..... -0.3 to +30V
Error Amp Sink Current..... 10mA

Maximum Power Dissipation
8L SOIC 750mW
8L PDIP 1000mW
14L SOIC 950mW
Maximum Junction Temperature ..... 150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature, Soldering 10 Seconds ..... 300°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED CONDITION

PARAMETER	SYMBOL	RATING	UNIT
SUPPLY VOLTAGE	V_{CC}		
AS3842, AS3844		15	V
AS3843, AS3845		10	V
OSCILLATOR	f_{OSC}	50 to 500	kHz

TYPICAL THERMAL RESISTANCES

PACKAGE	θ_{JA}	θ_{JC}	TYPICAL DERATING
8L PDIP	95° C/W	50° C/W	10.5 mW/°C
8L SOIC	175° C/W	45° C/W	5.7 mW/°C
14L SOIC	130° C/W	35° C/W	7.7 mW/°C

ELECTRICAL CHARACTERISTICS

Electrical characteristics are guaranteed over full junction temperature range (0 to 70°C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are V_{CC} = 15V, R_T = 10kΩ, and C_T = 3.3nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Test Conditions	Typ	Min	Max	Units
5 V Regulator					
Output Voltage	T_J = 25°C, I_{REG} = 1mA	5.00	4.95	5.05	V
Line Regulation	12 ≤ V_{CC} ≤ 25V	2		10	mV
Load Regulation	1 ≤ 1_{REG} ≤ 20 mA	2		10	mV
Temperature Stability[1]		0.2		0.4	mV/°C
Total Output Variation[1]	Line, load, temperature		4.85	5.15	V
Long-Term Stability[1]	Over 1,000 hours at 25°C	5		25	mV
Output Noise Voltage	10 Hz ≤ f ≤ 100kHz, T_J = 25°C	50			µV
Short Circuit Current		100	30	180	mA
2.5 V Internal Reference					
Nominal Voltage	T = 25°C, I_{REG} = 1mA	2.500	2.475	2.525	V
Line Regulation	12 ≤ V_{CC} ≤ 25V	2		5	mV
Load Regulation	1 ≤ 1_{REG} ≤ 20 mA	2		5	mV
Temperature Stability[1]		0.1		0.2	mV/°C
Total Output Variation[1]	Line, load, temperature	2.500	2.450	2.550	V
Long-Term Stability[1]	Over 1,000 hours at 25°C	2		12	mV
Oscillator					
Initial Accuracy	T_J = 25°C	52	47	57	kHz
Voltage Stability	12V ≤ V_{CC} ≤ 25V	0.2		1	%
Temperature Stability[1]	T_{MIN} ≤ T_J ≤ T_{MAX}	5			%
Amplitude	$V_{RT/CT}$ peak-to-peak	1.6			V
Upper Trip Point		2.9			V
Lower Trip Point		1.3			V
Discharge Current		8.7	7.5	9.5	mA
Duty Cycle Limit	R_T = 680 Ω, C_T = 5.3 nF, T_J = 25°C	50	46	52	%

ELECTRICAL CHARACTERISTICS (cont'd)

Electrical characteristics are guaranteed over full junction temperature range (0 to 70°C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are V_{CC} = 15V, R_T = 10kΩ, and C_T = 3.3nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Test Conditions	Typ	Min	Max	Units
Error Amplifier					
Input Voltage	T_J = 25°C	2.50	2.475	2.525	V
Input Bias Current		-0.1		-1	µA
Voltage Gain	2 ≤ V_{COMP} ≤ 4V	90	65	1	dB
Transconductance		1			mA/mV
Unity Gain Bandwidth[1]		1.2	0.8		MHz
Power Supply Rejection Ratio	12 ≤ V_{CC} ≤ 25V	70	60		dB
Output Sink Current	V_{FB} = 2.3 V, V_{COMP} = 1.1V	6	2		mA
Output Source Current	V_{FB} = 2.3 V, V_{COMP} = 5V	0.8	0.5		mA
Output Swing High	V_{FB} = 2.7 V, R_L = 15 kΩ to Ground	5.5	5		V
Output Swing Low	V_{FB} = 2.7 V, R_L = 15 kΩ to Pin 8	0.7		1.1	V
Current Sense Comparator					
Transfer Gain[2,3]	-0.2 ≤ V_{SENSE} ≤ 0.8V	3.0	2.85	3.15	V/V
I_{SENSE} Level Shift[2]	V_{SENSE} = 0V	1.5			V
Maximum Input Signal[2]	V_{COMP} = 5V	1	0.9	1.1	V
Power Supply Rejection Ratio	12 ≤ V_{CC} ≤ 25V	70			dB
Input Bias Current		-1		-10	µA
Propagation Delay to Output[1]		150		300	ns
Output					
Output Low Level	I_{SINK} = 20 mA	0.1		0.4	V
	I_{SINK} = 200 mA	1.5		2.2	V
Output High Level	I_{SOURCE} = 20 mA	13.5	13		V
	I_{SOURCE} = 200 mA	13.5	12		V
Rise Time[1]	C_L = 1 nF	50		150	ns
Fall Time[1]	C_L = 1 nF	50		150	ns
Housekeeping					
Start-up Threshold	3842/4	16	15	17	V
	3843/5	8.4	7.8	9.0	V
Minimum Operating Voltage After Turn On	3842/4	10	9	11	V
	3843/5	7.6	7.0	8.2	V
Output Low Level in UV State	I_{SINK} = 20 mA, V_{CC} = 6 V	1.5		2.0	V
Over-Temperature Shutdown[4]		125			°C
PWM					
Maximum Duty Cycle	3842/3	97	94	100	%
Minimum Duty Cycle	3842/3			0	%
Maximum Duty Cycle	3844/5	49.5	49	50	%
Minimum Duty Cycle	3844/5			0	%
Supply Current					
Start-up Current	3842/4, V_{FB} = V_{SENSE} = 0V, V_{CC} = 14V	0.5		1.0	mA
	3843/5, V_{FB} = V_{SENSE} = 0V, V_{CC} = 7V	0.3		0.5	mA
Operating Supply Current		9		17	mA
V_{CC} Zener Voltage	I_{CC} - 25 mA	30			V

Notes:

1. This parameter is not 100% tested in production.
2. Parameter measured at trip point of PWM latch.
3. Transfer gain is the relationship between current sense input and corresponding error amplifier output at the PWM latch trip point and is mathematically expressed as follows:

$$A = \frac{\Delta I_{COMP};\ -0.2 \le V_{SENSE} \le 0.8V}{\Delta V_{SENSE}}$$

4. At the over-temperature threshold, TOT, the oscillator is disabled. The 5V reference and the PWM stages, including the PWM latch, remain powered.

APPLICATION INFORMATION

Section 1 - Theory of Operation

The AS3842/3/4/5 family of current-mode control ICs are low cost, high performance controllers which are pin compatible with the industry standard UC3842 series of devices. Suitable for many switch mode power supply applications, these ICs have been optimized for use in high frequency off-line ad DC-to-DC converters. The AS3842 has been enhanced to provide significantly improved performance, resulting in exceptionally better tolerances in power supply manufacturing. In addition, all electrical characteristics are guaranteed over the full 0 to 105°C temperature range. Among the many enhancements are: a precision trimmed 2.5 volt reference (+/- 1% of nominal at the error amplifier input), a significantly reduced propagation delay from current sense input to the IC output, a trimmed oscillator for precise duty-cycle clamping, a modified flip-flop scheme that gives a true 50% duty ratio clamp on 3844/45 types, and an improved 5V regulator for better AC noise immunity. Furthermore, the AS3842 provides guaranteed performance with current sense input below ground. The advanced oscillator design greatly simplifies synchronization. The device is more completely specified to guarantee all parameters that impact power supply manufacturing tolerances.

The functional block diagram of the AS3842 is shown in Figure 1. The IC is comprised of the six basic functions necessary to implement current mode control; the under-voltage lockout; the reference; the oscillator, the error amplifier; the current sense comparator/PWM latch; and the output. The following paragraphs will describe the theory of operation of each of the functional blocks.

1.1 Under-voltage lockout (UVLO)

The under-voltage lockout function of the AS3842 holds the IC in a low quiescent current (1 mA) "standby" mode until the supply voltage (V_{CC}) exceeds the upper UVLO threshold voltage. This guarantees that all of the ICs internal circuitry are properly biased and fully functional before the output stage is enabled. Once the IC turns on, the UVLO threshold shifts to a lower level (hysteresis) to prevent V_{CC} oscillations.

The low quiescent current standby mode of the AS3842 allows "bootstrapping" ---a technique used in off-line converters to start the IC from the rectified AC line voltage initially, after which power to the IC is provided by an auxiliary winding off the power supply's main transformer. Figure 14 shows a typical bootstrap circuit where capacitor (C) is charged via resistor (R) from the rectified AC line. When the voltage on the capacitor (V_{CC}) reaches the upper UVLO threshold, the IC (and hence, the power supply) turns on the voltage on C begins to quickly discharge due to the increased operating current. During this time, the auxiliary winding begins to supply the current necessary to run the IC. The capacitor must be sufficiently large to maintain a voltage greater than the lower UVLO threshold during start up. The value of R must be selected to provide greater than 1 mA of current at the minimum DC bus voltage (R < VDCmin/1 mA).

The UVLO feature of the AS3842 has significant advantages over standard 3842 devices. First, the UVLO thresholds are based on a temperature compensated band gap reference rather than conventional zeners. Second, the UVLO disables the

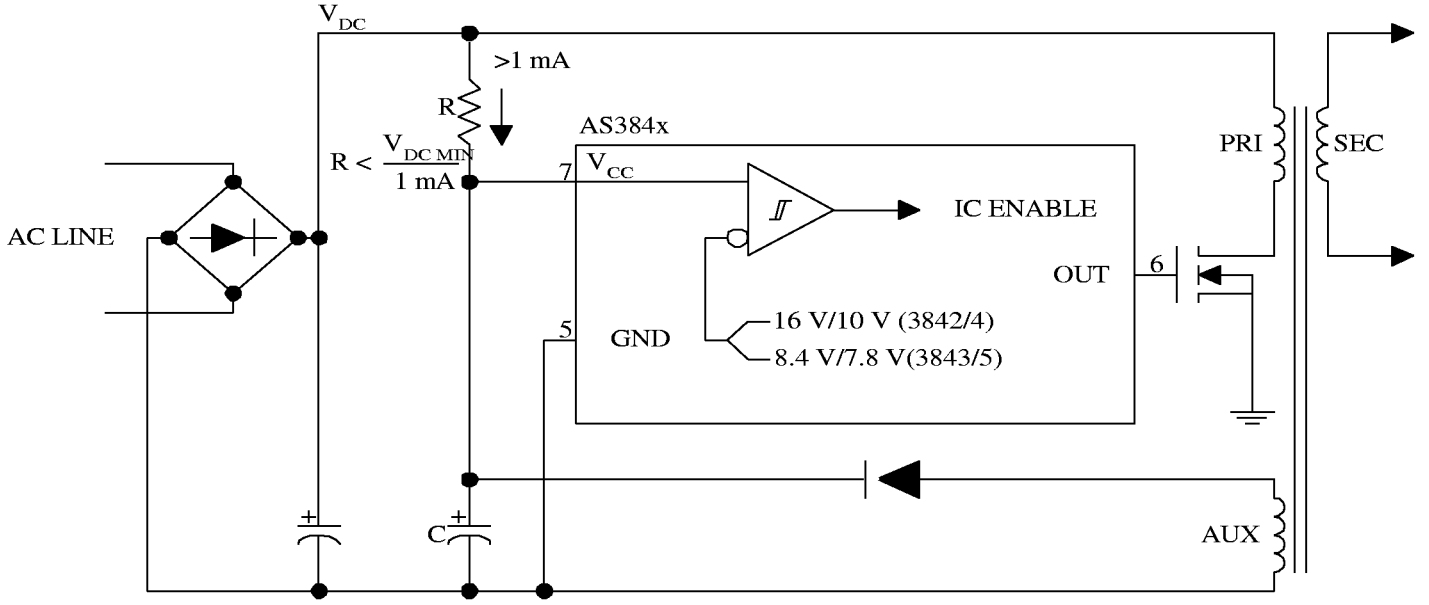


Figure 14. Boostrap Circuit

output at power down, offering additional protection in cases where V_{REG} is heavily decoupled. The UVLO on some 3842 devices shuts down the 5 volt regulator only, which results in eventual power down of the output only after the 5 volt rail collapses. This can lead to unwanted stresses on the switching devices during power down. The AS3842 has tow separate comparators which monitor both V_{CC} and V_{REF} and hold the output low if either are not within specification.

The AS3842 family offers two different UVLO options. The AS3842/4 has UVLO thresholds of 16 volts (on) and 10 volts (off). The AS3843/5 has UVLO levels of 8.4 volts (on) and 7.6 volts (off).

1.2 Reference (V_{REG} and V_{FB})
The AS3842 effectively has two precise band gap based temperature compensated voltage reference. Most obvious is the VREG pin (pin 8) which is the output of a series pass regulator. This 5.0 V output is normally used to provide charging current to the oscillator's timing capacitor (Section 1.3). In addition, there is a trimmed internal 2.5 V reference which is connected to the non-inverting (+) input of the error amplifier. The tolerance of the internal reference is $\pm$ 1% over the full specified temperature range, and $\pm$ 1% for V_{REG}.

The reference section of the AS3842 is greatly improved over the standard 3842 in a number of ways. For example, in a closed loop system, the voltage at the error amplifier's inverting input (V_{FB}, pin 1) is forced by the loop to match the voltage at the non-inverting input. Thus, V_{FB} is the voltage which sets the accuracy of the entire system. The 2.5 V reference of the AS3842 is tightly trimmed for precision at V_{FB}, including errors caused by the op amp, and is specified over temperature. This method of trim provides a precise reference voltage for the error amplifier while maintaining the original 5 V regulator specifications. In addition, force/sense (Kelvin) bonding to the package pin is utilized to further improve the 5 V load regulation. Standard 3842's, on the other hand, specify tight regulation for the 5 V output only and rate in over line, load and temperature. The voltage at V_{FB}, which is of critical importance, is loosely specified and only at 25°C.

The reference section, in addition to providing a precise DC reference voltage, also powers most of the IC's internal circuitry. Switching noise, therefore, can be internally coupled onto the reference. With this in mind, all of the logic within the AS3842 was designed with ECL type circuitry which generates less switching noise because it runs at essentially constant current regardless of logic state. This, together with improved AC noise rejection, results in substantially less switching noise on the 5 V output.

The reference output is short circuit protected and can safely deliver more that 20 mA to power external circuitry

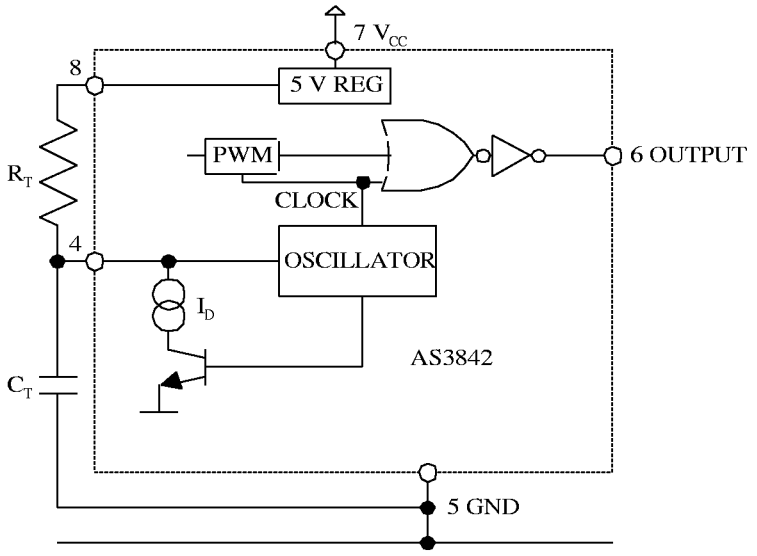
1.3 Oscillator
The newly designed oscillator of the AS3842 is enhanced to give significantly improved performance. These enhancements are discussed in the following paragraphs. The basic operation of the oscillator is as follows:

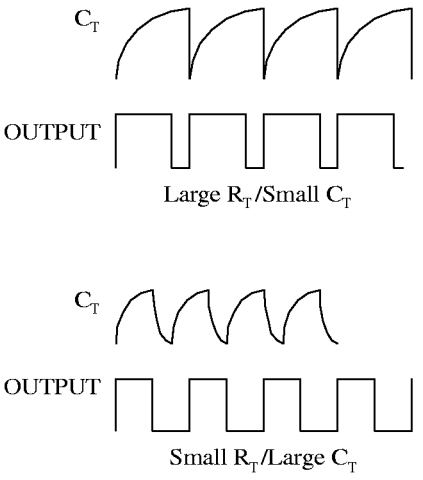
A simple RC network is used to program the frequency and the maximum duty ratio of the AS3842 output. See Figure 15. timing capacitor (C_T) is charged through timing resistor (R_T) from the fixed 5.0 V at V_{REG}. During the charging time, the OUT (pin 6) is high. Assuming that the output is not terminated by the PM latch, when the voltage across C_T reaches the upper oscillator trip point (3.0 V), an internal current sink from pin 4 to ground is turned on and discharges C_T towards the lower trip point. During this discharge time, an internal clock pulse blanks the output to its low state. When the voltage across C_T reaches the lower trip point (1.3 V), the current sink is turned off, the output goes high, and the cycle repeats. Since the output is blanked during the discharge of C_T, it is the discharge time which controls the output deadtime and hence, the maximum duty ratio.

The nature of the AS3842 oscillator circuit is such that, for a given frequency, many combinations of R_T and C_T are possible. However, only one value of R_T will yield the desired maximum duty ratio at a given frequency. Since a precise maximum duty ratio clamp is critical for many power supply designs, the oscillator discharge current is trimmed in a unique manner which provides significantly improved tolerances as explained later in this section. In addition, the AS3844/5 options have an internal flip-flop which effectively blanks every other output pulse (the oscillator runs at twice the output frequency), providing and absolute maximum 50% duty ratio regardless of discharge time.

1.3.1 Selecting timing components R_T and C_T
The values of R_T and C_T can be determined mathematically by the following expressions:

$$C_T = \frac{D}{R_T\, f_{OSC} \ln\left(\frac{K_L}{K_H}\right)} = \frac{1.63D}{R_T\, f_{OSC}} \qquad (1)$$





$$C_T = \frac{D}{R_T\, f_{OSC} \ln\left(\frac{K_L}{K_H}\right)} = \frac{1.63D}{R_T\, f_{OSC}} \quad (1)$$

$$R_T = \frac{V_{REG}}{I_D} \cdot \frac{(K_L)^{\frac{1}{D}} - (K_H)^{\frac{1}{D}}}{(K_L)^{\frac{1-D}{D}} - (K_H)^{\frac{1-D}{D}}} \quad (2)$$

$$= 582 \cdot \frac{(0.736)^{\frac{1}{D}} - (0.432)^{\frac{1}{D}}}{(0.736)^{\frac{1-D}{D}} - (0.432)^{\frac{1-D}{D}}}$$

$$K_L = \frac{V_{REG} - V_L}{V_{REG}} \approx 0.736 \quad (3)$$

$$K_H = \frac{V_{REG} - V_H}{V_H} \approx 0.736 \quad (4)$$

where f_{OSC} is the oscillator frequency, D is the maximum duty ratio, V_H is the oscillator's upper trip point, V_L is the lower trip point, V_R is the reference voltage, I_D is the discharge current.

Table 1 lists some common values of R_T and the corresponding maximum duty ratio. To select the timing components; first, use Table 1 or equation (2) to determine the value of R_T that will yield the desired maximum duty ratio. Then, use equation (1) to calculate the value of C_T. For example, for a switching frequency of 250 kHz and a maximum duty ratio of 50%, the value of R_T, from Table 1, is 683. Applying this value to equation (1) and solving for C_T gives a value of 4700 pF. In practice, some fine tuning of the initial values may be necessary during design. However, due to the advanced design of the AS3842 oscillator, once the final values are determined, they will yield repeatable results, thus eliminating the need for additional trimming of the timing components during manufacturing.

1.3.2 Oscillator Enhancements

The AS3842 oscillator is trimmed to provide guaranteed duty ratio clamping. This means that the discharge current (I_D) is trimmed to a value that compensates for all of the tolerances within the device (such as the tolerances of V_{REG}, propagation delays, the oscillator trip points, etc.) which have an effect on the frequency and maximum duty ratio. For example, if the combined tolerances of a particular device are 0.5% above nominal, the I_D is trimmed to 0.5% above nominal. This method of trimming virtually eliminates the need to trim external oscillator components during power supply manufacturing. Standard 3842 devices specify or trim only for a specific value of discharge current. This makes precise and repeatable duty ratio clamping virtually impossible due to other IC tolerances. The AS3844/5 provides true 50% duty ratio clamping by virtue of excluding from its flip-flop scheme, the normal output blanking associated with the discharge of C_T. Standard 3844/5 devices include the output blanking associated with the discharge of C_T, resulting in somewhat less than a 50% duty ratio.

Table 1. R_T vs. Maximum Duty Ratio

R_T (Ω)	Dmax
470	22%
560	37%
683	50%
750	54%
820	58%
910	63%
1,000	66%
1,200	72%
1,500	77%
1,800	81%
2,200	85%
2,700	88%
3,300	90%
3,900	91%
4,700	93%
5,600	94%
6,800	95%
8,200	96%
10,000	97%
18,000	98%

1.3.3 Synchronization

The advanced design of the AS3842 oscillator simplifies synchronizing the frequency of two or more devices to each other or to an external clock. The R_T/C_T doubles as a synchronization input which can easily be driven from any open collector logic output. Figure 16 shows some simple circuits for implementing synchronization.

1.4 Error Amplifier (COMP)

The As3842 error amplifier is a wide bandwidth, internally compensated operational amplifier which provides a high DC open loop gain (90 dB). The input to the amplifier is a PNP differential pair. The non-inverting (+) input is internally connected to the 2.5V reference, and the inverting (-) input is available at pin 2 (V_{FB}). The output of the error amplifier consists of an active pull-down as shown in Figure 17. This type of output stage allows easy implementation of soft start, latched shutdown and reduced current sense clamp functions. It also permits wire "OR-ing" of the error amplifier outputs to several 3842's, or complete bypass of the error amplifier when its output is forced to remain in its "pull-up" condition.

In most typical power supply designs, the converter's output voltage is divided down and monitored at the error amplifier's inverting input, V_{FB}. A simple resistor divider network is used and is scaled such that the voltage at V_{FB} is 2.5 V when the converter's output is at the desired voltage. The voltage at V_{FB} is then compared to the internal 2.5 V reference and any slight difference is amplified by the high gain of the error amplifier. The resulting error amplifier output is level shifted by two diode drops and is then divided by three to provide a 0 to 1 V reference (V_E) to one input of the current sense comparator. The level shifting reduces the input voltage range of the current sense input and prevents the output form going high when the error amplifier output is forced to its low state. An internal clamp limits V_E to 1.0 V. The purpose of the clamp is discussed in Section 1.5.

1.4.1 Loop Compensation

Loop compensation of a power supply is necessary to ensure stability and provide good line/load regulation and dynamic response. It is normally provided by a compensation network connected between the error amplifier's output (COMP) and inverting input as shown in Figure 17. The type of network used depends on the converter topology and in particular, the characteristics of the major functional blocks within the supply - i.e. the error amplifier, the modulator/switching circuit, and the output filter. In general, the network is designed such that the converter's overall gain/phase response approaches that of a single pole with a -20 dB/decade rolloff, crossing unity gain at the highest possible frequency (up to $f_{SW}/4$) for good dynamic response, with adequate phase margin (>45°) to ensure stability.

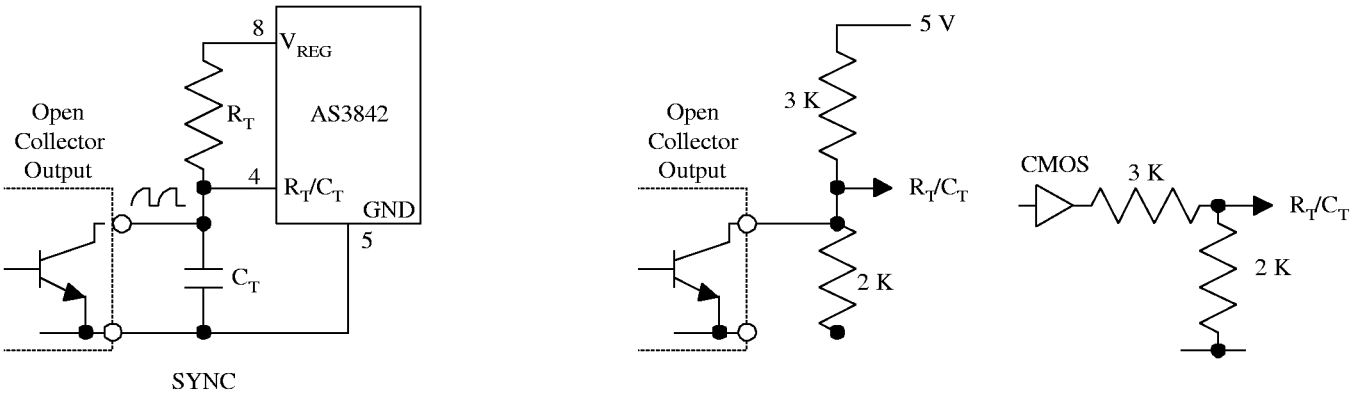


Figure 16.Synchronization

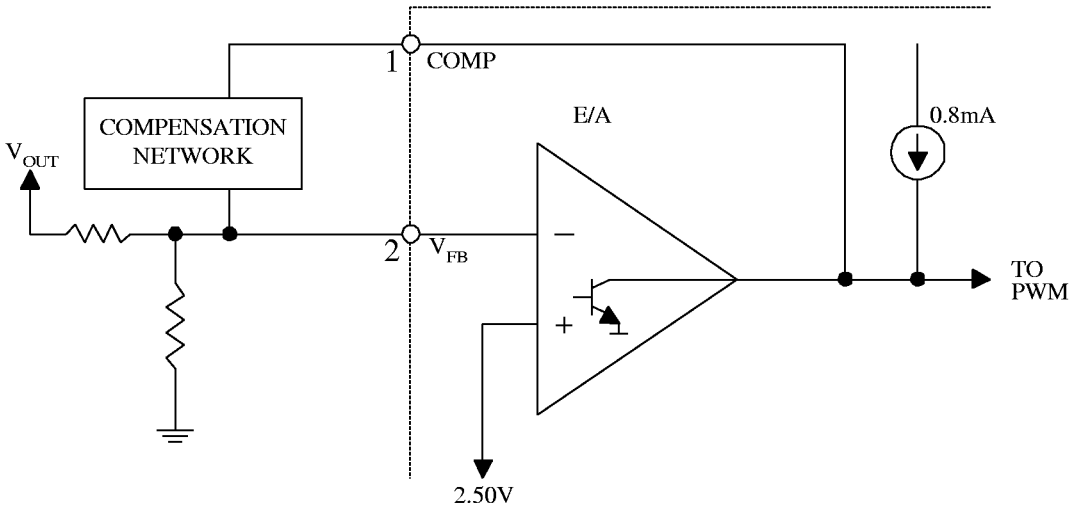


Figure 17. Error Amplifier Compensation

Figure 18 shows the Gain/Phase response of the error amplifier. The unity gain crossing is at 1.2 MHz with approximately 57° C of phase margin. This information is useful in determining the configuration and characteristics required for the compensation network.

One of the simplest types of compensation networks is shown in Figure 19. An RC network provides a single pole which is normally set to compensate for the zero introduced by the output capacitor's ESR. The frequency of the pole (f_P) is determined by the formula:

$$f_P = \frac{1}{2\pi R_f C_f} \qquad (5)$$

Resistors R_1 and R_F set the low frequency gain and should be chosen to provide the highest possible gain, without exceeding the unity gain crossing frequency limit of $f_{SW}/4$. R_{BIAS}, in conjunction with R_1, sets the converter's output voltage; but has no effect on the loop gain/phase response.

There are a few converter design considerations associated with the error amplifier. First, the values of the divider network (R_1 and R_{BIAS}) should be kept low in order to minimize errors caused by the error amplifier's input bias current. An output voltage error equal to the product of the input bias current and the equivalent divider resistance, can be quite significant with divider values greater that 5k. Low divider resistor values also help to improve the noise immunity of the sensitive V_{FB} input.

The second consideration is that the error amplifier will typically source only 0.8 mA; thus, the value of feedback resistance (R_F) should be no lower that 5 KΩ in order to maintain the error amplifier's full output range. In practice, however, the feedback resistance required is usually much greater than 5 KΩ hence this limitation is normally not a problem.

Some power supply topologies may require a more elaborate compensation network. For example, flyback and boost converters operating with continuous current have transfer functions that include a right half plane (RHP) zero. These types of systems require an additional pole elements within the compensation network. A detailed discussion of loop compensation, however, is beyond the scope of this application note.

1.5 I_{SENSE} Current Comparator/PWM Latch

The current sense comparator (sometimes called the PWM comparator) and accompanying latch circuitry make up the pulse width modulator (PWM). It provides pulse-by-pulse current sensing/limiting and generates a variable duty ratio pulse train which controls the output voltage of the power supply. Included is a high speed comparator followed by ECL type logic circuitry which has very low propagation delays and switching noise. This is essential for high frequency power supply designs. The comparator has been designed to provide guaranteed performance with the current sense input below ground. The PWM latch ensures that only one pulse is allowed at the output for each oscillator period.

The inverting input to the current sense comparator is internally connected to the level shifted output of the error amplifier (V_E) as discussed in the previous section. The non-inverting input is the I_{SENSE} input (pin 3). It monitors the switched inductor current of the converter.

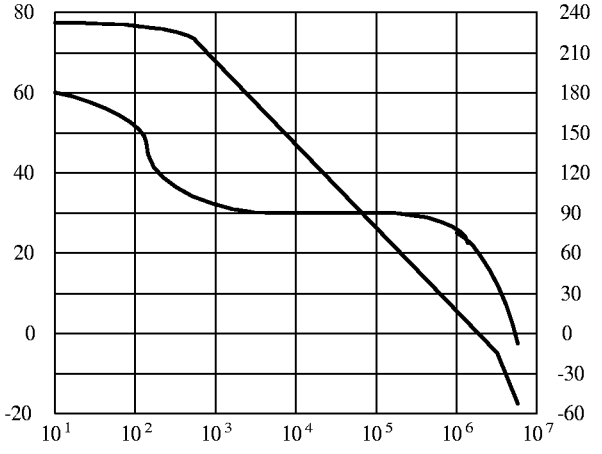


Figure 18. Gain/Phase Response of the AS3842

Figure 20 shows the current sense/PWM circuitry of the AS3842, and associated waveforms. The output is set high by an internal clock pulse and remains high until one of two conditions occur; 1) the oscillator times out (Section 1.3) or 2) the PWM latch is set by the current sense comparator. During the time when the output is high, the converter's switching device is turned on and current flows through resistor R_S. This produces a stepped ramp waveform at pin 3 as shown in Figure 20. The current will continue to ramp up until it reaches the level of V_E at the inverting input. At that point, the comparator's output goes high, setting the PWM latch and the output pulse in then terminated. Thus, V_E is a variable reference for the current sent comparator, and it controls the peak current sensed by R_S on a cycle-by-cycle basis. V_S varies in proportion to changes in the input voltage/current (inner control loop) while V_E varies in proportion to changes in the converters output voltage/current (outer control loop). The two control loops merge at the current sense comparator, producing a variable duty ratio pulse train that controls the output of the converter.

The current sense comparator's inverting input is internally clamped to a level of 1.0V to provide a current limit (or power limit for multiple output supplies) function. The value of RS is selected to produce 1.0 V at the maximum allowed peak inductor current, the RS is selected to equal 1 V/1.5 A = 0.66Ω. In high power applications, power dissipation in the current sense resistor may become intolerable, In such a case, a current transformer can be used to step down the current seen by the sense resistor. See Figure 21.

1.6 Output (OUT)

The output stage of the AS3842 is a high current totem-pole configuration that is well suited for directly driving power MOSFETs. It is capable of sourceing and sinking up to 1 A of peak current. Cross conduction losses in the output stage have

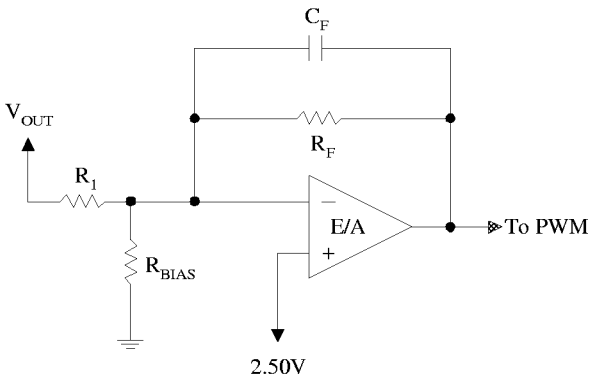


Figure 19. A Typical Compensation Network

been minimized resulting in lower power dissipation in the device. This is particularly important for high frequency operation. During under-voltage shutdown conditions, the output is active low. This eliminates the need for an external pulldown resistor.

1.7 Over-Temperature Shutdown

The AS3842 has a built-in over-temperature shutdown which will limit the die temperature to 130° C typically. When the over-temperature to condition is reached, the oscillator is disabled. All other circuit blocks remain operational. Therefore, when the oscillator stops running, output pulses terminate without losing control of the supply or losing any peripheral functions that may be running off the 5 V regulator. The output may go high during the final cycle, but the PWM latch is still fully operative, and the normal termination of this cycle by the current sense comparator will latch the output low until the over-temperature condition is rectified. Cycling the power will reset the over-temperature disable mechanism, or the chip will re-start after cooling through a nominal hysteresis band.

Section 2 - Design Considerations

2.1 Leading Edge Filter

The current sensed by R_S contains a leading edge spike as shown in Figure 20. This spike is caused by parasitic elements within the circuit including the interwinding capacitance of the power transformer and the recovery characteristics of the rectifier diode (s). The spike, if not properly filtered, can cause stability problems by prematurely terminating the output pulse.

A simple RC filter is used to suppress the spike. The time constant should be chosen such that it approximately equals the duration of the spike. A good choice for R_1 is 1 kΩ, as this value is optimum for the filter and at the same time, it simplifies the determination of R_{SLOPE} (Section 2.2). If the duration of the spike is, for example, 100 ns, then C is determined by:

$$C = \frac{\text{Time Constant}}{1\ \text{k}\Omega} \qquad (6)$$

$$= \frac{100\ \text{ns}}{1\ \text{k}\Omega}$$

$$= 100\ \text{pF}$$

2.2 Slope Compensation

Current-mode controlled converters can experience instabilities or subharmonic oscillations when operated at duty ratios greater than 50%. Two different phenomena can occur as shown graphically in Figure 22.

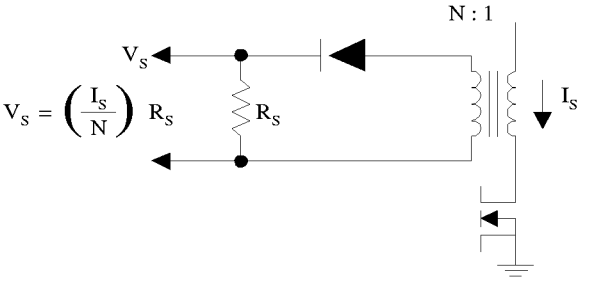


Figure 21. Optional Current Transformer

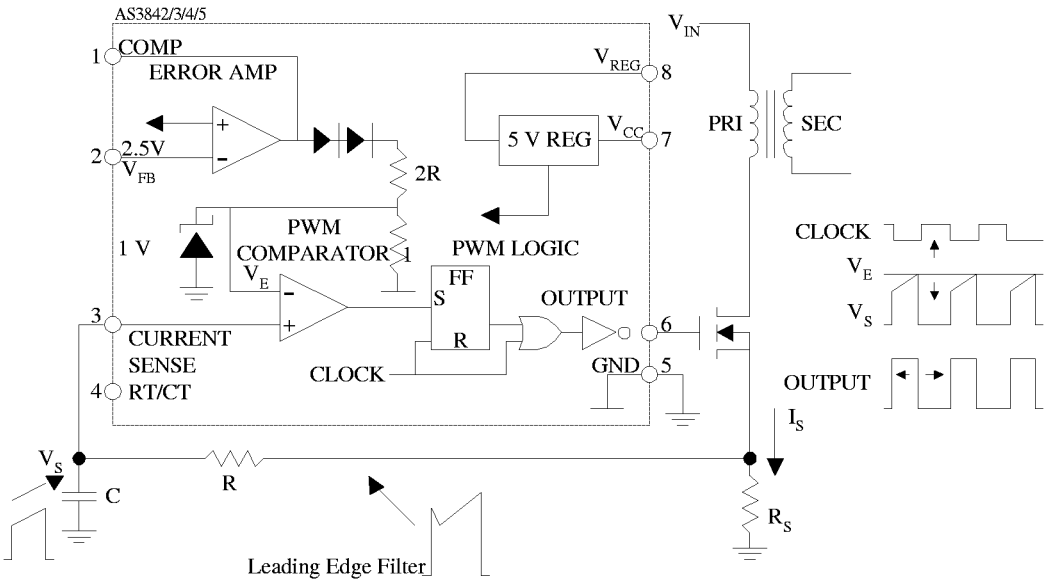


Figure 20. Current Sense/PWN Latch Circuit and Waveforms

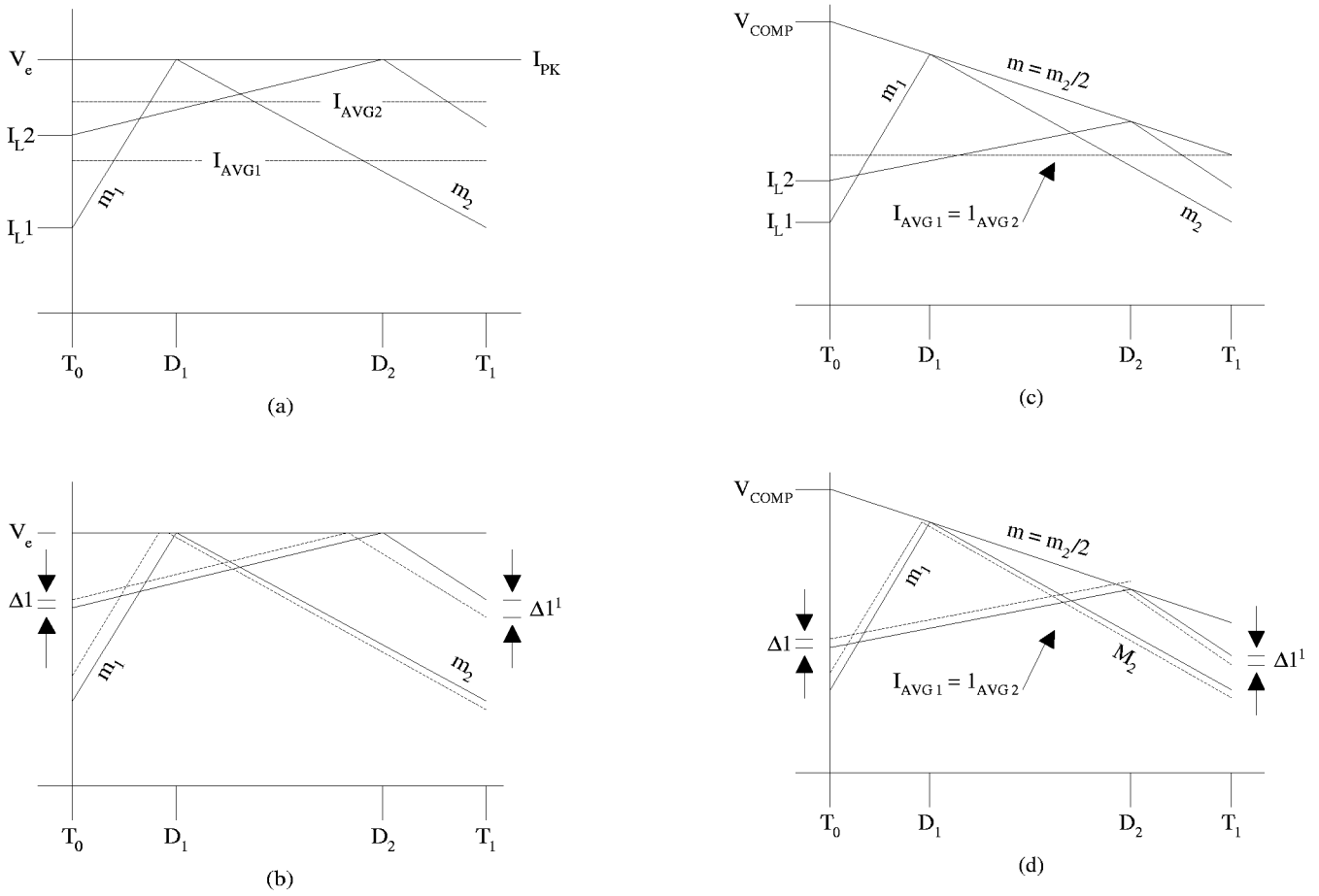


Figure 22. Slope Compensation

First, current-mode controllers detect and control the peak inductor current, where as the converter's output corresponds to the average inductor current. Figure 22(a) clearly shows that the average inductor current (I_1 & I_2) changes as the duty ratio (D_1 & D_2) changes. Note that for a fixed control voltage, the peak current is the same for any duty ratio. The difference between the peak and average currents represents an error which causes the converter to deviate from true current-mode control.

Second, Figure 22(b) depicts how a small perturbation of the inductor current (I) can result in an unstable condition. For duty ratios less than 50 %, the disturbance will quickly converge to a steady state condition. For duty ratios greater than 50%, it progressively increases on each cycle, causing an unstable condition.

Both of these problems are corrected simultaneously by injecting a compensating ramp into either the control voltage (V_E) as shown in figure 22 © & (d), or to the current sense waveform at pin 3. Since V_E is not directly accessible, and, a at pin 4, it is more practical to add the slope compensation to positive ramp waveform is readily available from the oscillator the current waveform. This can be implemented quite simply with the addition of a single resistor, R_{SLOPE}, between pin 4 and pin 3 as shown in Figure 23 (a). R_{SLOPE}, in conjunction with the leading edge filter resistor, R_1 (Section 2.1), forms a divider network which determines the amount of slope added to the waveform. The amount of slope added to the current waveform is inversely proportional to the value of R_{SLOPE}. It has been determined that the amount of slope (m) required is equal to or greater than ½ the downslope (m_2) of the inductor current. Mathematically stated:

$$m \geq \frac{m_2}{2} \qquad (7)$$

In some cases the required value of R_{SLOPE} may be low enough to affect the oscillator circuit and thus cause the frequency to shift. An emitter follower circuit can be used as a buffer for R_{SLOPE} as depicted in Figure 23(b).

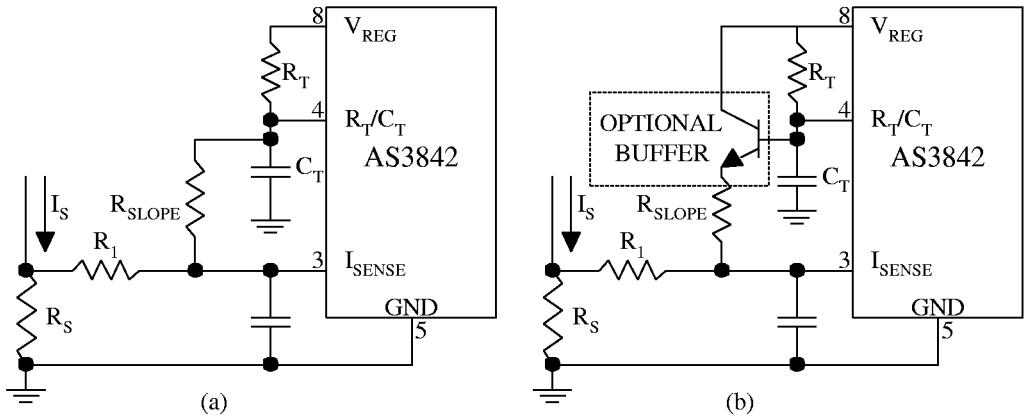


Figure 23. Slope Compensation

Slope compensation can also be used to improve noise immunity in current mode converters operating at less than 50% duty ratio. Power supplies operating under very light load can experience instabilities caused by the low amplitude of the current sense ramp waveform. In such a case, any noise on the waveform can be sufficient to trip the comparator resulting in random and premature pulse termination. The addition of a small amount of artificial ramp (slope compensation) can eliminate such problems without drastically affecting the overall performance of the system.

2.3 Circuit layout and Other Considerations

The electronic noise generated by any switch mode power supply can cause severe stability problems if the circuit is not layed-out (wired) properly. A few simple layout practices will help to minimize noise problems.

When building prototype breadboards, never use plug-in protoboards or wire wrap construction. For best results, do all breadboarding on double sided PCB using ground plane techniques. Keep all traces and lead lengths to a minimum. Avoid large loops and keep the area enclosed within any loops to a minimum. Use common point grounding techniques and separate the power ground traces from the signal ground traces. Locate the control IC and circuitry away from switching devices and magnetics. Also, the timing capacitor's ground connection must be right at pin 5 as shown in Figure 15. These grounding and wiring techniques are very important because the resistance and inductance of the traces are significant enough to generate noise glitches which can disrupt the normal operation of the IC.

Also, to provide a low impedance path for high frequency noise, V_{CC} and V_{REF} should be decoupled to IC ground with 0.1 µF capacitor. Additional decoupling in other sensitive areas may also be necessary. It is very important to locate the decoupling capacitors as close as possible to the circuit being decoupled.