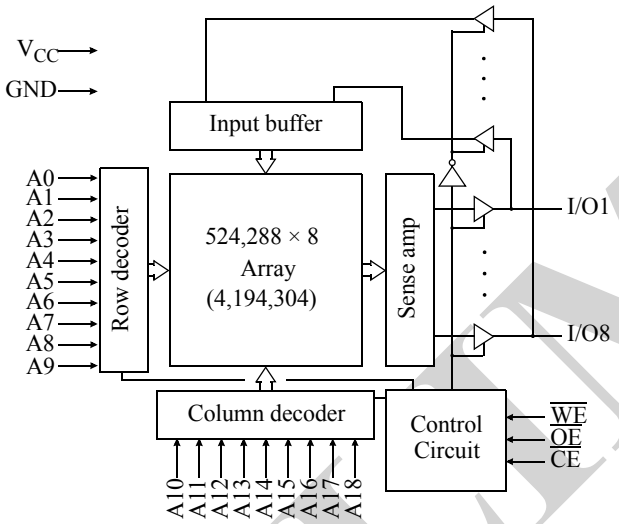
AS7C4096A

5.0V 512K × 8 CMOS SRAM

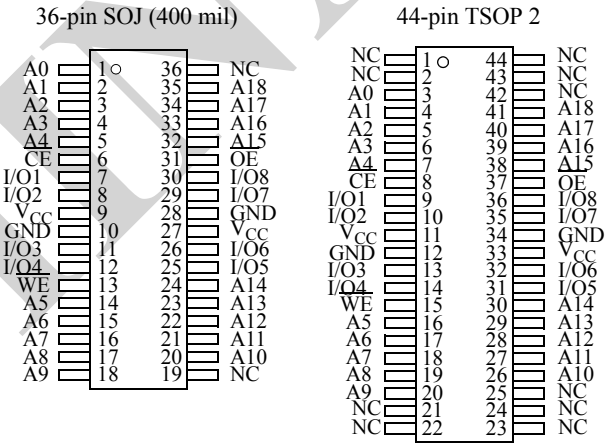
Features

- Pin compatible to AS7C4096
- Industrial and commercial temperature
- Organization: 524,288 words × 8 bits
- Center power and ground pins
- High speed
  - 10/12/15/20 ns address access time
  - 5/6 ns output enable access time
- Low power consumption: ACTIVE
  - 880mW/max @ 10 ns
- Low power consumption: STANDBY
  - 55mW/max CMOS
- Equal access and cycle times
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- TTL-compatible, three-state I/O
- JEDEC standard packages
  - 400 mil 36-pin SOJ
  - 44-pin TSOP 2
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram



Pin arrangements



Selection guide

	–10	–12	–15	–20	Unit
Maximum address access time	10	12	15	20	ns
Maximum outputenable access time	5	6	6	6	ns
Maximum operating current	160	140	120	100	mA
Maximum CMOS standby current	10	10	10	10	mA

Functional description

The AS7C4096A is a high-performance CMOS 4,194,304-bit Static Random Access Memory (SRAM) device organized as 524,288 words × 8 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 10/12/15/20 ns with output enable access times (t_{OE}) of 5/6 ns are ideal for high-performance applications. The chip enable input $\overline{CE}$ permits easy memory expansion with multiple-bank memory systems.

When $\overline{CE}$ is high the device enters standby mode. The device is guaranteed not to exceed 55mW power consumption in CMOS standby mode.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CE}$). Data on the input pins I/O1–I/O8 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and chip enable ($\overline{CE}$), with write enable ($\overline{WE}$) high. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5.0V supply voltage. This device is available as per industry standard 400-mil 36-pin SOJ and 44-pin TSOP 2 packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to GND	V_{t1}	–0.5	+7.0	V
Voltage on any pin relative to GND	V_{t2}	–0.5	V_{CC} +0.5	V
Power dissipation	P_D	–	1.0	W
Storage temperature (plastic)	T_{stg}	–65	+150	°C
Temperature with V_{CC} applied	T_{bias}	–55	+125	°C
DC current into output (low)	I_{OUT}	–	20	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High Z	Standby (I_{SB}, I_{SB1})
L	H	H	High Z	Output disable (I_{CC})
L	H	L	D_{OUT}	Read (I_{CC})
L	L	X	D_{IN}	Write (I_{CC})

Recommended operating condition

Parameter		Symbol	Min	Nominal	Max	Unit
Supply voltage		V_{CC}(10/12/15/20)	4.5	5.0	5.5	V
Input voltage		V_{IH}*	2.2	–	V_{CC} + 0.5	V
		V_{IL}**	–0.5	–	0.8	V
Ambient operating temperature	commercial	T_A	0	–	70	°C
	industrial	T_A	–40	–	85	°C

*V_{IH} max = V_{CC} + 1.5V for pulse width less than 5 nS.

**V_{IL} min = –1.0V for pulse width less than 5 nS.

DC operating characteristics (over the operating range)[1]

Parameter	Symbol	Test conditions	–10		–12		–15		–20		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Input leakage current	$\|I_{LI}\|$	V_{CC} = Max, V_{IN} = GND to V_{CC}	–	1	–	1	–	1	–	1	µA	
Output leakage current	$\|I_{LO}\|$	V_{CC} = Max, $\overline{CE}$ = V_{IH} V_{OUT}= GND to V_{CC}	–	1	–	1	–	1	–	1	µA	
Operating power supply current	I_{CC}	V_{CC} = Max, $\overline{CE}$ < V_{IL} f = f_{Max}, I_{OUT} = 0mA	–	160	–	140	–	120	–	100	mA	
Standby power supply current	I_{SB}	V_{CC} = Max, $\overline{CE}$ ≥ V_{IH} f = f_{Max}, I_{OUT} = 0mA	–	60	–	55	–	50	–	40	mA	
	I_{SB1}	V_{CC} = Max, $\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} – 0.2V, f = 0	–	10	–	10	–	10	–	10	mA	
Output voltage	V_{OL}	I_{OL} = 6 mA, V_{CC} = Min	–	0.4	–	0.4	–	0.4	–	0.4	V	4
		I_{OL} = 8 mA, V_{CC} = Min	–	0.5	–	0.5	–	0.5	–	0.5		
	V_{OH}	I_{OH} = –4 mA, V_{CC} = Min	2.4	–	2.4	–	2.4	–	2.4	–	V	4

Capacitance (f = 1MHz, T_a = 25° C, V_{CC} = NOMINAL)[4]

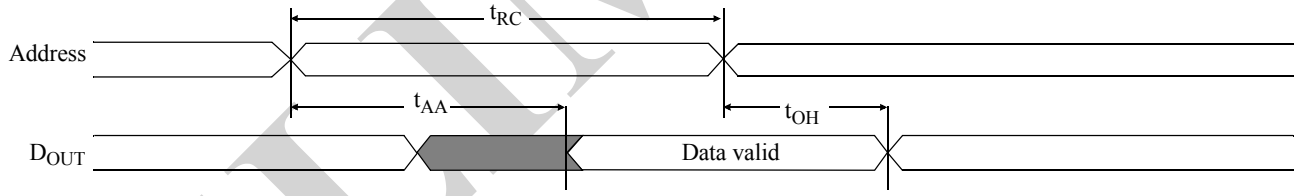
Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$	V_{IN} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{IN} = V_{OUT} = 0V	7	pF

Read cycle (over the operating range)[2,8]

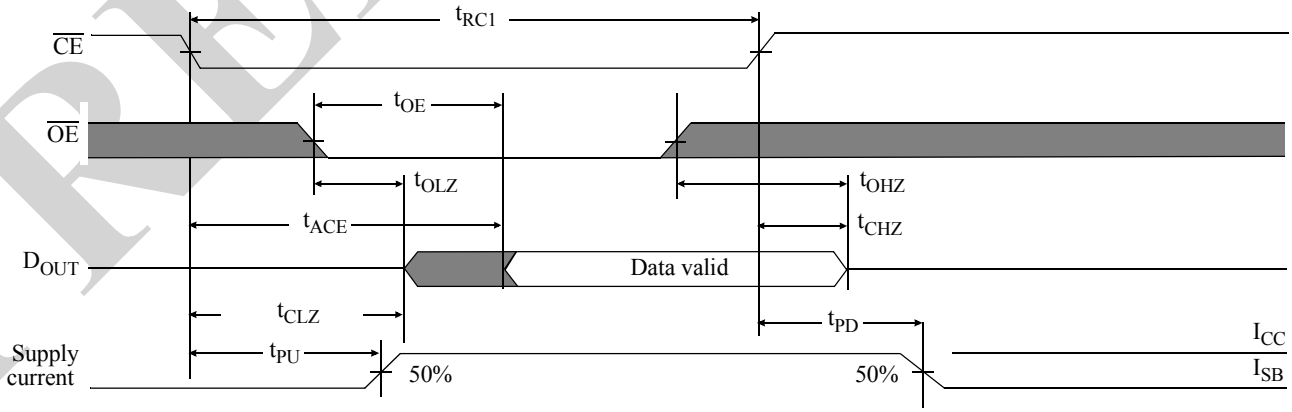
Parameter	Symbol	–10		–12		–15		–20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	10	–	12	–	15	–	20	–	ns	
Address access time	t_{AA}	–	10	–	12	–	15	–	20	ns	2
Chip enable ($\overline{CE}$) access time	t_{ACE}	–	10	–	12	–	15	–	20	ns	2
Output enable ($\overline{OE}$) access time	t_{OE}	–	5	–	6	–	6	–	6	ns	
Output hold from address change	t_{OH}	3	–	3	–	3	–	3	–	ns	4
$\overline{CE}$ Low to output in low Z	t_{CLZ}	3	–	3	–	3	–	3	–	ns	3,4
$\overline{CE}$ High to output in high Z	t_{CHZ}	–	5	–	6	–	7	–	9	ns	3,4
$\overline{OE}$ Low to output in low Z	t_{OLZ}	0	–	0	–	0	–	0	–	ns	3,4
$\overline{OE}$ High to output in high Z	t_{OHZ}	–	5	–	6	–	7	–	9	ns	3,4
Power up time	t_{PU}	0	–	0	–	0	–	0	–	ns	3,4
Power down time	t_{PD}	–	10	–	12	–	15	–	20	ns	3,4

Key to switching waveforms

Read waveform 1 (address controlled)[2,5,6,8]



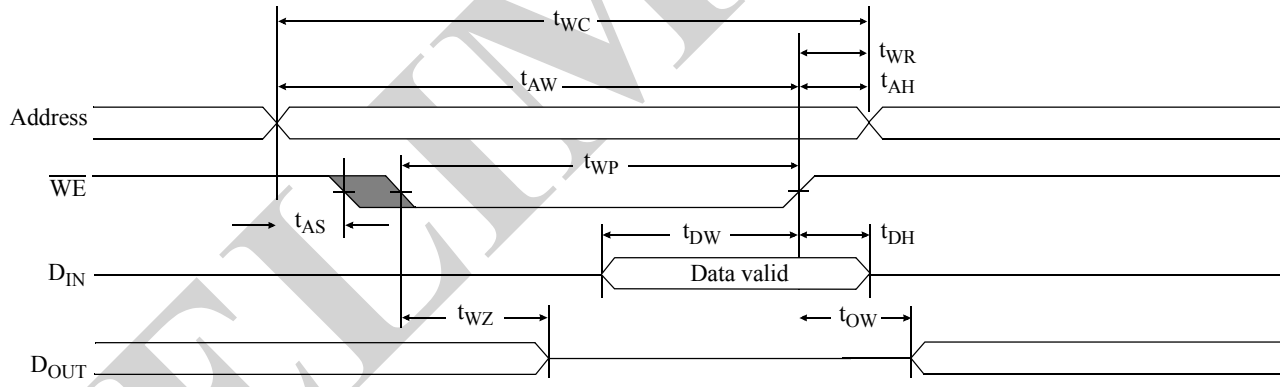
Read waveform 2 ($\overline{CE}$, $\overline{OE}$ controlled)[2,5,7,8]



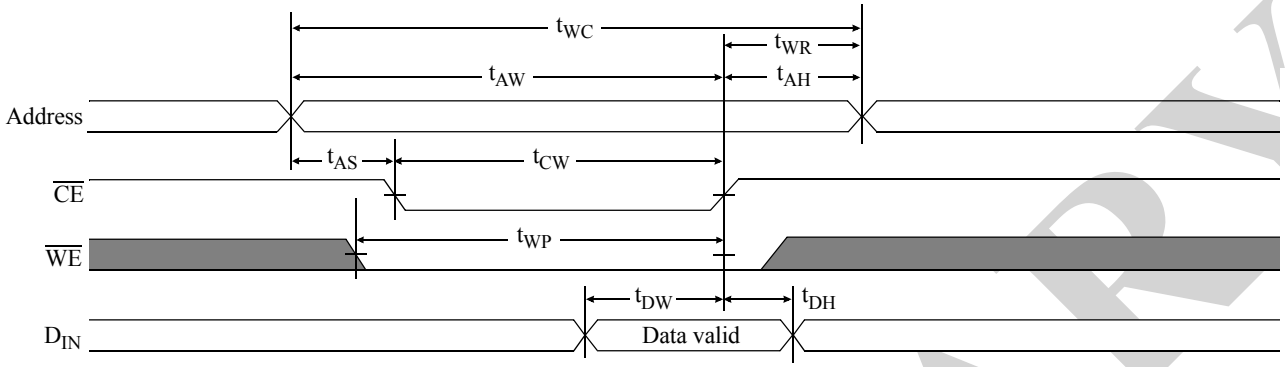
Write cycle (over the operating range)[9]

Parameter	Symbol	–10		–12		–15		–20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	10	–	12	–	15	–	20	–	ns	
Chip enable ($\overline{CE}$) to write end	t_{CW}	7	–	8	–	10	–	12	–	ns	
Address setup to write end	t_{AW}	7	–	8	–	10	–	12	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	ns	
Write pulse width ($\overline{OE}$ = high)	t_{WP1}	7	–	8	–	10	–	12	–	ns	
Write pulse width ($\overline{OE}$ = low	t_{WP2}	10	–	12	–	15	–	20	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	0	–	ns	
Write recovery time	t_{WR}	0	–	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	5	–	6	–	7	–	9	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	0	–	ns	3,4
Write enable to output in high Z	t_{WZ}	2	5	2	6	2	7	2	9	ns	3,4
Output active from write end	t_{OW}	3	–	3	–	3	–	3	–	ns	3,4

Write waveform 1 ($\overline{WE}$ controlled)[9]



Write waveform 2 ($\overline{CE}$ controlled)[9]



AC test conditions

- Output load: see Figure B.
- Input pulse level: GND to V_{CC} - 0.5V. See Figures A and B.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

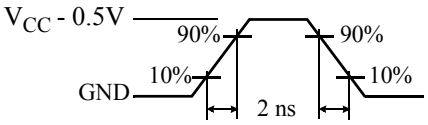


Figure A: Input pulse

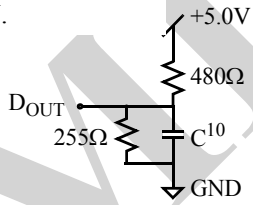
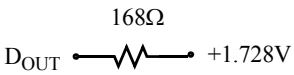


Figure B: 5.0V Output load

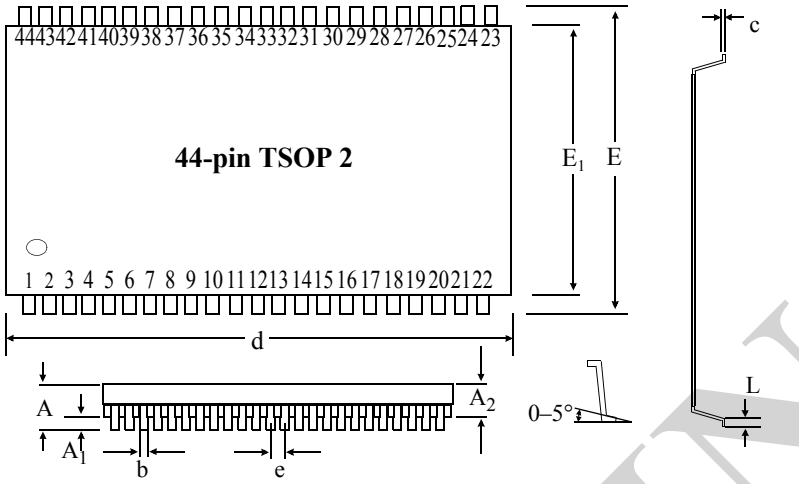
Thevenin equivalent:



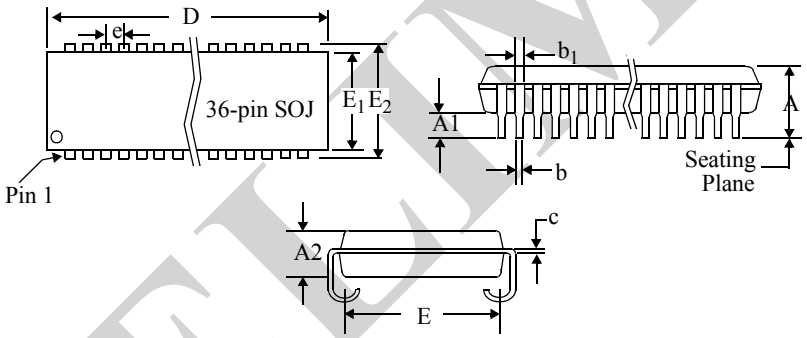
Notes

1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE}$ is required to meet I_{SB} specification.
2 For test conditions, see *AC Test Conditions*.
3 t_{CLZ} and t_{CHZ} are specified with C_L = 5pF as in Figure B. Transition is measured ±500 mV from steady-state voltage.
4 This parameter is guaranteed, but not tested.
5 $\overline{WE}$ is HIGH for read cycle.
6 $\overline{CE}$ and $\overline{OE}$ are LOW for read cycle.
7 Address valid prior to or coincident with $\overline{CE}$ transition Low.
8 All read cycle timings are referenced from the last valid address to the first transitioning address.
9 All write cycle timings are referenced from the last valid address to the first transitioning address.
10 C = 30pF, except at high Z and low Z parameters, where C = 5pF.

Package dimensions



	44-pin TSOP 2	
	Min(mm)	Max(mm)
A		1.2
A_1	0.05	0.15
A_2	0.95	1.05
b	0.30	0.45
c	0.12	0.21
d	18.31	18.52
E_1	10.06	10.26
E	11.68	11.94
e	0.80 (typical)	
L	0.40	0.60



	36-pin SOJ 400	
	Min(mils)	Max(mils)
A	0.128	0.148
A_1	0.025	–
A_2	0.105	0.115
b	0.015	0.020
b_1	0.026	0.032
c	0.007	0.013
D	.920	.930
e	0.045	0.055
E	0.370 BSC	
E_1	0.395	0.405
E_2	0.435	0.445

Ordering codes

Package	Version	10 ns	12 ns	15 ns	20 ns
SOJ	Commercial	AS7C4096A-10JC	AS7C4096A-12JC	AS7C4096A-15JC	AS7C4096A-20JC
	Industrial	AS7C4096A-10JI	AS7C4096A-12JI	AS7C4096A-15JI	AS7C4096A-20JI
TSOP 2	Commercial	AS7C4096A-10TC	AS7C4096A-12TC	AS7C4096A-15TC	AS7C4096A-20TC
	Industrial	AS7C4096A-10TI	AS7C4096A-12TI	AS7C4096A-15TI	AS7C4096A-20TI

Note: Add suffix 'N' to the above part number for Lead Free Parts. (Ex: AS7C4096A - 10 TIN)

Part numbering system

AS7C	4096A	–XX	J or T	X	X
SRAM prefix	Device number	Access time	Packages: J: SOJ 400 mil T: TSOP 2	Temperature ranges: C: Commercial, 0°C to 70°C I: Industrial, –40°C to 85°C	N=Lead Free Parts

Revision History

Rev. No.	History	Revised Date
v1.0	Initial release	11/08/04
v1.1	Included I_{CC}, I_{SB} & I_{SB1} parameters	05/27/05
	Corrected the following: T_{OE}, $V_{IH,}$ V_{OL} & t_{WZ}	

Alliance Semiconductor Corporation
2575, Augustine Drive,
Santa Clara, CA 95054
Tel: 408 - 855 - 4900
Fax: 408 - 855 - 4999

www.alsc.com

Part Number: AS7C4096A
Document Version: v. 1.1