PRELIMINARY

Integrated Circuit Systems, Inc.

ICS813001I

DUAL VCXO W/3.3V, 2.5V LVPECL FEMTOCLOCK™ PLL

GENERAL DESCRIPTION

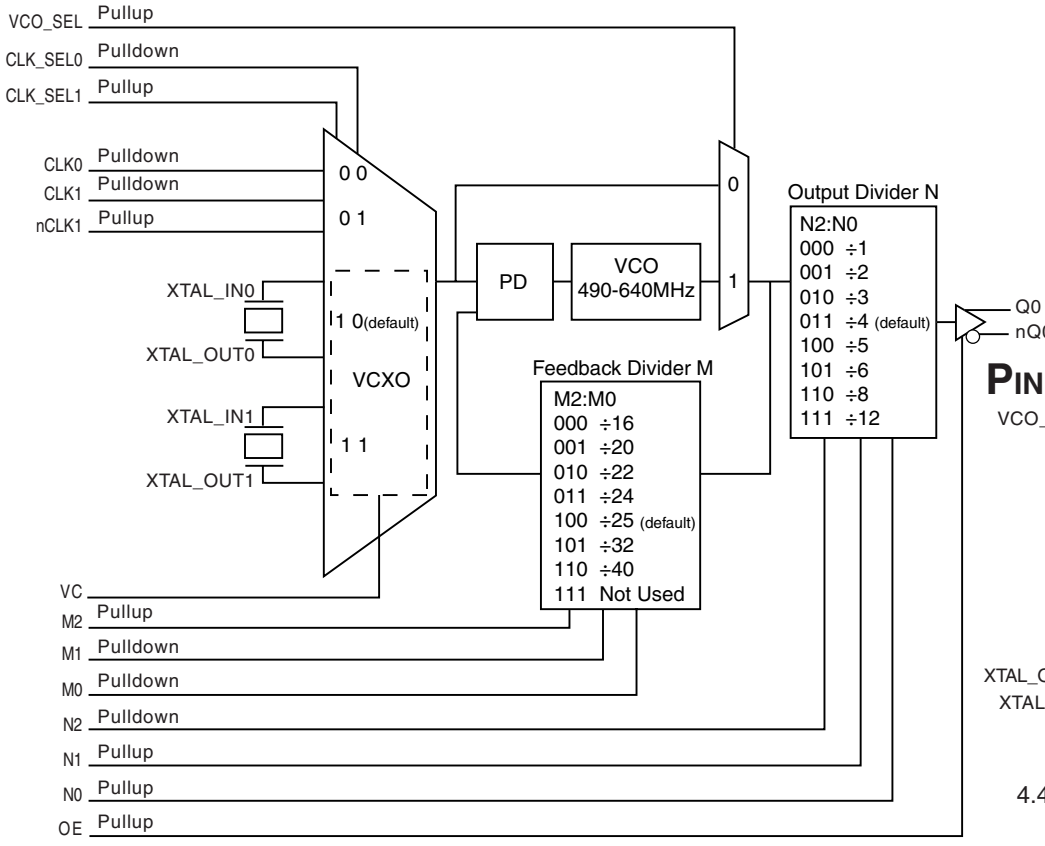
The ICS813001I is a dual VCXO + FemtoClock™ Multiplier designed for use in Discrete PLL loops. Two selectable external VCXO crystals allow the device to be used in multi-rate applications, where a given line card can be switched, for example, between 1Gb Ethernet (125MHz system reference clock) and 1Gb Fibre Channel (106.25MHz system reference clock) modes. Of course, a multitude of other applications are also possible such as switching between 74.25MHz and 74.175824MHz for HDTV, switching between SONET, FEC and non FEC rates, etc.

The ICS813001I is a two stage device – a VCXO followed by a FemtoClock™ PLL. The FemtoClock™ PLL can multiply the crystal frequency of the VCXO up to a range of 40.83MHz to 640MHz, with a random rms phase jitter of less than 1 ps (12kHz – 20MHz). This phase jitter performance meets the requirements of 1Gb/10Gb Ethernet, 1Gb, 2Gb, 4Gb and 10Gb Fibre Channel, and SONET up to OC48. The FemtoClock™ PLL can also be bypassed if frequency multiplication is not required. For testing/debug purposes, de-assertion of the output enable pin will place both Q0 and nQ0 in a high impedance state.

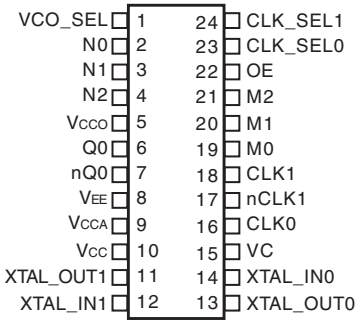
FEATURES

- One 3.3V or 2.5V LVPECL output pair
- Two selectable crystal oscillator interfaces for the VCXO, one differential clock or one LVCMOS/LVTTL clock inputs
- CLK1 and nCLK1 supports the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Crystal operating frequency range: 14MHz - 24MHz
- VCO range: 490MHz - 640MHz
- Output frequency range: 40.83MHz - 640MHz
- VCXO pull range: ±100ppm (typical)
- Supports the following applications (among others): SONET, Ethernet, Fibre Channel, HDTV, MPEG
- RMS phase jitter @ 622.08MHz (12kHz - 20MHz): 0.84 (typical)
- Supply voltage modes:
  V_{CC}/V_{CCO}
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- -40°C to 85°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS813001I
24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm
package body
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	VCO_SEL	Input	Pullup	VCO select pin. LVCMOS/LVTTL interface levels.
2, 3	N0, N1	Input	Pullup	Output divider select pins. Default value = ÷4. LVCMOS/LVTTL interface levels.
4	N2	Input	Pulldown	
5	V_{CCO}	Power		Output supply pin.
6, 7	Q0, nQ0	Ouput		Differential output pair. LVPECL interface levels.
8	V_{EE}	Power		Negative supply pin.
9	V_{CCA}	Power		Analog supply pin.
10	V_{CC}	Power		Core supply pin.
11 12	XTAL_OUT1, XTAL_IN1	Input		Parallel resonant crystal interface. XTAL_OUT1 is the output, XTAL_IN1 is the input.
13 14	XTAL_OUT0, XTAL_IN0	Input		Parallel resonant crystal interface. XTAL_OUT0 is the output, XTAL_IN0 is the input.
15	VC	Input		VCXO control voltage input.
16	CLK0	Input	Pulldown	LVCMOS/LVTTL clock input.
17	nCLK1	Input	Pullup	Inverting differential clock input.
18	CLK1	Input	Pulldown	Non-inverting differential clock input.
19, 20	M0, M1	Input	Pulldown	Feedback divider select pins. Default value = ÷25. LVCMOS/LVTTL interface levels.
21	M2	Input	Pullup	
22	OE	Input	Pullup	Output enable. When HIGH, the output is active. When LOW, the output is in a high impedance state. LVCMOS/LVTTL interface levels.
23	CLK_SEL0	Input	Pulldown	Clock select pin. Selects CLK0. LVCMOS/LVTTL interface levels.
24	CLK_SEL1	Input	Pullup	Clock select pin. When LOW, selects CLK1. When HIGH, selects nCLK1. LVCMOS/LVTTL interface levels.

NOTE: *Pulldown and Pullup* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL)	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	70°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			110		mA
I_{CCO}	Output Supply Current			5		mA

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA}$ = 3.3V±5%, V_{CCO} = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			110		mA
I_{CCO}	Output Supply Current			5		mA

TABLE 3C. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			105		mA
I_{CCO}	Output Supply Current			5		mA

TABLE 3C. LVCMOS / LVTTL DC CHARACTERISTICS, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2.0		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V	-0.3		0.8	V
			V_{CC} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	N2, M0, M1, CLK0, CLK_SEL0	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
		N0, N1, M2, VCO_SEL, CLK_SEL1	V_{CC} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	N2, M0, M1, CLK0, CLK_SEL0	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		N0, N1, M2, VCO_SEL, CLK_SEL1	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

TABLE 3D. DIFFERENTIAL DC CHARACTERISTICS, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK1	V_{IN} = V_{CC} = 3.465V or 2.625V			150	µA
		nCLK1	V_{IN} = V_{CC} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	CLK1	V_{IN} = 0V, V_{CC} = 3.465V or 2.625V	-5			µA
		nCLK1	V_{IN} = 0V, V_{CC} = 3.465V or 2.625V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended appliations, the maximum input voltage for CLK1, nCLK1 is V_{CC} + 0.3V.

TABLE 3E. LVPECL DC CHARACTERISTICS, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			MHz
Frequency		14		24	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Load				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5A. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	VCO_SEL = 1	40.83		640	MHz
$t$jit(Ø)	RMS Phase Jitter, (Random); NOTE 1, 2	622.08MHz (12kHz - 20MHz)		0.84		ps
f_{VCO}	PLL VCO Lock Range		490		640	MHz
t_L	PLL Lock Time			TBD		ms
t_R / t_F	Output Rise/Fall Time	20% to 80%		400		ps
odc	Output Duty Cycle			50		%

NOTE 1: Phase jitter using a crystal interface.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{CC} = V_{CCA}$ = 3.3V±5%, V_{CCO} = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	VCO_SEL = 1	40.83		640	MHz
$t$jit(Ø)	RMS Phase Jitter, (Random); NOTE 1, 2	622.08MHz (12kHz - 20MHz)		0.87		ps
f_{VCO}	PLL VCO Lock Range		490		640	MHz
t_L	PLL Lock Time			TBD		ms
t_R / t_F	Output Rise/Fall Time	20% to 80%		370		ps
odc	Output Duty Cycle			50		%

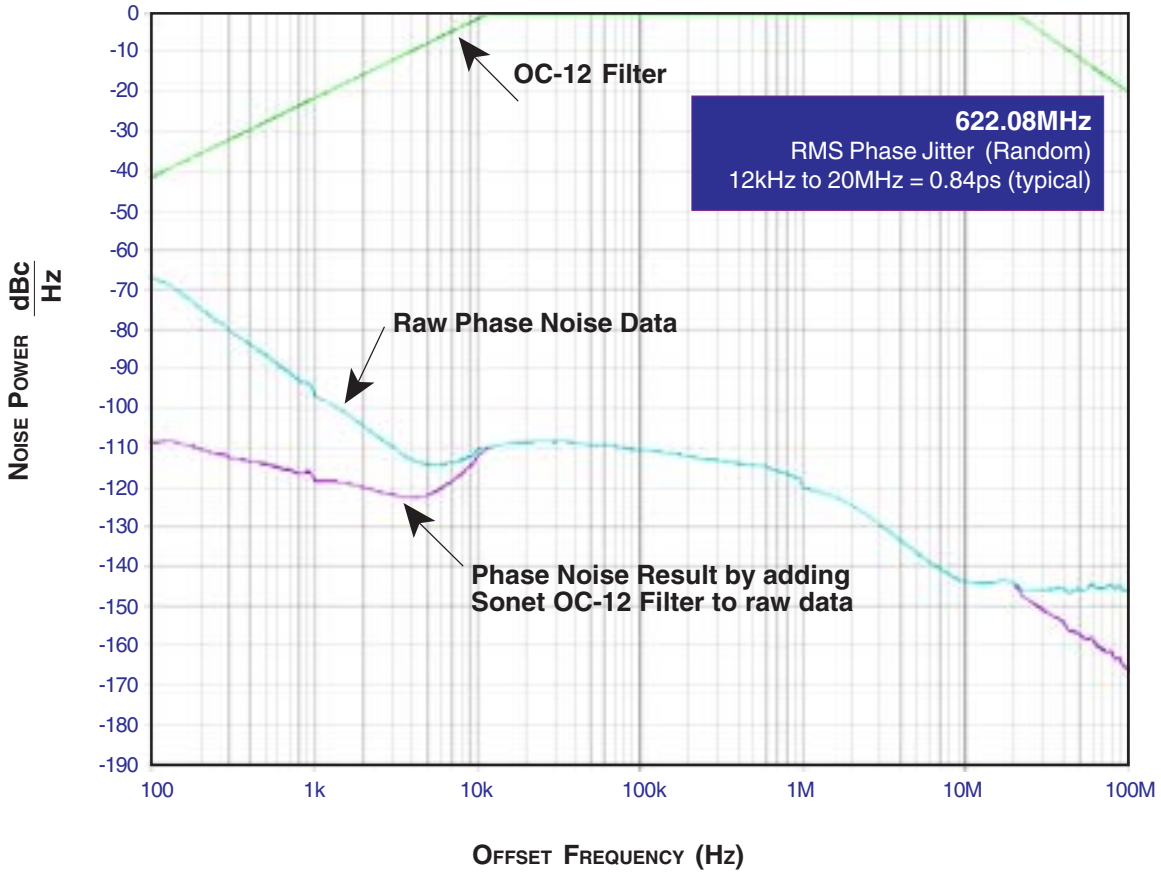
NOTE 1: Phase jitter using a crystal interface.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5C. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 2.5V±5%, TA = -40°C TO 85°C

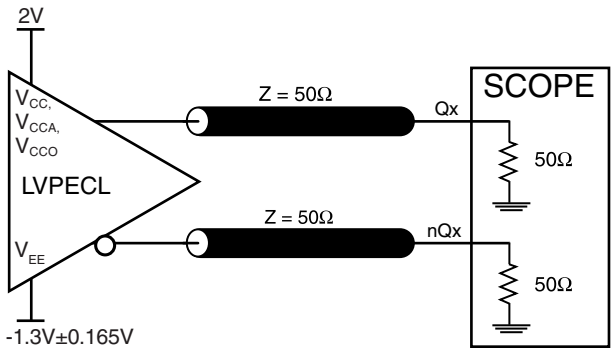
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	VCO_SEL = 1	40.83		640	MHz
f_{IN}	Input Frequency		12.25		40	MHz
$t$jit(Ø)	RMS Phase Jitter, (Random); NOTE 1, 2	622.08MHz (12kHz - 20MHz)		1.2		ps
f_{VCO}	PLL VCO Lock Range		490		640	MHz
t_L	PLL Lock Time			TBD		ms
t_R / t_F	Output Rise/Fall Time	20% to 80%		370		ps
odc	Output Duty Cycle			50		%

NOTE 1: Phase jitter using a crystal interface.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

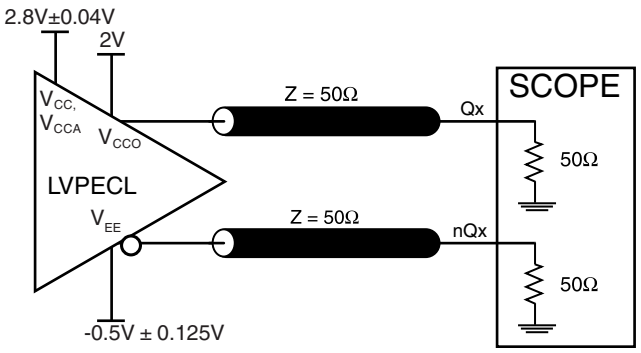
TYPICAL PHASE NOISE AT 622.08MHZ



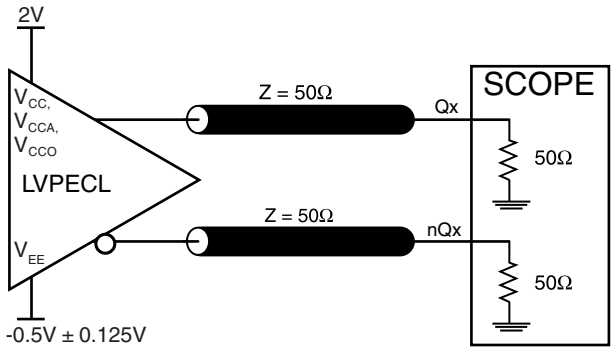
PARAMETER MEASUREMENT INFORMATION



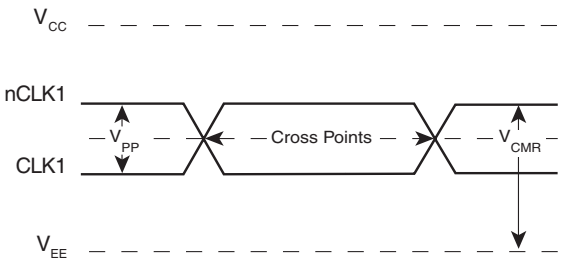
3.3V CORE/3.3V LVPECL OUTPUT LOAD AC TEST CIRCUIT



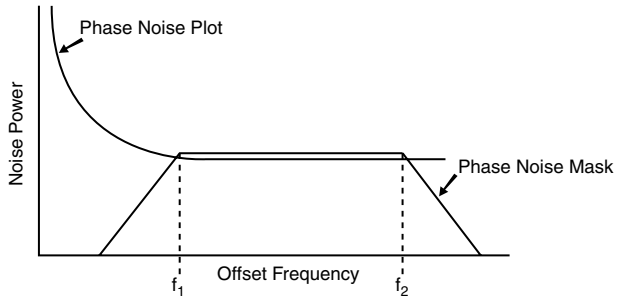
3.3V CORE/2.5V LVPECL OUTPUT LOAD AC TEST CIRCUIT



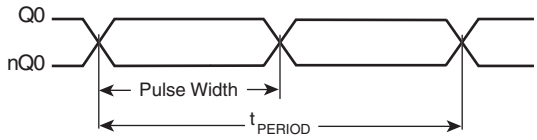
2.5V CORE/2.5V LVPECL OUTPUT LOAD AC TEST CIRCUIT



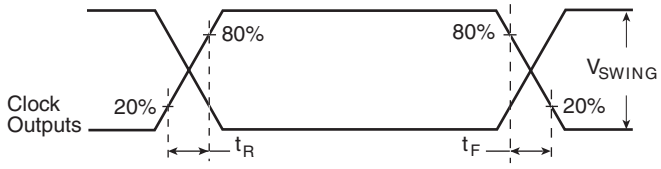
DIFFERENTIAL INPUT LEVELS



RMS PHASE JITTER



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS813001I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA}.

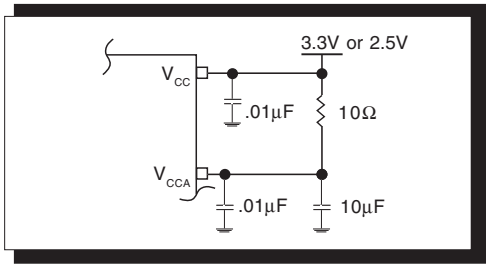


FIGURE 1. POWER SUPPLY FILTERING

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

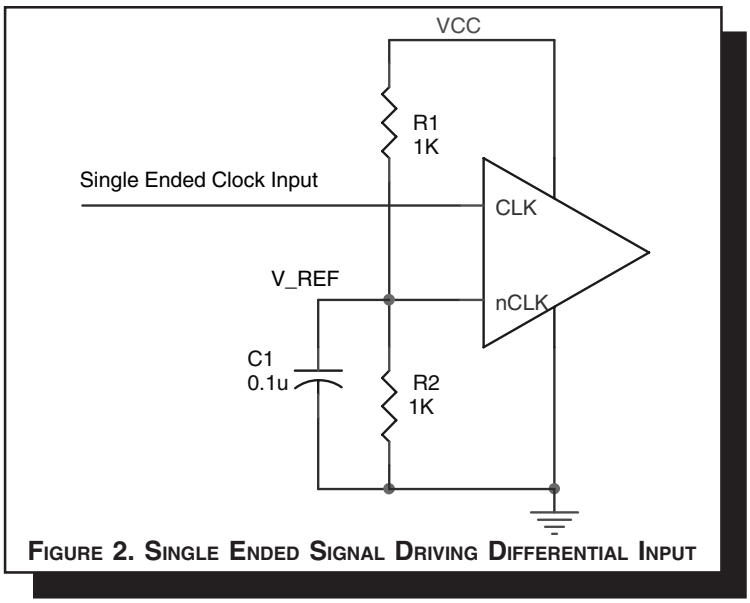


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

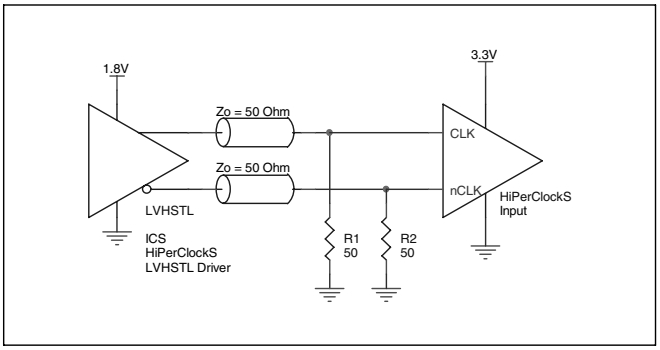


FIGURE 3A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

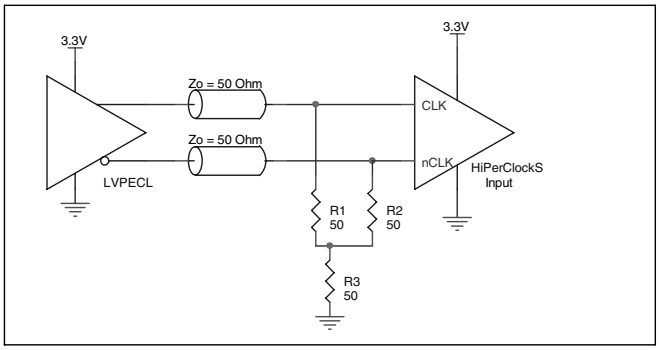


FIGURE 3B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

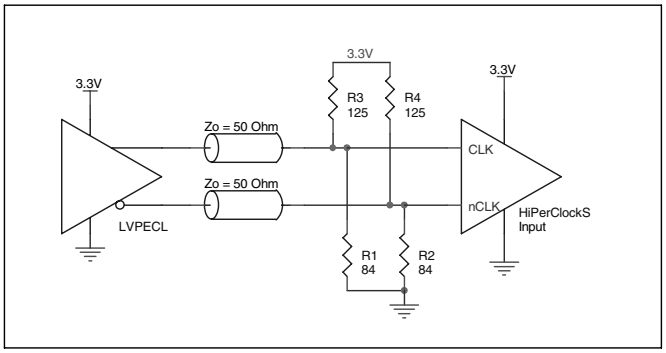


FIGURE 3C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

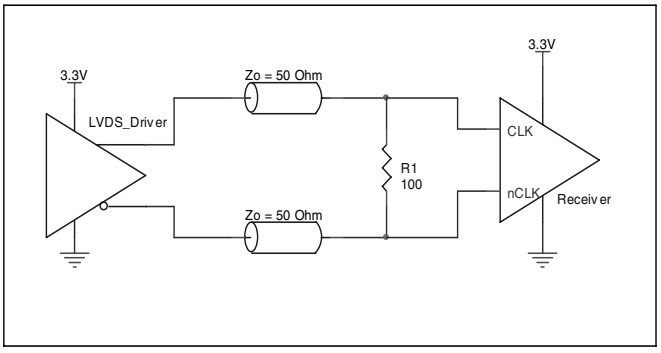


FIGURE 3D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

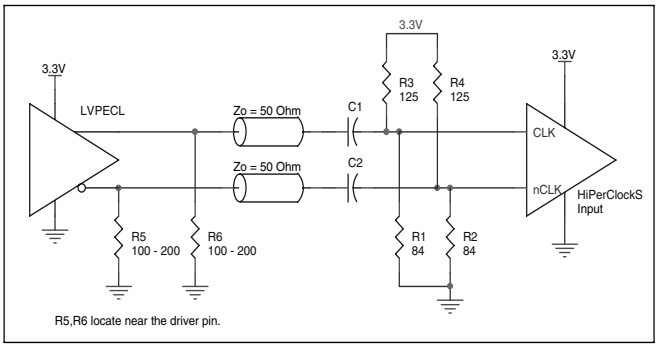


FIGURE 3E. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

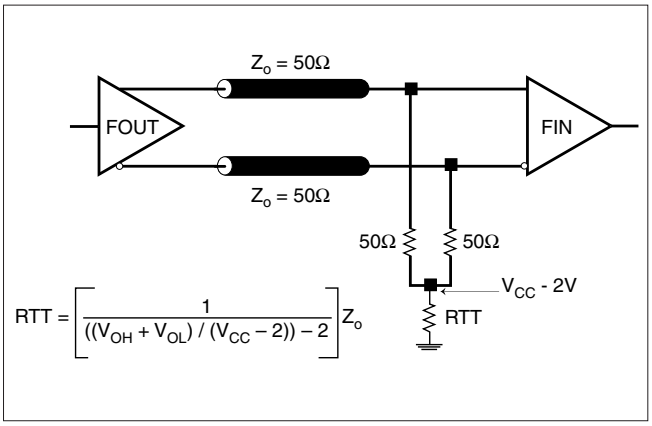


FIGURE 4A. LVPECL OUTPUT TERMINATION

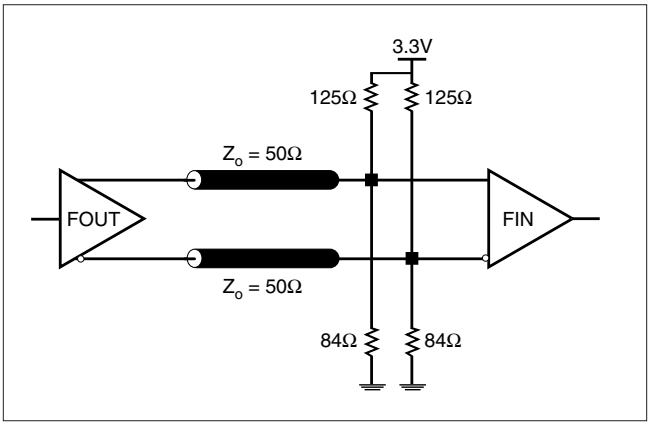


FIGURE 4B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CCO} = 2.5V, the V_{CCO} - 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

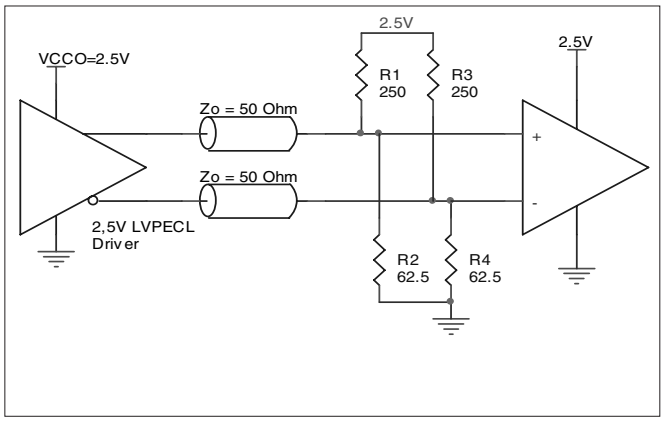


FIGURE 5A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

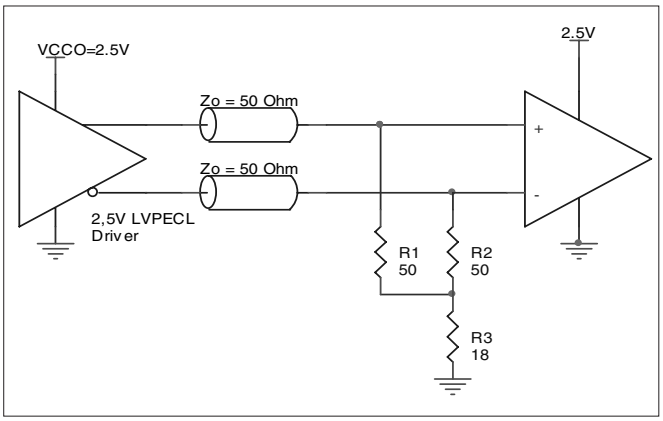


FIGURE 5B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

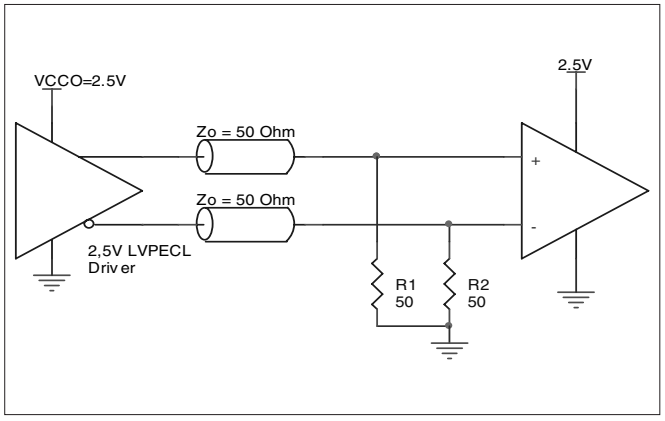


FIGURE 5C. 2.5V LVPECL TERMINATION EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS813001I.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS813001I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 110mA = **381.15mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**

Total Power$_{_MAX}$ (3.465V, with output switching) = 381.2mW + 30mW = **411.2mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 70°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.411W * 65°C/W = 111.7°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 24-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

3. Calculations and Equations.
The purpose of this section is to derive the power dissipated into the load.
LVPECL output driver circuit and termination are shown in *Figure 6.*

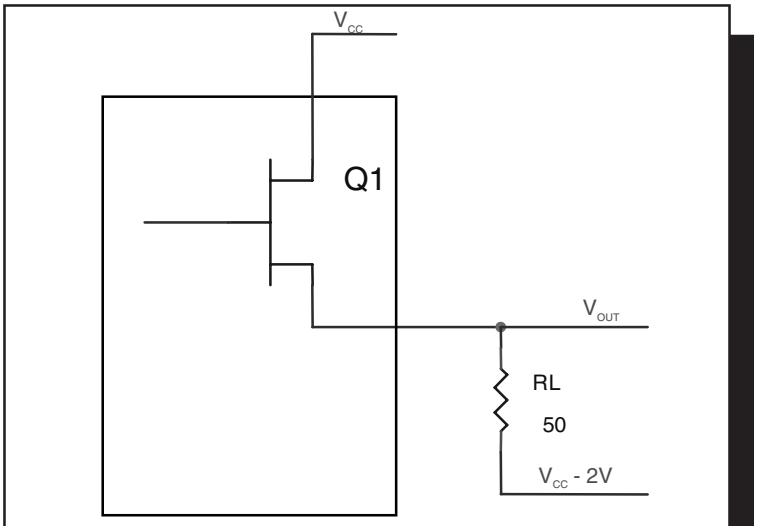


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50Ω] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

TRANSISTOR COUNT

The transistor count for ICS813001I is: 3948

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

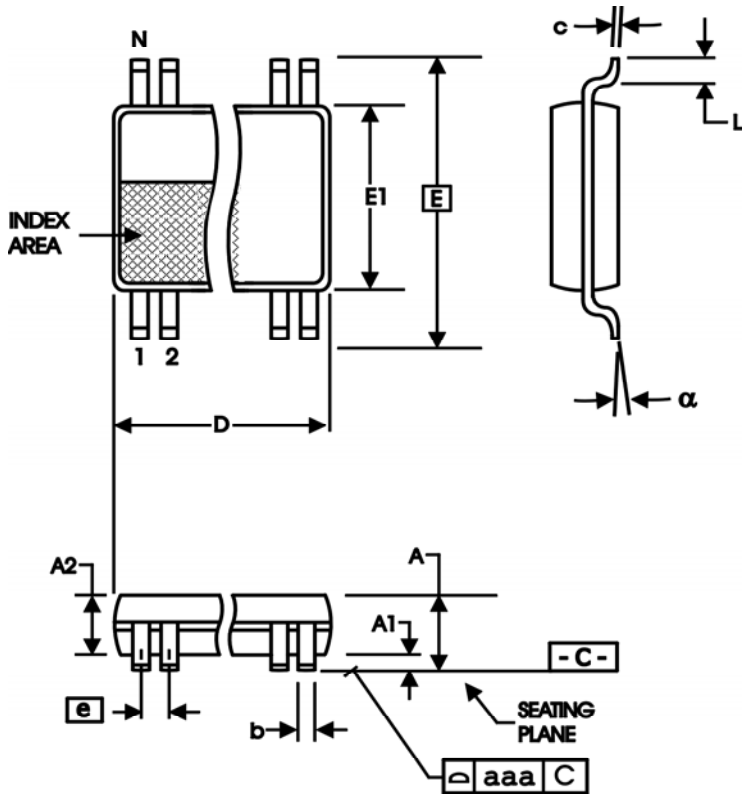


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS813001AGI	ICS813001AGI	24 Lead TSSOP	tube	-40°C to 85°C
ICS813001AGIT	ICS813001AGI	24 Lead TSSOP	tape & reel	-40°C to 85°C