



Integrated
Circuit
Systems, Inc.

PRELIMINARY

ICS843001-22

FEMTOCLOCKS™ CRYSTAL-TO-3.3V LVPECL FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The ICS843001-22 is a highly versatile, low phase noise LVPECL Synthesizer which can generate low jitter reference clocks for a variety of communications applications and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. The dual crystal interface allows the synthesizer to support up to two communications standards in a given application (i.e. 1Gb Ethernet with a 25MHz crystal and 1Gb Fibre Channel using a 25.5625MHz crystal). The rms phase jitter performance is typically less than 1ps, thus making the device acceptable for use in demanding applications such as OC48 SONET and 10Gb Ethernet. The ICS843001-22 is packaged in a small 24-pin TSSOP package.

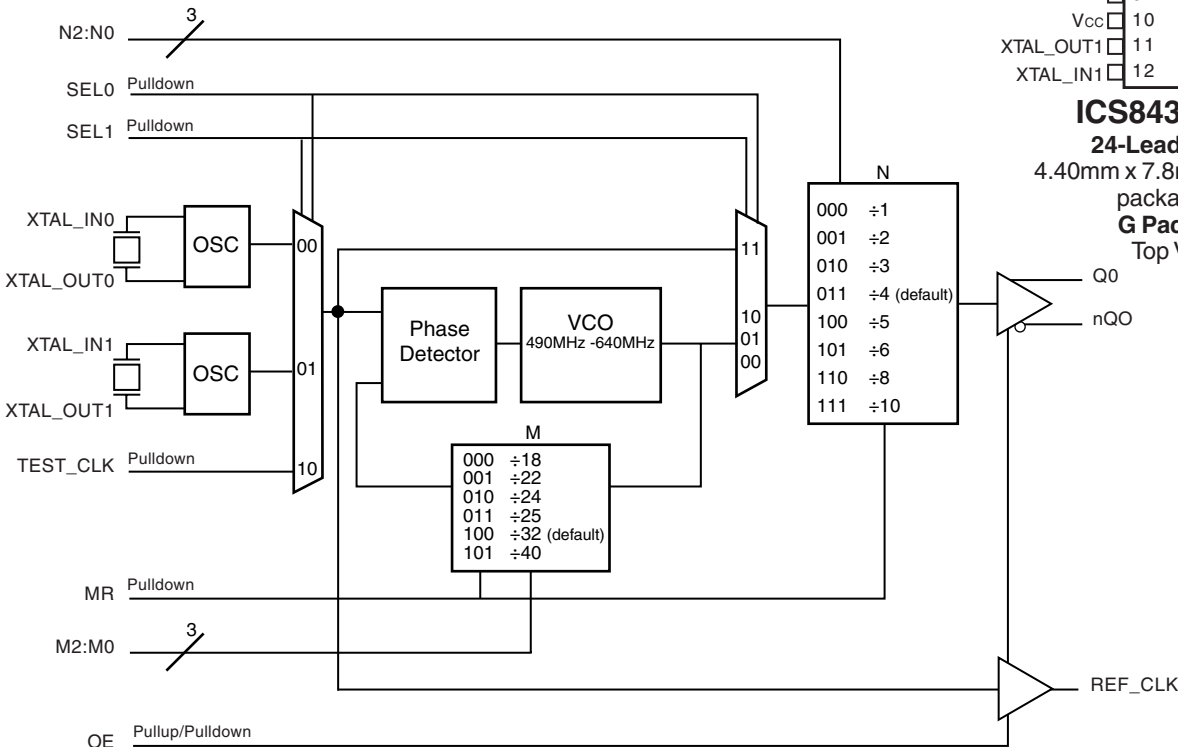
FEATURES

- One 3.3V LVPECL output pair and one LVCMOS output
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- VCO range: 490MHz - 640MHz
- Output frequency range: 490MHz - 640MHz
- Supports the following applications: SONET, Ethernet, Fibre Channel, Serial ATA, and HDTV
- RMS phase jitter @ 622.08MHz (12kHz - 20MHz): 0.79ps (typical) design target
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature

CONTROL INPUT FUNCTION TABLE

Control Input	Outputs	
OE	Q0/nQ0	REF_CLK
0	High-Z	High-Z
1	Active	High-Z
FLOAT	High-Z	Active

BLOCK DIAGRAM



PIN ASSIGNMENT

VCCO_CMOS	1	24	REF_CLK
N0	2	23	VEE
N1	3	22	OE
N2	4	21	M2
VCCO_PECL	5	20	M1
Q0	6	19	M0
nQ0	7	18	MR
VEE	8	17	SEL1
VCCA	9	16	SELO
VCC	10	15	TEST_CLK
XTAL_OUT1	11	14	XTAL_IN0
XTAL_IN1	12	13	XTAL_OUT0

ICS843001-22

24-Lead TSSOP

4.40mm x 7.8mm x 0.92mm

package body

G Package

Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.



TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V _{CCO_CMOS}	Power		Output supply pin for REF_CLK output.
2, 3	N0, N1	Input	Pullup	Output divider select pins. Default value = ÷4. LVCMOS/LVTTL interface levels.
4	N2	Input	Pulldown	
5	V _{CCO_PECL}	Power		Output supply pin for Q0/nQ0 LVPECL output.
6, 7	Q0, nQ0	Output		Differential output pair. LVPECL interface levels.
8, 23	V _{EE}	Power		Negative supply pin.
9	V _{CCA}	Power		Analog supply pin.
10	V _{CC}	Power		Core supply pin.
11, 12	XTAL_OUT1, XTAL_IN1	Input		Parallel resonant crystal interface. XTAL_OUT1 is the output, XTAL_IN1 is the input.
13, 14	XTAL_OUT0, XTAL_IN0	Input		Parallel resonant crystal interface. XTAL_OUT0 is the output, XTAL_IN0 is the input.
15	TEST_CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
16, 17	SEL0, SEL1	Input	Pulldown	Input MUX select pins. LVCMOS/LVTTL interface levels.
18	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true output Q0 to go low and the inverted output nQ0 to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
19, 20	M0, M1	Input	Pulldown	Feedback divider select pins. Default value = ÷32. LVCMOS/LVTTL interface levels.
21	M2	Input	Pullup	
22	OE	Input	Pullup/ Pulldown	3-State clock output enable, (High/Low/Float). LVCMOS/LVTTL interface levels. See Control Input Function Table for states.
24	REF_CLK	Output		Reference clock output. LVCMOS/LVTTL interface levels.

NOTE: *Pulldown and Pullup* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ
R _{PULLUP}	Input Pullup Resistor			51		kΩ
R _{out}	Output Impedance			15		Ω



Integrated
Circuit
Systems, Inc.

PRELIMINARY

ICS843001-22
FEMTOCLOCKS™ CRYSTAL-TO-
3.3V LVPECL FREQUENCY SYNTHESIZER

TABLE 3A. COMMON CONFIGURATIONS TABLE

Input Reference Clock	M Divider Value	N Divider Value	VCO (MHz)	Output Frequency (MHz)	Application
27	22	8	594	74.25	HDTV
22.4	25	8	560	70	
24.75	24	8	594	74.25	HDTV
25	24	3	600	200	
14.8351649	40	8	593.4066	74.1758245	HDTV
19.44	32	4	622.08	155.52	SONET
19.44	32	8	622.08	77.76	SONET
19.44	32	1	622.08	622.08	SONET
19.44	32	2	622.08	311.04	SONET
19.53125	32	4	625	156.25	10 GigE
20	25	2	500	250	Ethernet
25	25	5	625	125	1 GigE
25	25	10	625	62.5	1 GigE
25	24	6	600	100	PCI Express
25	24	4	600	150	SATA
25	24	8	600	75	SATA
26.5625	24	6	637.5	106.25	Fibre Channel 1
26.5625	24	3	637.5	212.5	4 Gig Fibre Channel
26.5625	24	4	637.5	159.375	10 Gig Fibre Channel
31.25	18	3	562.5	187.5	12 Gig Ethernet

TABLE 3B. PROGRAMMABLE M OUTPUT DIVIDER FUNCTION TABLE

Inputs			M Divider Value	Input Frequency (MHz)	
M2	M1	M0		Minimum	Maximum
0	0	0	18	27.22	35.56
0	0	1	22	22.27	29.09
0	1	0	24	20.41	26.67
0	1	1	25	19.6	25.6
1	0	0	32	15.31	20
1	0	1	40	12.25	16

TABLE 3C. PROGRAMMABLE N OUTPUT DIVIDER FUNCTION TABLE

Inputs			M Divide Value
N2	N1	N0	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	8
1	1	1	10

TABLE 3D. BYPASS MODE FUNCTION TABLE

Inputs		Reference	PLL Mode
SEL1	SEL0		
0	0	XTAL0	Active
0	1	XTAL1	Active
1	0	TEST_CLK	Active
1	1	TEST_CLK	Bypass



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_i	-0.5V to $V_{CC} + 0.5V$
Outputs, I_o (LVPECL)	
Continuous Current	50mA
Surge Current	100mA
Outputs, V_o (LVCMOS)	-0.5V to $V_{CCO} + 0.5V$
Package Thermal Impedance, θ_{JA}	70°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO_PECL} = V_{CCO_CMOS} = 3.3V \pm 10\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.97	3.3	3.63	V
V_{CCA}	Analog Supply Voltage		2.97	3.3	3.63	V
V_{CCO_PECL} , V_{CCO_CMOS}	Output Supply Voltage		2.97	3.3	3.63	V
I_{EE}	Power Supply Current			115		mA
I_{CCO_PECL} , I_{CCO_CMOS}	Output Supply Current			5		mA

TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO_CMOS} = 3.3V \pm 10\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	SEL0, SEL1, MR, M0:M2, N0:N2, TEST_CLK	2		$V_{CC} + 0.3$	V
		OE	$V_{CC} - 0.4$			V
V_{IL}	Input Low Voltage	SEL0, SEL1, MR, M0:M2, N0:N2, TEST_CLK	-0.3		0.8	V
		OE			$V_{CC} + 0.3$	V
I_{IH}	Input High Current	TEST_CLK, SEL0, SEL1, MR, M0, M1, N2, OE	$V_{CC} = V_{IN} = 3.63V$		150	μA
		M2, N0, N1	$V_{CC} = V_{IN} = 3.63V$		5	μA
I_{IL}	Input Low Current	TEST_CLK, SEL0, SEL1, MR, M0, M1, N2, OE	$V_{CC} = 3.63V, V_{IN} = 0V$	-5		μA
		M2, N0, N1	$V_{CC} = 3.63V, V_{IN} = 0V$	-150		μA
V_{OH}	Output High Voltage; NOTE 1		2.6			V
V_{OL}	Output Low Voltage: Note 1				0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCO_CMOS}/2$. See Parameter Measurement Information Section, "3.3V Output Load Test Circuit Diagram".



TABLE 4C. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO_PECL} = 3.3V \pm 10\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCO_PECL} - 2V$.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			MHz
Frequency		12		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO_PECL} = V_{CCO_CMOS} = 3.3V \pm 10\%$, $T_A = 0^\circ C$ TO $70^\circ C$

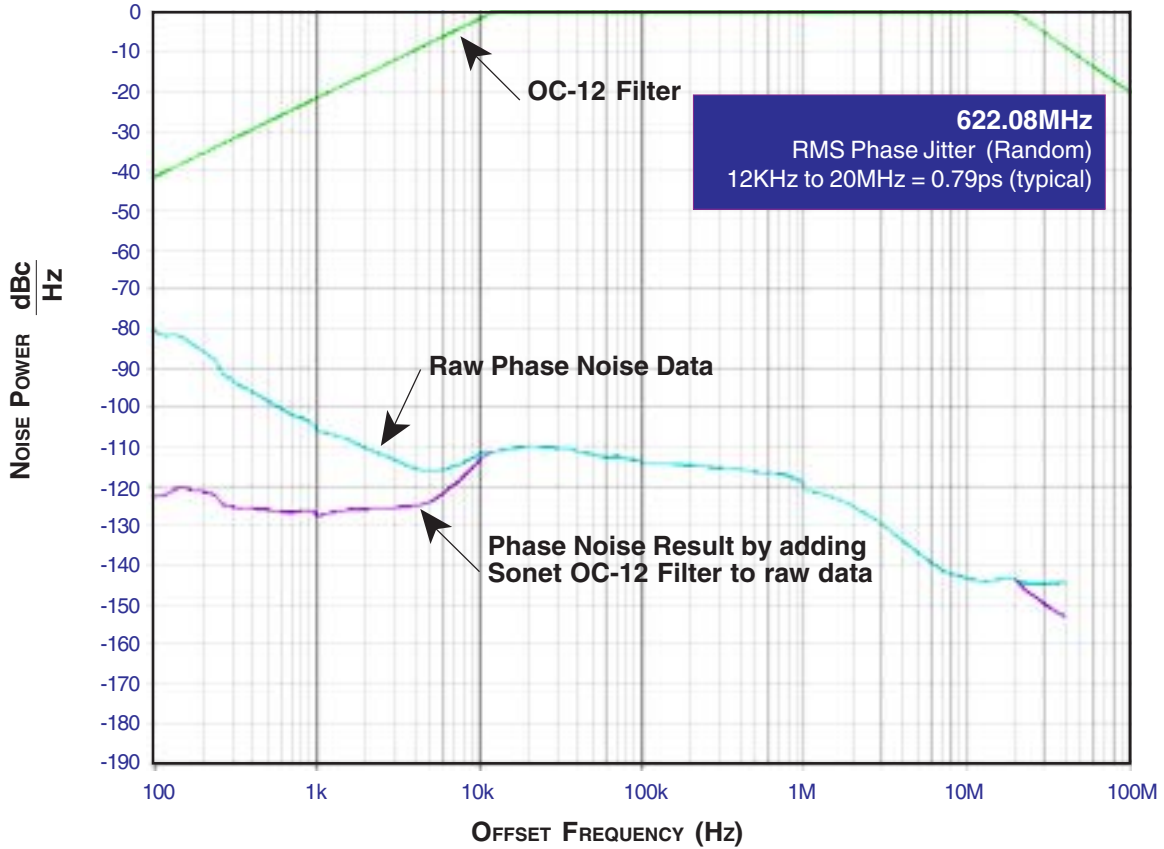
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		49		640	MHz
$f_{jit}(\emptyset)$	RMS Phase Jitter, (Random); NOTE 1, 2	622.08MHz, Integration Range: 1kHz - 20MHz		0.79		ps
f_{VCO}	PLL VCO Lock Range		490		640	MHz
t_R / t_F	Output Rise/Fall Time	20% to 80%		450		ps
odc	Output Duty Cycle			50		%

NOTE 1: Phase jitter using a crystal interface.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

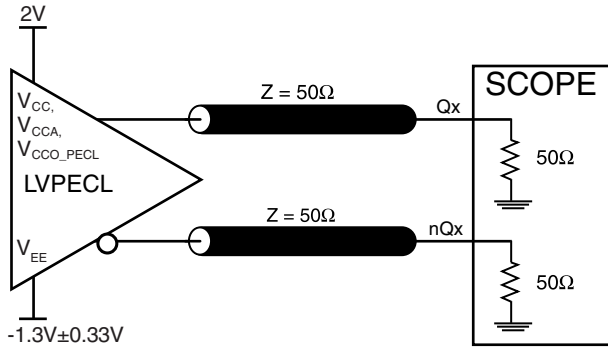


TYPICAL PHASE NOISE AT 622.08MHz

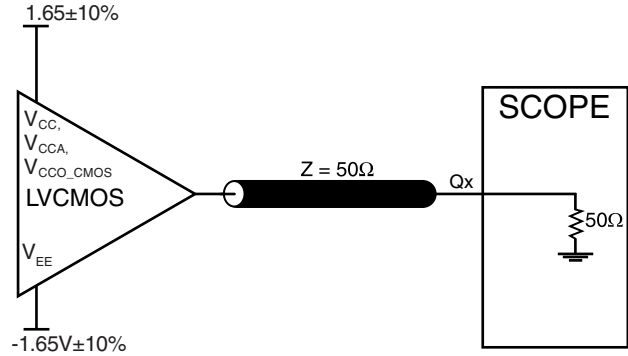




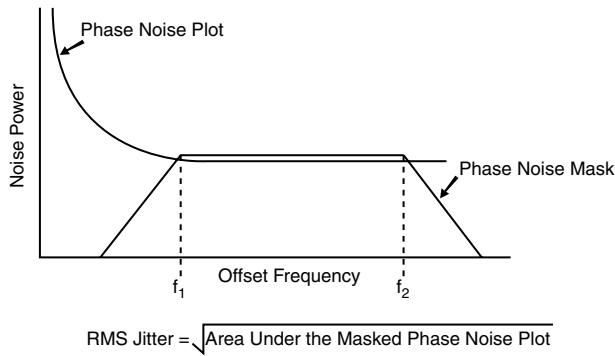
PARAMETER MEASUREMENT INFORMATION



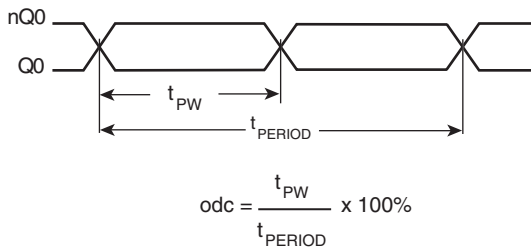
3.3V LVPECL OUTPUT LOAD AC TEST CIRCUIT



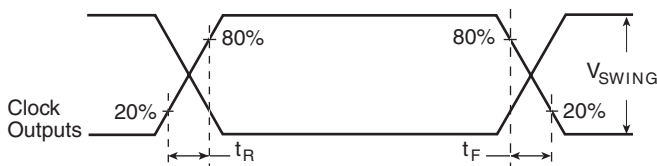
3.3V LVCMOS OUTPUT LOAD AC TEST CIRCUIT



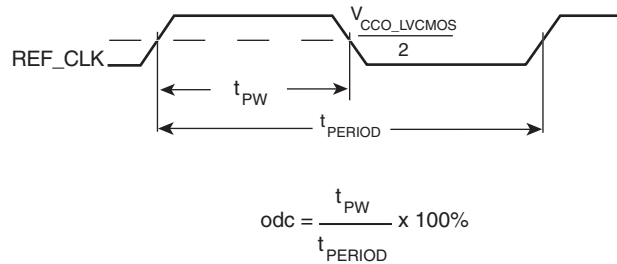
RMS PHASE JITTER



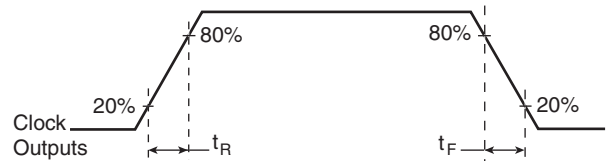
LVPECL OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



LVPECL OUTPUT RISE/FALL TIME



LVCMOS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



LVCMOS OUTPUT RISE/FALL TIME



APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843001-22 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} , V_{CCA} , and $V_{CCO,x}$ should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a $10\mu F$ and a $.01\mu F$ bypass capacitor should be connected to each V_{CCA} .

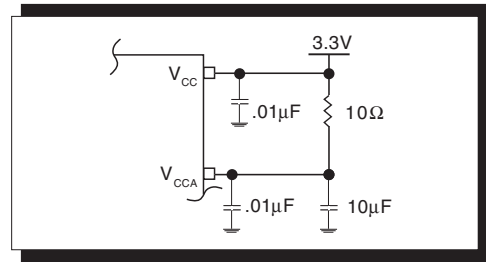


FIGURE 1. POWER SUPPLY FILTERING

TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are

designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

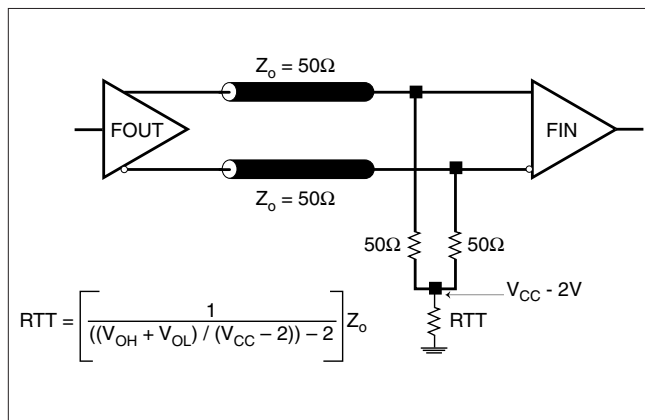


FIGURE 2A. LVPECL OUTPUT TERMINATION

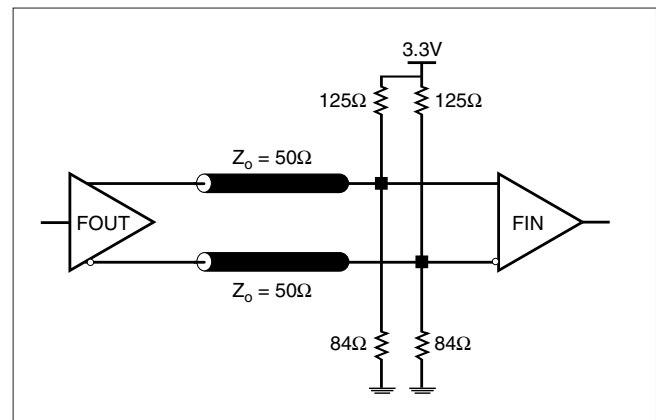


FIGURE 2B. LVPECL OUTPUT TERMINATION



CRYSTAL INPUT INTERFACE

The ICS843001-22 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 3* below were determined using a 26.5625MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

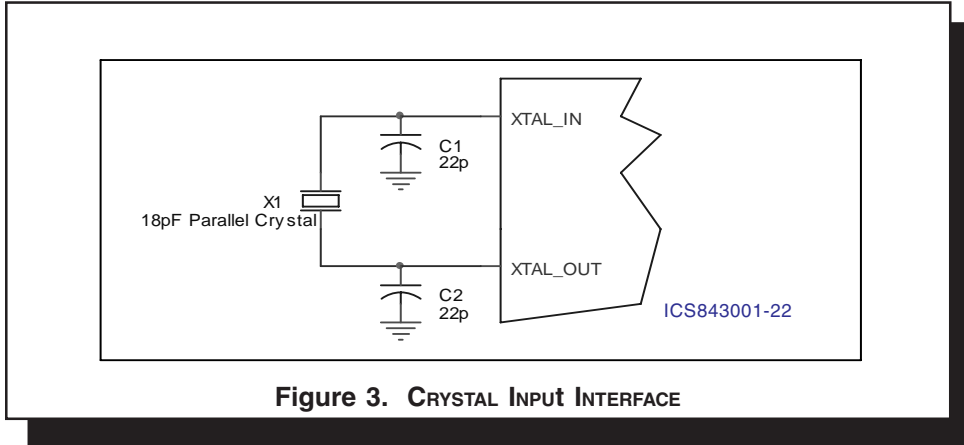


Figure 3. CRYSTAL INPUT INTERFACE

RELIABILITY INFORMATION

TABLE 7. θ_{JA} vs. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

TRANSISTOR COUNT

The transistor count for ICS843001-22 is: 4137



PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

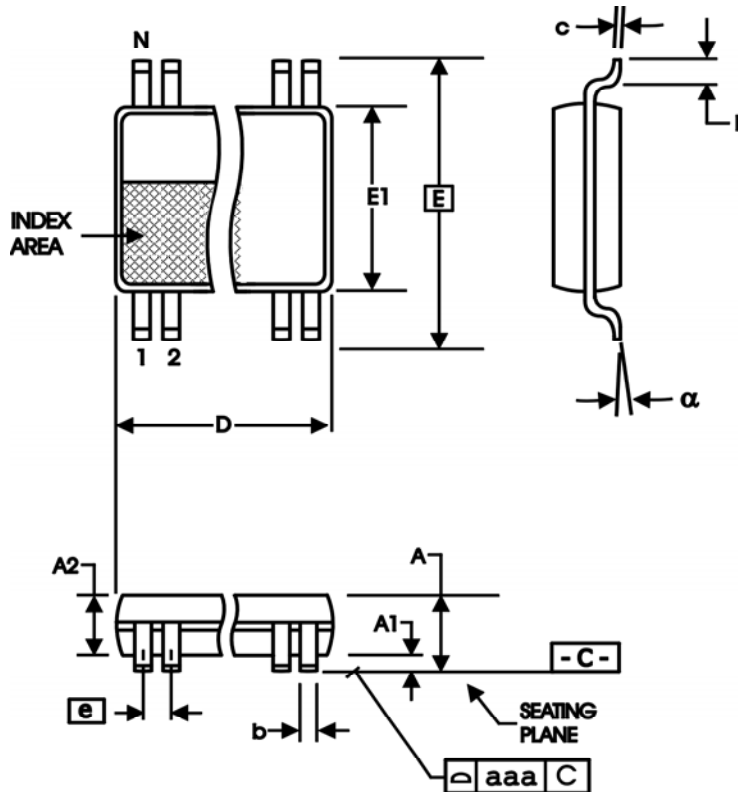


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153



Integrated
Circuit
Systems, Inc.

PRELIMINARY

ICS843001-22
FEMTOCLOCKS™ CRYSTAL-TO-
3.3V LVPECL FREQUENCY SYNTHESIZER

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843001AG-22	ICS843001AG-22	24 Lead TSSOP	tube	0°C to 70°C
ICS843001AG-22T	ICS843001AG-22	24 Lead TSSOP	2500 tape & reel	0°C to 70°C

The aforementioned trademarks, HiPerClockS™ and FemtoClocks™ are a trademark of Integrated Circuit Systems, Inc. or its subsidiaries in the United States and/or other countries. While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems, Incorporated (ICS) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by ICS. ICS reserves the right to change any circuitry or specifications without notice. ICS does not authorize or warrant any ICS product for use in life support devices or critical medical instruments.