19-3568; Rev 0; 3/05

Dual, High-Side, Current-Sense Amplifiers and Drive Amplifiers

General Description

The MAX1350–MAX1357 offer two programmable high-side current-sense amplifiers and two drive amplifiers integrated in a single package.

The current-sense amplifiers have a 5V to 32V common-mode input range and provide a voltage output that is a multiple of the sense voltage. The common-mode input range is independent of supply voltage. An external sense resistor determines the range of current monitored by a current-sense amplifier. Gains of 2 or 10 are available with a typical input-referred offset voltage of zero or 3mV. The 3mV offset option is ideal for applications where offset nulling is required.

The drive amplifiers provide up to ±10mA of output current capability and a high output capacitive load tolerance. Output transients are limited to ±100mV during power-up and power-down events. The drive amplifiers feature a digitally controllable fast output clamp to ground. The drive amplifier outputs are current limited and are offered with gains of 2 or 4.

The drive amplifiers draw approximately 4.75mA, while the current-sense amplifiers draw approximately 250µA with full-scale sense inputs. In shutdown mode, the total supply current reduces to less than 1µA.

The MAX1350–MAX1357 are available in a 20-pin TSSOP package and operate over the extended (-40°C to +85°C) temperature range.

Applications

Cellular Base Stations

Industrial Process Control

Power Amplifiers

Features

- **High-Side Current-Sense Amplifier with Gain of 2 or 10**
- **±1% Current-Sense Accuracy**
- **Wide 5V to 32V Common-Mode Voltage Range—Independent of Supply Voltage**
- **Adjustable Low Noise 0 to 5V or 0 to 10V Output Voltage Ranges with ±10mA Gate Drive**
- **Drive Amplifier Features Fast Clamp to Ground**

Ordering Information

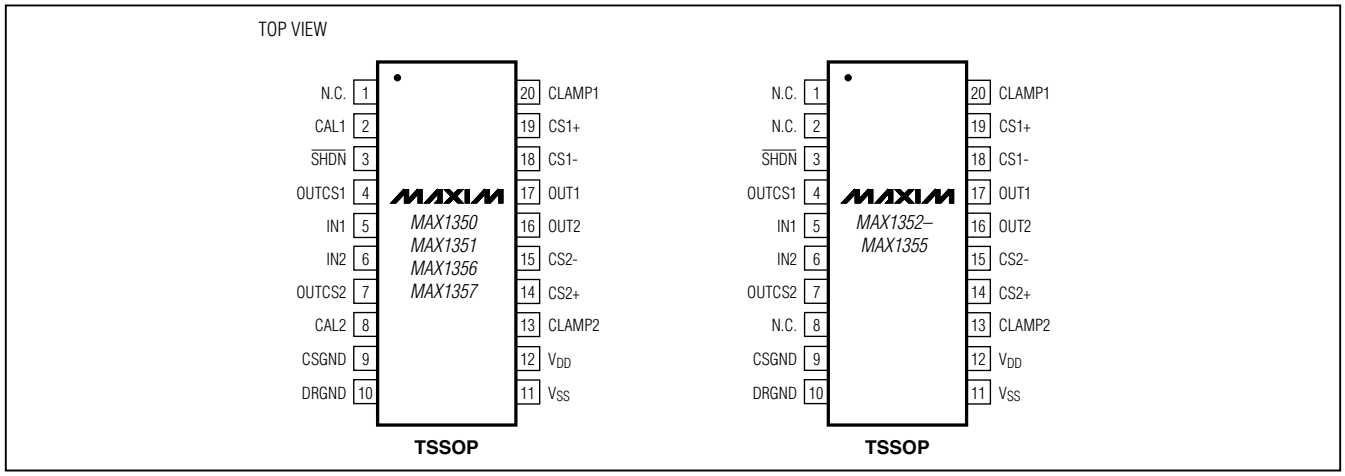
PART	TEMP RANGE**	PIN-PACKAGE
MAX1350EUP*	-40°C to +85°C	20 TSSOP
MAX1351EUP*	-40°C to +85°C	20 TSSOP
MAX1352EUP*	-40°C to +85°C	20 TSSOP
MAX1353EUP*	-40°C to +85°C	20 TSSOP
MAX1354EUP	-40°C to +85°C	20 TSSOP
MAX1355EUP*	-40°C to +85°C	20 TSSOP
MAX1356EUP*	-40°C to +85°C	20 TSSOP
MAX1357EUP*	-40°C to +85°C	20 TSSOP

*Future product—contact factory for availability.

**For parts that operate over a wider temperature range, contact factory for availability.

Selector Guide appears at end of data sheet.

Pin Configurations



Dual, High-Side, Current-Sense Amplifiers and Drive Amplifiers

ABSOLUTE MAXIMUM RATINGS

V_{DD} to V_{SS} .....-0.3V to +14V
V_{SS} to CSGND or DRGND..... -1V to +0.3V
CSGND to DRGND..... -0.3V to +0.3V
CS1+, CS2+ to V_{SS} .....-0.3V to +34V
CS1- to CS1+ ..... -6V to +0.3V
or if CS1+ < 5.7V .....(-CS1 - 0.3)V to +0.3V
CS2- to CS2+ ..... -6V to +0.3V
or if CS2+ < 5.7V .....(-CS2 - 0.3)V to +0.3V
OUT1, OUT2 to V_{SS} .....-0.3 to (V_{DD} + 0.3V)
CAL1, CAL2, $\overline{SHDN}$ to CSGND or DRGND.....-0.3V to +6V
CLAMP1, CLAMP2 to CSGND or DRGND .....-0.3V to +6V
OUTCS1, OUTCS2 to V_{SS} .....-0.3V to +34V
IN1, IN2 to V_{SS}.....-0.3 to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP (derate 11mW/°C above +70°C) 879.1mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +10V, V_{SS} = 0V, V_{CS_+} = 30V, C_{OUTCS1}, C_{OUTCS2} to CSGND = 10pF, C_{OUT1}, C_{OUT2} to DRGND = 10nF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-SIDE CURRENT-SENSE AMPLIFIER						
Operating and Common-Mode Input Voltage Range	V_{CS_+}		5		32	V
Common-Mode Rejection Ratio	CMRR	5V < V_{CS_+} < 32V, measured at DC		110		dB
Current-Sense Negative Input Bias Current	I_{CS-}		-1	±0.1	+1	µA
Input-Referred Offset Voltage	V_{OS}	MAX1352–MAX1355, T_A = +25°C	-0.7	±0.2	+0.7	mV
		MAX1350/MAX1351/MAX1356/MAX1357, T_A = +25°C (Note 1)	2.0	3.0	4.0	
Input-Referred Offset Drift				±2		µV/°C
Full-Scale Sense Voltage Range (Note 2)	V_{SENSE}	MAX1350–MAX1353	2		1250	mV
		MAX1354–MAX1357	2		500	
Total Output Voltage Error (Note 3)		V_{SENSE} = 100mV to 1250mV	-1.0	±0.3	+1.0	%
		V_{SENSE} = 20mV to 100mV	-5	±1.3	+5	
		V_{SENSE} = 2mV to 20mV	-50	±13	+50	
Output Impedance	$R_{OUTCS\_}$	Measured at DC	8.75	12.5	17.25	kΩ
Output Voltage Range (Note 4)	$V_{OUTCS\_}$	MAX1350/MAX1351	0.010		2.506	V
		MAX1352/MAX1353	0.004		2.500	
		MAX1354/MAX1355	0.02		5.00	
		MAX1356/MAX1357	0.05		5.03	
Voltage Gain Error				±0.1		%
-3dB Bandwidth	BW			1.15		MHz
Output Settling Time to 0.1% of Final Value				10		µs
Output Capacitive Load		(Note 5)		10		pF
Input Referred Noise at 1kHz				25		nV/√Hz
Power-Supply Rejection Ratio	PSRR	5V < V_{CS_+} < 32V, measured at DC		110		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +10V, V_{SS} = 0V, V_{CS_+} = 30V, C_{OUTCS1}, C_{OUTCS2} to CSGND = 10pF, C_{OUT1}, C_{OUT2} to DRGND = 10nF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Up Time to 0.1% of Final Value				100		µs
Saturation Recovery Time				100		µs
Shutdown Recovery Time				100		µs
DRIVE AMPLIFIER						
Output Voltage Range for Full Accuracy		At OUT_, $I_{OUT\_}$ = ±10mA	V_{SS} + 1		V_{DD} - 1	V
		At OUT_, $I_{OUT\_}$ = ±0.1mA	V_{SS} + 0.75		V_{DD} - 0.75	
Drive Amplifier Input Bias Current	$I_{IN\_}$	(Note 6)	-20	+2	+20	nA
Output Impedance	$R_{OUT\_}$	Measured at DC		0.1		Ω
Settling Time to 0.1% of Final Value		R_S = 50Ω, $C_{OUT\_}$ = 15µF		10		ms
		R_S = 0Ω, $C_{OUT\_}$ = 10nF		20		µs
Output Capacitive Load	$C_{OUT\_}$		0		10	nF
		50Ω in series with $C_{OUT\_}$	0		25	µF
Input-Referred Noise at 1kHz				20		nV/√Hz
Voltage Gain Error			-0.20	+0.02	+0.20	%
-3dB Bandwidth	BW	MAX1350/MAX1352/MAX1354/MAX1356		300		kHz
		MAX1351/MAX1353/MAX1355/MAX1357		150		
Input-Referred Offset Voltage	V_{OS}		-0.75	±0.25	+0.75	mV
Input-Referred Offset Drift				±2		µV/°C
Common-Mode Rejection Ratio	CMRR	Measured at DC (Note 6)		96		dB
Power-Supply Rejection Ratio	PSRR	Measured at DC (Note 6)		96		dB
Clamp to Zero Delay		CLAMP_ driven high		1		µs
Clamp to Zero Switch Impedance	R_{CLAMP}			300	500	Ω
Output Short-Circuit Current	I_{SC}	1s, sinking or sourcing		±40		mA
Power-Up Time to 0.1% of Final Value				100		µs
Saturation Recovery Time				100		µs
Shutdown Recovery Time				100		µs
Maximum Power-On Transient				±100		mV
DIGITAL INPUTS ($\overline{SHDN}$, CLAMP1, CLAMP2, CAL1, CAL2)						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.4	V
Input Hysteresis				0		mV
Input Bias Current			-1.0	±0.1	+1.0	µA
Input Capacitance				5.0		pF
POWER SUPPLIES						
Drive Supply Voltage	V_{DD}	V_{SS} = DRGND	4.75		11.00	V
Drive Supply Current	I_{DD}	(Note 7)		4.75	7	mA
Sense Supply Voltage Range	V_{CS+}		5		32	V

Dual, High-Side, Current-Sense Amplifiers and Drive Amplifiers

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +10V, V_{SS} = 0V, V_{CS_+} = 30V, C_{OUTCS1}, C_{OUTCS2} to CSGND = 10pF, C_{OUT1}, C_{OUT2} to DRGND = 10nF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Sense Supply Current	I_{CS+}	$V_{OUTCS\_}$ = 200mV		135	195	µA
		$V_{OUTCS\_}$ = 2.5V		320	450	
V_{DD} to V_{SS} Voltage Range	V_{DS}		4.75		11.00	V
V_{SS} to DRGND Voltage Range	V_{SG}		-1		0	V
Shutdown Supply Current		$\overline{SHDN}$ = DRGND (Note 8), T_A = +25°C		0.1	1	µA
		T_A = +85°C		2.5	10	

Note 1: Input deliberately offset by 3mV for nulling purposes.

Note 2: The output does not reverse phase when overdriven. $V_{SENSE} = V_{CS+} - V_{CS-}$.

Note 3: Total output voltage error = (($V_{OUTMEASURED}$ - $V_{OUT-IDEAL}$) / $V_{OUT-IDEAL}$) x 100%
Total output voltage error = ((Total offset voltage error + total gain voltage error) / $V_{OUT-IDEAL}$) x 100%
where:
$V_{OUT-IDEAL}$ = (V_{SENSE} + 3mV) x 2 for the MAX1350/MAX1351
$V_{OUT-IDEAL}$ = V_{SENSE} x 2 for the MAX1352/MAX1353
$V_{OUT-IDEAL}$ = V_{SENSE} x 10 for the MAX1354/MAX1355
$V_{OUT-IDEAL}$ = (V_{SENSE} + 3mV) x 10 for the MAX1356/MAX1357

Note 4: For the MAX1350–MAX1353, the minimum CS_+ to OUTCS_ voltage is 2.494V. For the MAX1354–MAX1357, the minimum CS_+ to OUTCS_ voltage is 2.75V.

Note 5: Adding a capacitor (C_{OUTCS}) to CSGND at OUTCS_ can limit the bandwidth below that of the sense amplifier by introducing a pole at f_{POLE}, where $f_{POLE} = 1 / (2\pi \times R_{OUTCS} \times C_{OUTCS})$. For example, for $R_{OUTCS\_}$ = 12.5kΩ, adding a 100pF capacitor introduces a pole at 127kHz (±40%). This can be of benefit if noise needs to be restricted or the signal digitized.

Note 6: For the MAX1350/MAX1352/MAX1354/MAX1356, the voltage input range is $0.18V \le V_{IN} \le V_{DD} / 2$. For the MAX1351/MAX1353/MAX1355/MAX1357, the voltage input range is $0.18V \le V_{IN} \le V_{DD} / 4$.

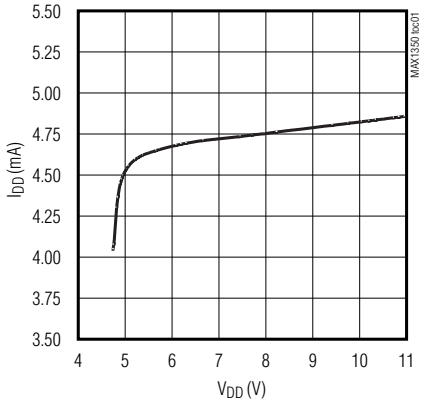
Note 7: Measured with all the digital inputs low, except $\overline{SHDN}$, and no load.

Note 8: All digital inputs low. Any digital input consumes current if left in a high state.

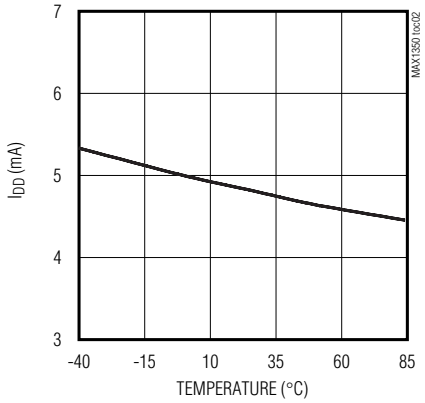
Typical Operating Characteristics

(V_{DD} = 10V, V_{SS} = 0, V_{CS+} = 30V, V_{SENSE} = 100mV, T_A = +25°C, unless otherwise noted.)

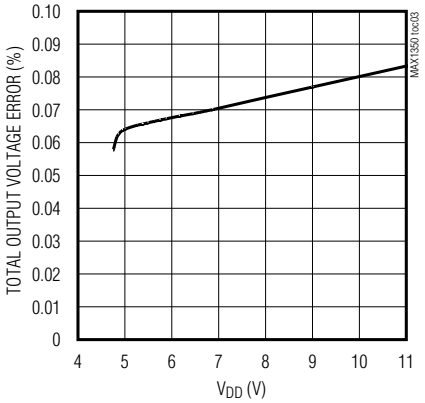
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



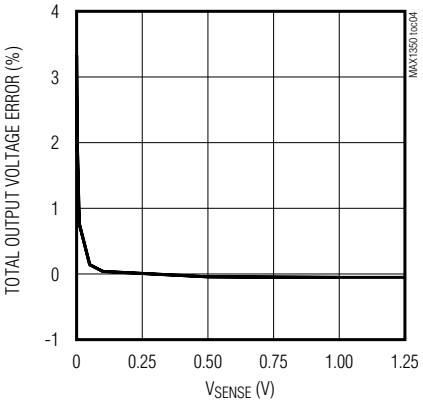
SENSE-AMPLIFIER TOTAL OUTPUT VOLTAGE ERROR vs. SUPPLY VOLTAGE



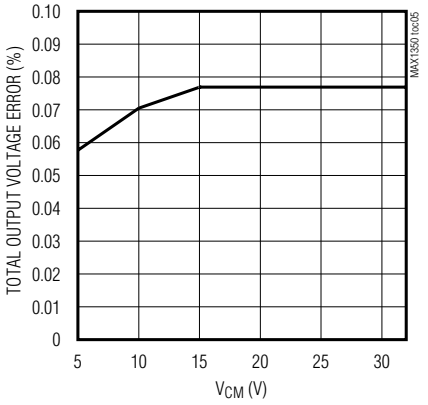
Typical Operating Characteristics (continued)

(V_{DD} = 10V, V_{SS} = 0, V_{CS+} = 30V, V_{SENSE} = 100mV, T_A = +25°C, unless otherwise noted.)

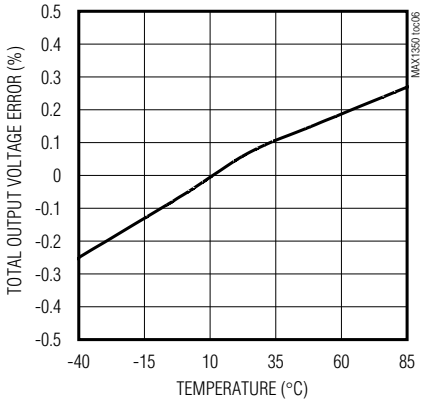
SENSE-AMPLIFIER TOTAL OUTPUT VOLTAGE ERROR vs. SENSE VOLTAGE



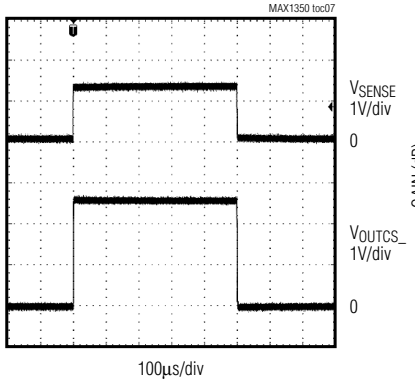
SENSE-AMPLIFIER TOTAL OUTPUT VOLTAGE ERROR vs. COMMON-MODE VOLTAGE



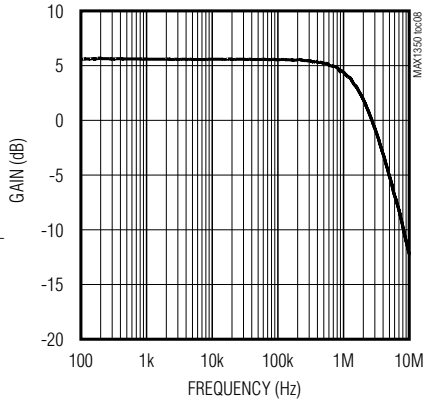
SENSE-AMPLIFIER TOTAL OUTPUT VOLTAGE ERROR vs. TEMPERATURE



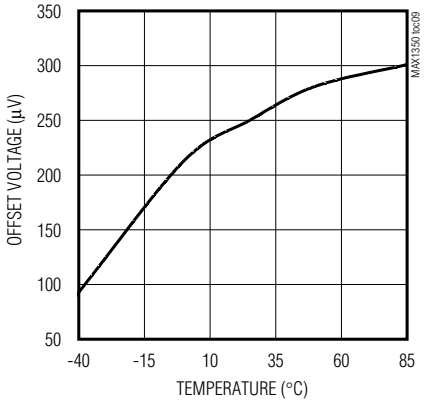
SENSE-AMPLIFIER TRANSIENT RESPONSE



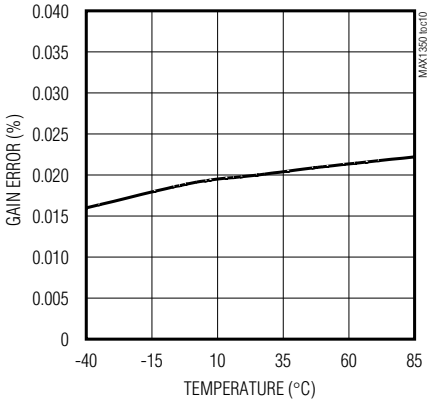
SENSE-AMPLIFIER GAIN vs. FREQUENCY



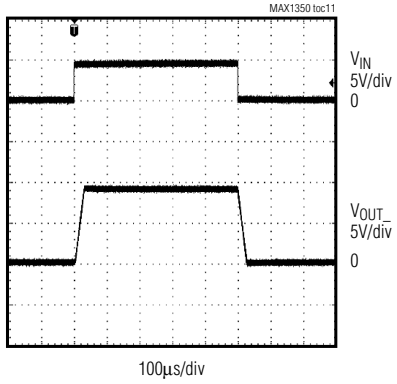
DRIVE-AMPLIFIER OFFSET VOLTAGE vs. TEMPERATURE



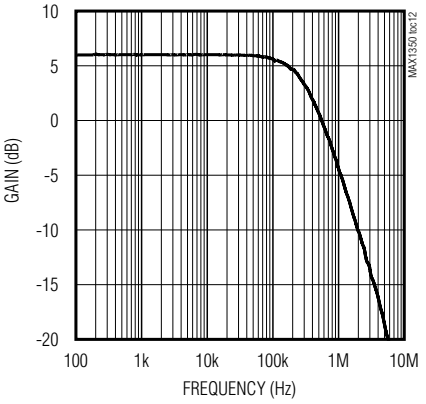
DRIVE-AMPLIFIER GAIN ERROR vs. TEMPERATURE



DRIVE-AMPLIFIER TRANSIENT RESPONSE



DRIVE-AMPLIFIER GAIN vs. FREQUENCY

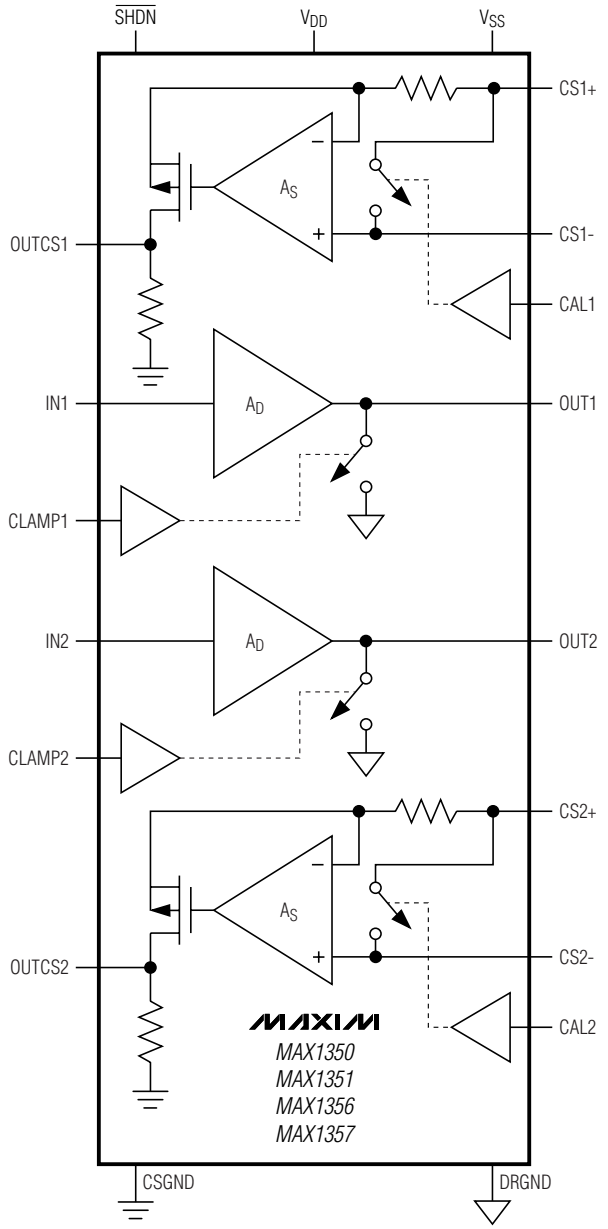


Dual, High-Side, Current-Sense Amplifiers and Drive Amplifiers

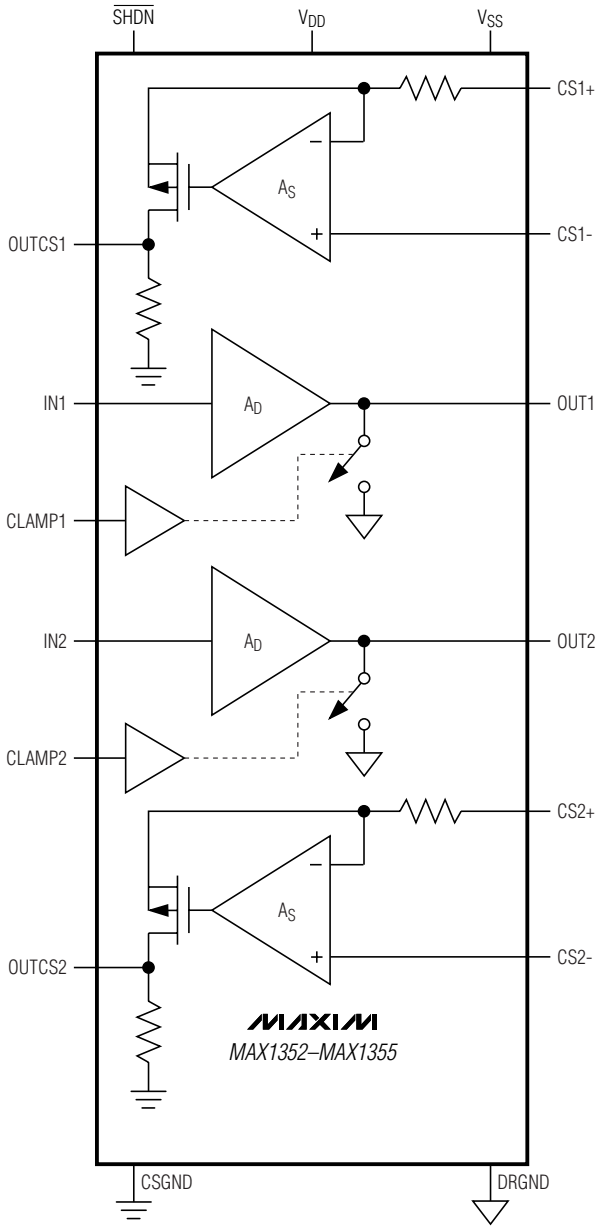
Pin Description

PIN		NAME	FUNCTION
MAX1350 MAX1351 MAX1356 MAX1357	MAX1352–MAX1355		
1	1, 2, 8	N.C.	No Connection. Not internally connected.
2	—	CAL1	Offset Calibration Digital Input 1. Drive CAL1 high to short CS1- to CS1+ for input offset nulling. Drive CAL1 low for normal operation.
3	3	$\overline{SHDN}$	Shutdown Digital Input. Drive $\overline{SHDN}$ low to place device in low-power shutdown. Drive $\overline{SHDN}$ high for normal operation.
4	4	OUTCS1	Current-Sense Amplifier Voltage Output 1. $V_{OUTCS1} = A_S \times (V_{CS1+} - V_{CS1-})$.
5	5	IN1	Drive Amplifier 1 Input
6	6	IN2	Drive Amplifier 2 Input
7	7	OUTCS2	Current-Sense Amplifier Voltage Output 2. $V_{OUTCS2} = A_S \times (V_{CS2+} - V_{CS2-})$.
8	—	CAL2	Offset Calibration Input 1. Drive CAL2 high to short CS2- to CS2+ for input offset nulling. Drive CAL2 low for normal operation.
9	9	CSGND	Current-Sense Ground. Ground reference for the current-sense amplifier outputs.
10	10	DRGND	Drive Amplifier Ground. Ground reference for the drive amplifier outputs and digital inputs.
11	11	V_{SS}	Negative Drive Power Input. Bypass with a 0.1µF capacitor to DRGND.
12	12	V_{DD}	Positive Drive Power Input. Bypass with a 0.1µF capacitor to DRGND.
13	13	CLAMP2	Output 2 Clamp Control Input. Drive CLAMP2 high to clamp OUT2 to DRGND. Drive CLAMP2 low for normal operation.
14	14	CS2+	Current-Sense Positive Input 2/Sense-Amplifier Power Input. CS2+ is the power connection to the external sense resistor and supplies power to the sense amplifier. For normal operation of the MAX1350–MAX1357, CS1+ and CS2+ must both be in the specified common-mode range.
15	15	CS2-	Current-Sense Negative Input 2. CS2- is the load connection to the external sense resistor. See the typical operating circuit.
16	16	OUT2	Drive Amplifier 2 Output. $V_{OUT2} = A_D \times V_{IN2}$.
17	17	OUT1	Drive Amplifier 1 Output. $V_{OUT1} = A_D \times V_{IN1}$.
18	18	CS1-	Current-Sense Negative Input 1. CS1- is the load connection to the external sense resistor. See the typical operating circuit.
19	19	CS1+	Current-Sense Positive Input 1/Sense-Amplifier Power Input. CS1+ is the power connection to the external sense resistor and supplies power to the sense amplifier. For normal operation of the MAX1350–MAX1357, CS1+ and CS2+ must be in the specified common-mode range.
20	20	CLAMP1	Output 1 Clamp Control Input. Drive CLAMP1 high to clamp OUT1 to DRGND. Drive CLAMP1 low for normal operation.

Functional Diagrams



A_S: SENSE-AMPLIFIER VOLTAGE GAIN
A_S = 2 FOR THE MAX1350/MAX1351
A_S = 10 FOR THE MAX1356/MAX1357
A_D: DRIVE-AMPLIFIER VOLTAGE GAIN
A_D = 2 FOR THE MAX1350/MAX1356
A_D = 4 FOR THE MAX1351/MAX1357



A_S: SENSE-AMPLIFIER VOLTAGE GAIN
A_S = 2 FOR THE MAX1352/MAX1353
A_S = 10 FOR THE MAX1354/MAX1355
A_D: DRIVE-AMPLIFIER VOLTAGE GAIN
A_D = 2 FOR THE MAX1352/MAX1354
A_D = 4 FOR THE MAX1353/MAX1355

Dual, High-Side, Current-Sense Amplifiers and Drive Amplifiers

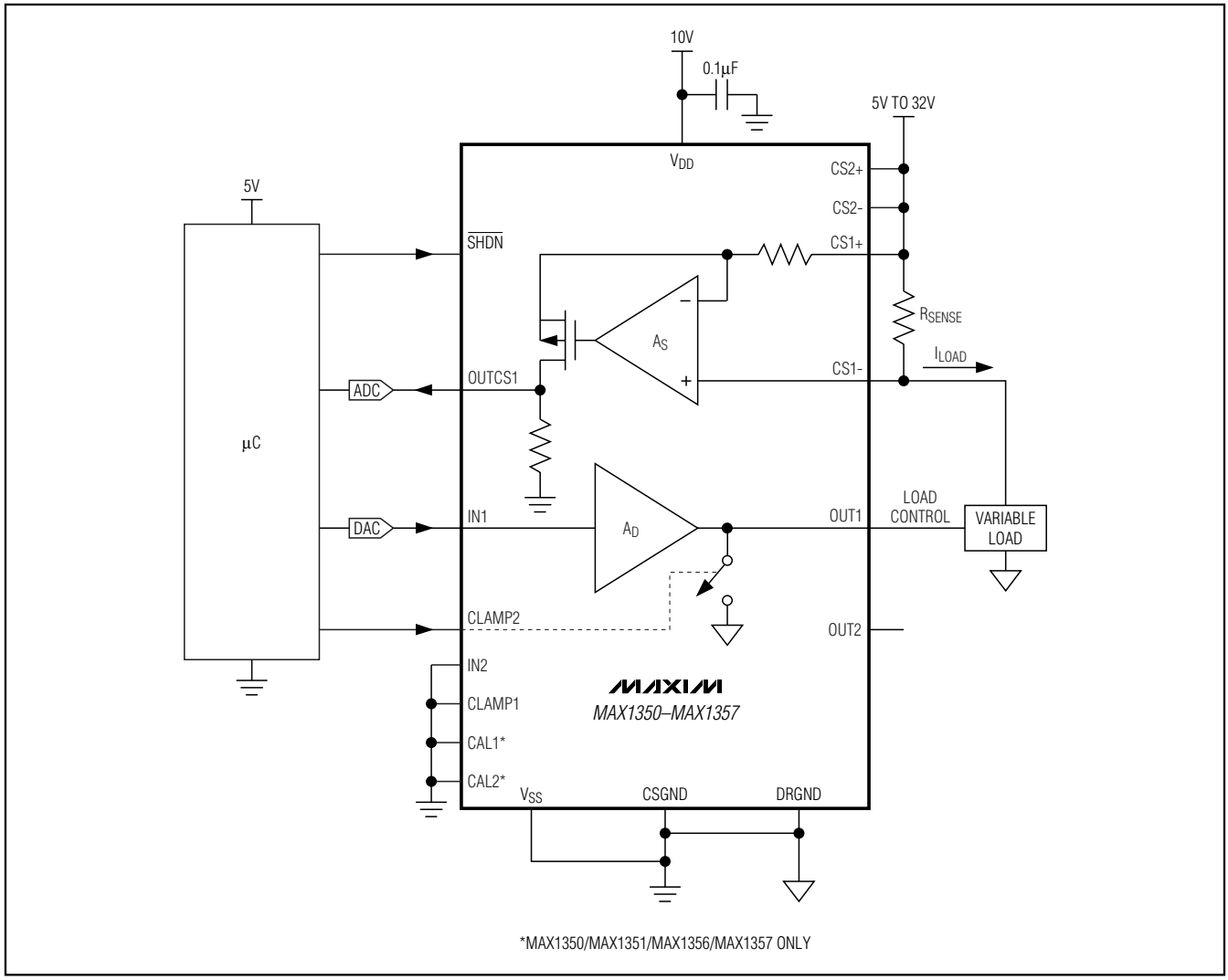


Figure 1. Typical Operating Circuit

Detailed Description

Each of the MAX1350–MAX1357 parts includes two high-side current-sense amplifiers and two drive amplifiers. The current-sense amplifiers are unidirectional and provide a 5V to 32V input common-mode range. For normal operation, the device requires a 4.75V to 11V supply at V_{DD} and a 5V to 32V supply at CS1+ and CS2+. Both CS1+ and CS2+ must be within the specified common-mode range for proper operation of all amplifiers. The CS1+ and CS2+ inputs function as power inputs to the sense amplifier and each typically draws 320µA with a full-scale sense voltage (see the *Electrical Characteristics*).

Current-Sense Amplifiers

The sense amplifiers measure the load current, I_{LOAD}, through an external sense resistor, R_{SENSE}, between the CS_+ and CS_- inputs. The sense voltage range ($V_{SENSE} = V_{CS\_+} - V_{CS\_-}$) is between 2mV and 1250mV for the MAX1350–MAX1353 and between 2mV and 500mV for the MAX1354–MAX1357. The sense amplifiers provide a voltage output at OUTCS1 and OUTCS2, where the output voltage is determined by the following equation:

$$V_{OUTCS\_} = A_S \times (V_{CS\_+} - V_{CS\_-})$$

Offset Calibration (CAL1 and CAL2)

The MAX1350/MAX1351/MAX1356/MAX1357 offer a typical input offset voltage of 3mV for systems requiring offset nulling. For the MAX1352–MAX1355, where the nominal input offset voltage is 0, only positive offset is detectable since the output cannot go below ground. With the deliberate input offset voltage of 3mV, the output offset voltage (A_S x 3mV) can be easily nulled using external circuitry. Nulling out the sense-amplifier offset significantly improves the total output voltage error at sense voltages below 100mV.

Drive CAL_ high to short CS_+ and CS_- together to measure the offset at OUTCS_. Drive CAL_ low for normal operation. The width of the CAL_ pulse should be greater than 40µs. Sample OUTCS1/OUTCS2 until 40µs after the digital inputs have gone low.

Drive Amplifiers

The MAX1350–MAX1357 include dual drive amplifiers with an internally fixed gain (A_D) of 2 for the MAX1350/MAX1352/MAX1354/MAX1356 and 4 for the MAX1351/MAX1353/MAX1355/MAX1357.

Output Clamp to DRGND (CLAMP1 and CLAMP2)

The MAX1350–MAX1357 offer an output clamp feature for the drive amplifiers. Drive CLAMP1 and CLAMP2 high to clamp OUT1 and OUT2 respectively to DRGND. The CLAMP_ high to OUT_ low delay is typically 1µs (see the *Electrical Characteristics*). Drive CLAMP1 and CLAMP2 low for normal operation.

Power-On Reset

After a power-on reset, the MAX1350–MAX1357 are in shutdown regardless of the state of $\overline{SHDN}$. Toggle $\overline{SHDN}$ (provide a low-to-high transition) to take the device out of shutdown mode. $\overline{SHDN}$ then continues to function as a level-triggered, active-low input. Drive $\overline{SHDN}$ high for normal operation.

Digital Inputs ($\overline{SHDN}$, CLAMP1, CLAMP2, CAL1, CAL2)

Drive the digital inputs with 3.3V or 5V logic. The absolute maximum voltage that can be applied to these inputs is 6V.

Unused Devices

Figure 1 illustrates an example in which the MAX1350–MAX1357 facilitate current control to a variable load. If using only one of the current-sense amplifiers, connect CS_+ and CS_- of the unused amplifier to the same point as CS_+ of the active sense amplifier. This ensures that the unused CS_+ input resides in the common-mode range for proper operation, and the amplifier output is zero since CS_+ and CS_- are shorted together. For an unused drive amplifier, connect the input (IN_) to DRGND and drive the associated CLAMP_ high to force the outputs to DRGND.

Applications Information

Application Example—Base-Station LDMOS Bias

The MAX1350–MAX1357 can be used to sense and control the drain current in an LDMOS transistor in base-station applications (see Figure 2). As the temperature of the LDMOS changes, the gate-to-source threshold voltage changes, resulting in an increase or decrease in drain current if the gate bias voltage is fixed. The MAX1350–MAX1357 allow for a software-controllable scheme to sense the LDMOS drain current and adjust the gate bias voltage to compensate for the temperature shift.

The circuit in Figure 2 can control up to eight LDMOS transistors when using four MAX1350–MAX1357 devices. The MAX1230 is a 12-bit, 16-channel ADC, which processes up to eight drain current measurements and eight LDMOS temperature measurements (one for each transistor). The MAX5306 is a 12-bit, octal DAC, which controls up to eight gate-drive amplifiers. The digital inputs are controlled using a 5V microcontroller.

Current-Sense Resistor Selection

Select R_{SENSE} based on the following criteria:

1) Voltage Loss: A high R_{SENSE} value causes the power-source voltage to degrade through I^2R loss. For minimal voltage loss, use the lowest possible R_{SENSE} value.
2) Accuracy: A high R_{SENSE} value allows lower currents to be measured more accurately. This is because offsets become less significant when the sense voltage is larger.
3) Efficiency and Power Dissipation: At high current levels, the I^2R losses in R_{SENSE} can be significant. Take this into consideration when choosing the resistor value and its power-dissipation rating. Also, the sense resistor's value can drift if it is allowed to heat up excessively.
4) Inductance: Keep inductance low if the current being sensed has a large high-frequency component. Wire-wound resistors have the highest inductance, while metal film is somewhat better. Low-inductance metal-film resistors are also available. Instead of being spiral wrapped around a core, as in metal-film or wire-wound resistors, low-inductance metal film resistors are a straight band of metal and are available in values under 1Ω.

Dual, High-Side, Current-Sense Amplifiers and Drive Amplifiers

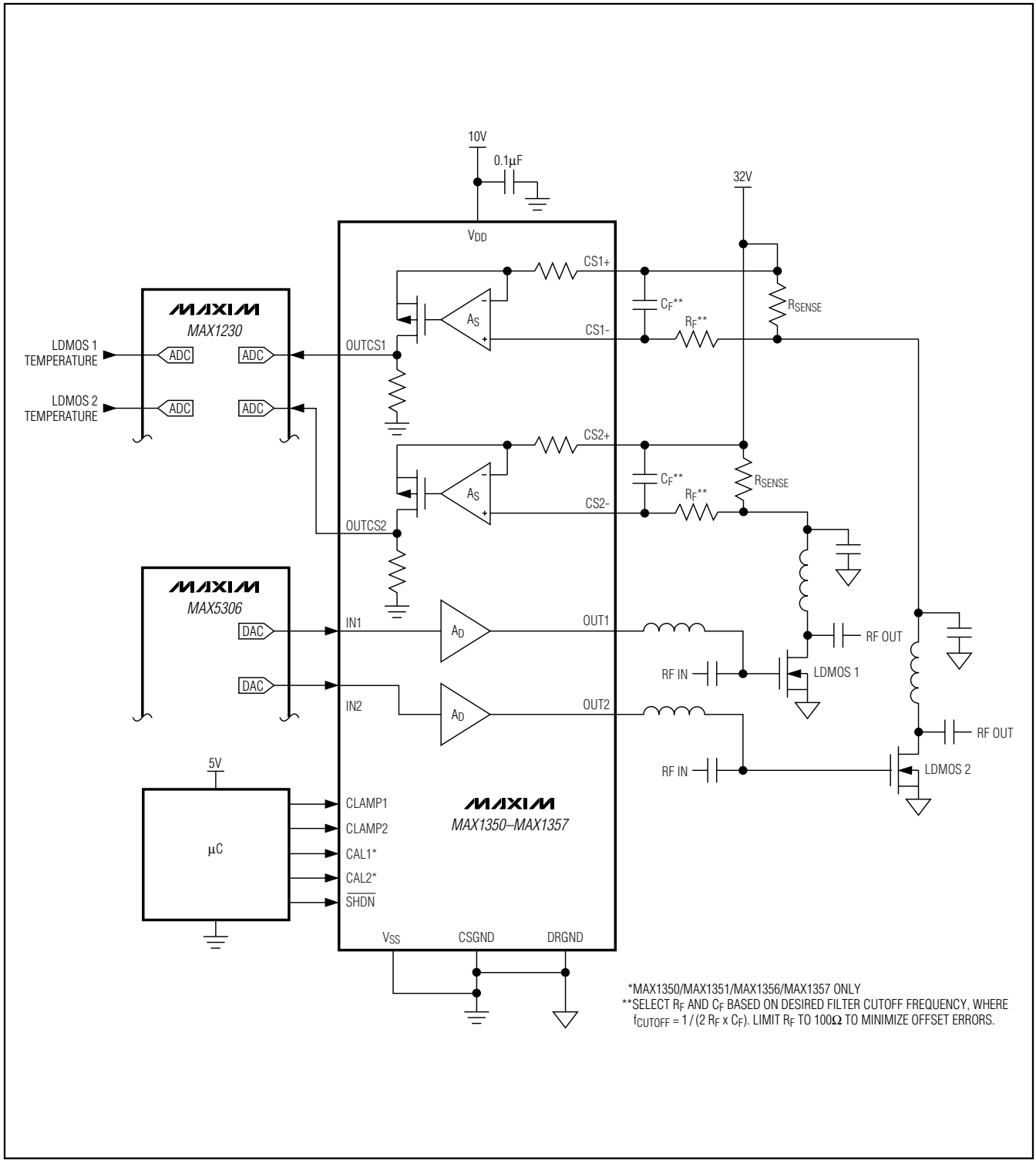


Figure 2. LDMOS Biasing Application

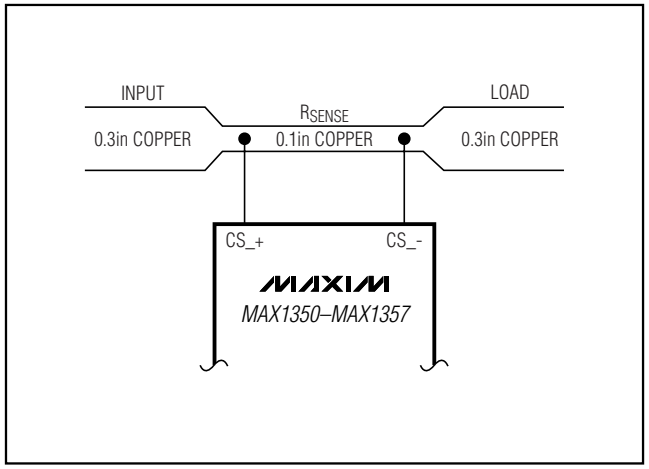


Figure 3. Using PC Board Trace for R_{SENSE}

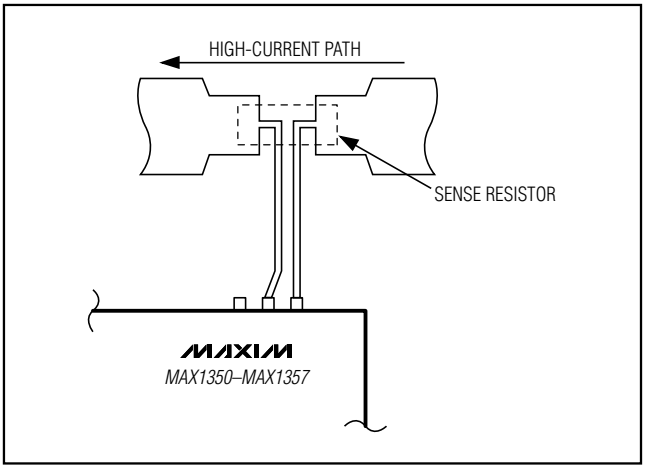


Figure 4. Kelvin Connects for Sense Resistors

5) Cost: If the cost of R_{SENSE} is an issue, it may be preferable to use an alternative solution, as shown in Figure 3. This solution uses the PC board traces to create a sense resistor. Because of the inaccuracies of the copper resistor, the full-scale current value must be adjusted with a potentiometer. Also, copper's resistance temperature coefficient is relatively high (approximately 0.4%/°C).

Using a PC Board Trace to Create a Sense Resistor

In Figure 3, assume that the load current to be measured is 10A using a 0.3in-wide, 2oz copper trace. The resistance of 0.1in-wide, 2oz (70µm thickness) copper is 30mΩ/ft. For 10A, select R_{SENSE} = 5mΩ for a 50mV drop at full scale. This resistor requires approximately 2in of 0.1in-wide copper trace.

Selector Guide

PART	SENSE-AMPLIFIER GAIN (A_S)	SENSE-AMPLIFIER INPUT OFFSET VOLTAGE (mV)	DRIVE-AMPLIFIER GAIN (A_D)
MAX1350	2	3	2
MAX1351	2	3	4
MAX1352	2	0	2
MAX1353	2	0	4
MAX1354	10	0	2
MAX1355	10	0	4
MAX1356	10	3	2
MAX1357	10	3	4

High-Current Measurement

The MAX1350–MAX1357 can achieve high-current measurements by using low-value sense resistors, which can be paralleled to further increase the current-sense limit (see Figure 3). As an alternative, PC board traces can be adjusted over a wide range. Minimize the trace length and ensure accurate sensing with Kelvin connections (see Figure 4).

Power Supply Bypassing and Layout Considerations

Bypass V_{DD} and V_{SS} to DRGND each with at least a 0.1µF ceramic capacitor as close to pins as possible to isolate the device for supply-voltage transients. Bypass CS1+ and CS2+ to CSGND each with at least a 0.1µF ceramic capacitor as close to the pins as possible. For optimum performance, separate the CSGND and DRGND planes. Use a star-ground configuration and connect the two ground planes together through a low-value resistor.

Chip Information

TRANSISTOR COUNT: 804

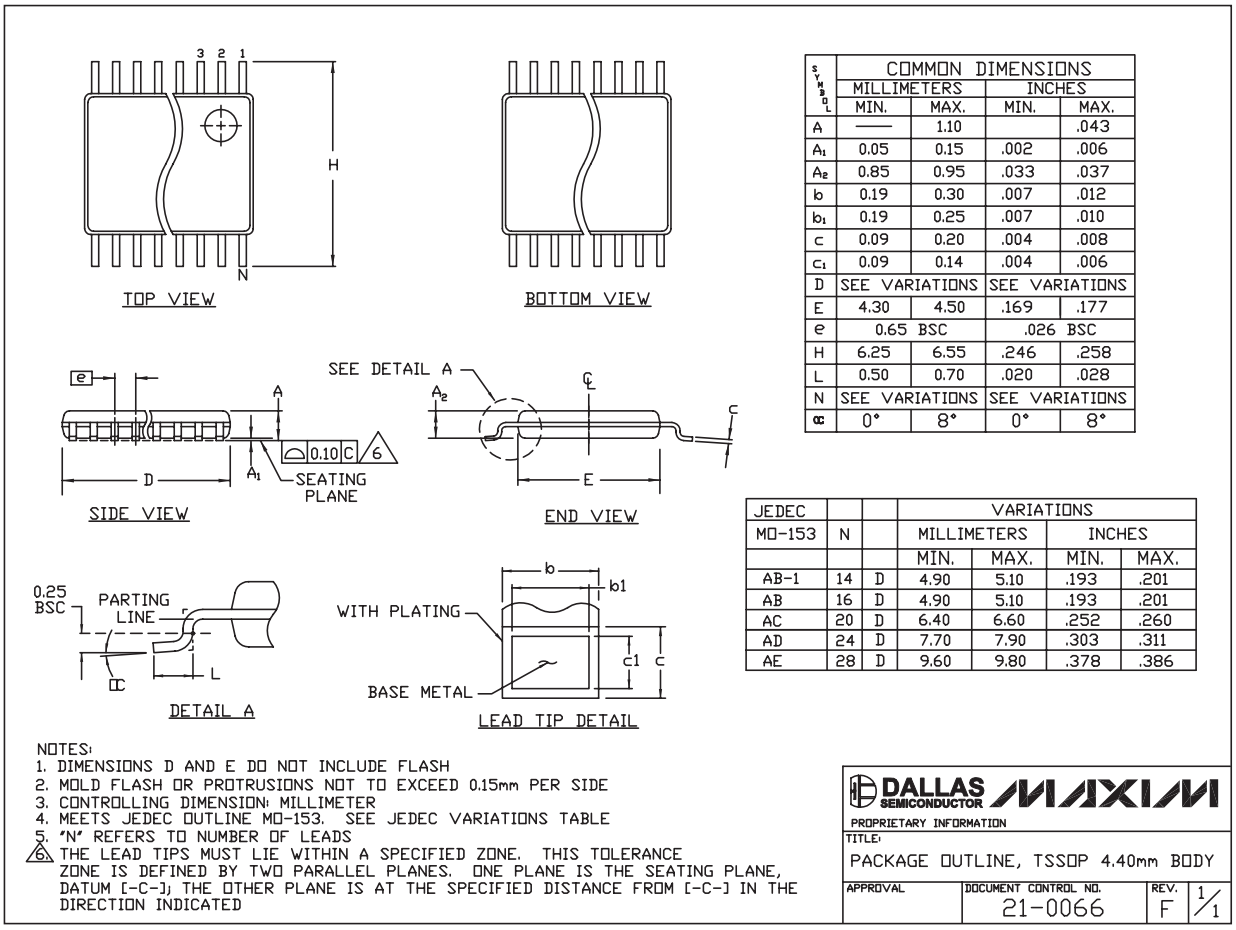
PROCESS: BiCMOS

Dual, High-Side, Current-Sense Amplifiers and Drive Amplifiers

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-], THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1