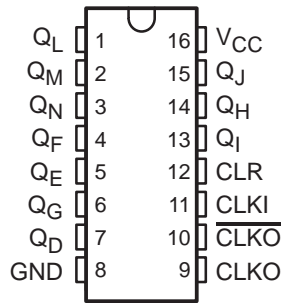


SN54HC4060, SN74HC4060 14-STAGE ASYNCHRONOUS BINARY COUNTERS AND OSCILLATORS

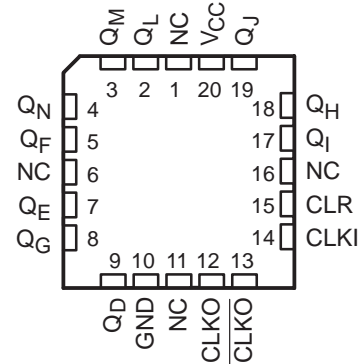
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- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 14$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Allow Design of Either RC- or Crystal-Oscillator Circuits

SN54HC4060 . . . J OR W PACKAGE
SN74HC4060 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC4060 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'HC4060 devices consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC- or crystal-oscillator circuits. A high-to-low transition on the clock ($CLKI$) input increments the counter. A high level at the clear (CLR) input disables the oscillator ($CLKO$ goes high and $CLKO$ goes low) and resets the counter to zero (all Q outputs low).

ORDERING INFORMATION

| TA | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| -40°C to 85°C | PDIP – N | Tube of 25 | SN74HC4060N | SN74HC4060N |
| | SOIC – D | Tube of 40 | SN74HC4060D | HC4060 |
| | | Reel of 2500 | SN74HC4060DR | |
| | | Reel of 250 | SN74HC4060DT | |
| | SOP – NS | Reel of 2000 | SN74HC4060NSR | HC4060 |
| | SSOP – DB | Reel of 2000 | SN74HC4060DBR | HC4060 |
| | TSSOP – PW | Tube of 90 | SN74HC4060PW | HC4060 |
| Reel of 2000 | | SN74HC4060PWR | | |
| Reel of 250 | | SN74HC4060PWT | | |
| -55°C to 125°C | CDIP – J | Tube of 25 | SNJ54HC4060J | SNJ54HC4060J |
| | CFP – W | Tube of 150 | SNJ54HC4060W | SNJ54HC4060W |
| | LCCC – FK | Tube of 55 | SNJ54HC4060FK | SNJ54HC4060FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

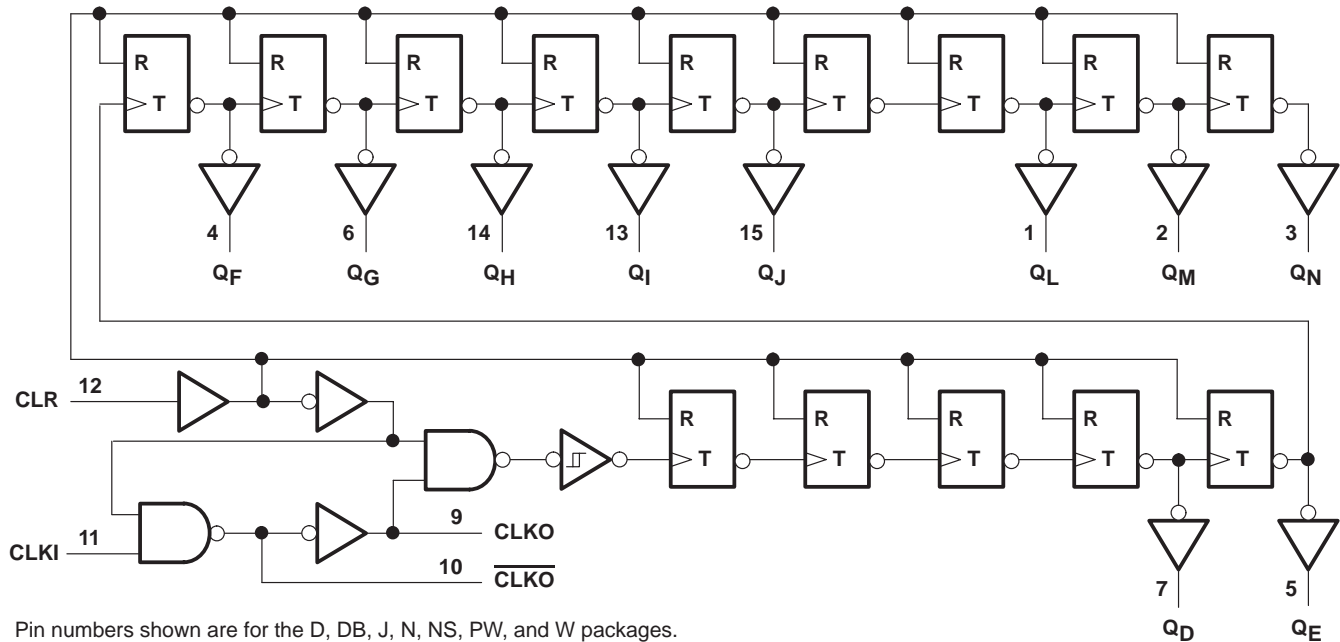
SN54HC4060, SN74HC4060 14-STAGE ASYNCHRONOUS BINARY COUNTERS AND OSCILLATORS

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FUNCTION TABLE
(each buffer)

| INPUTS | | FUNCTION |
|--------|-----|-----------------------|
| CLK | CLR | |
| ↑ | L | No change |
| ↓ | L | Advance to next stage |
| X | H | All outputs L |

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ± 20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ± 20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 25 mA |
| Package thermal impedance, θ_{JA} (see Note 2): | |
| D package | 73°C/W |
| DB package | 82°C/W |
| N package | 67°C/W |
| NS package | 64°C/W |
| PW package | 108°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

| | | SN54HC4060 | | | SN74HC4060 | | | UNIT |
|-----------------|---------------------------------|-------------------------|-----|-----------------|------------|-----------------|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 2 | 5 | 6 | 2 | 5 | 6 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | | 1.5 | 1.5 | | V | |
| | | V _{CC} = 4.5 V | | 3.15 | 3.15 | | | |
| | | V _{CC} = 6 V | | 4.2 | 4.2 | | | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | | | 0.5 | 0.5 | V | |
| | | V _{CC} = 4.5 V | | | 1.35 | 1.35 | | |
| | | V _{CC} = 6 V | | | 1.8 | 1.8 | | |
| V _I | Input voltage | 0 | | V _{CC} | 0 | V _{CC} | V | |
| V _O | Output voltage | 0 | | V _{CC} | 0 | V _{CC} | V | |
| Δt/Δv | Input transition rise/fall time | V _{CC} = 2 V | | | 1000 | 1000 | ns | |
| | | V _{CC} = 4.5 V | | | 500 | 500 | | |
| | | V _{CC} = 6 V | | | 400 | 400 | | |
| T _A | Operating free-air temperature | -55 | | 125 | -40 | 85 | °C | |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | V _{CC} | T _A = 25°C | | | SN54HC4060 | | SN74HC4060 | | UNIT |
|---------------------------|---|--|--|-------------------------|-----------------------|-------|------|------------|-------|------------|-------|------|
| | | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | All outputs | V _I = V _{IH} or V _{IL} , I _{OH} = -20 μA | | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | V | |
| | | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | Q outputs | V _I = V _{IH} or V _{IL} | | I _{OH} = -4 mA | 4.5 V | 3.98 | 4.3 | | 3.7 | | | 3.84 |
| I _{OH} = -5.2 mA | | | | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| V _{OL} | All outputs | V _I = V _{IH} or V _{IL} , I _{OL} = 20 μA | | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | Q outputs | V _I = V _{IH} or V _{IL} | | I _{OL} = 4 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | | |
| I _{OL} = 5.2 mA | | | | 6 V | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| I _I | V _I = V _{CC} or 0 | | | 6 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | | | 6 V | | | 8 | | 160 | | 80 | μA |
| C _i | | | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | pF |



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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | V _{CC} | T _A = 25°C | | SN54HC4060 | | SN74HC4060 | | UNIT |
|--------------------|---------------------------------------|------------------|-----------------------|-----|------------|-----|------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | 2 V | 5.5 | | 3.7 | | 4.3 | | MHz |
| | | 4.5 V | 28 | | 19 | | 22 | | |
| | | 6 V | 33 | | 22 | | 25 | | |
| t _w | Pulse duration | CLKI high or low | 2 V | 90 | 135 | | 115 | | ns |
| | | | 4.5 V | 18 | 27 | | 23 | | |
| | | | 6 V | 15 | 23 | | 20 | | |
| | CLR high | 2 V | 90 | 135 | | 115 | | | |
| | | 4.5 V | 18 | 27 | | 23 | | | |
| | | 6 V | 15 | 23 | | 20 | | | |
| t _{su} | Setup time, CLR inactive before CLKI↓ | 2 V | 160 | 240 | | 200 | | ns | |
| | | 4.5 V | 32 | 48 | | 40 | | | |
| | | 6 V | 27 | 41 | | 34 | | | |

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | T _A = 25°C | | | SN54HC4060 | | SN74HC4060 | | UNIT |
|------------------|--------------|----------------|-----------------|-----------------------|-----|-----|------------|-----|------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f _{max} | | | 2 V | 5.5 | 10 | | 3.7 | | 4.3 | MHz | |
| | | | 4.5 V | 28 | 45 | | 19 | | 22 | | |
| | | | 6 V | 33 | 53 | | 22 | | 25 | | |
| t _{pd} | CLKI | Q _D | 2 V | | 240 | 490 | | 735 | | 615 | ns |
| | | | 4.5 V | | 58 | 98 | | 147 | | 123 | |
| | | | 6 V | | 42 | 83 | | 125 | | 105 | |
| t _{PHL} | CLR | Any Q | 2 V | | 66 | 140 | | 210 | | 175 | ns |
| | | | 4.5 V | | 18 | 28 | | 42 | | 35 | |
| | | | 6 V | | 14 | 24 | | 36 | | 30 | |
| t _t | | Any | 2 V | | 28 | 75 | | 110 | | 95 | ns |
| | | | 4.5 V | | 8 | 15 | | 22 | | 19 | |
| | | | 6 V | | 6 | 30 | | 19 | | 16 | |

operating characteristics, T_A = 25°C

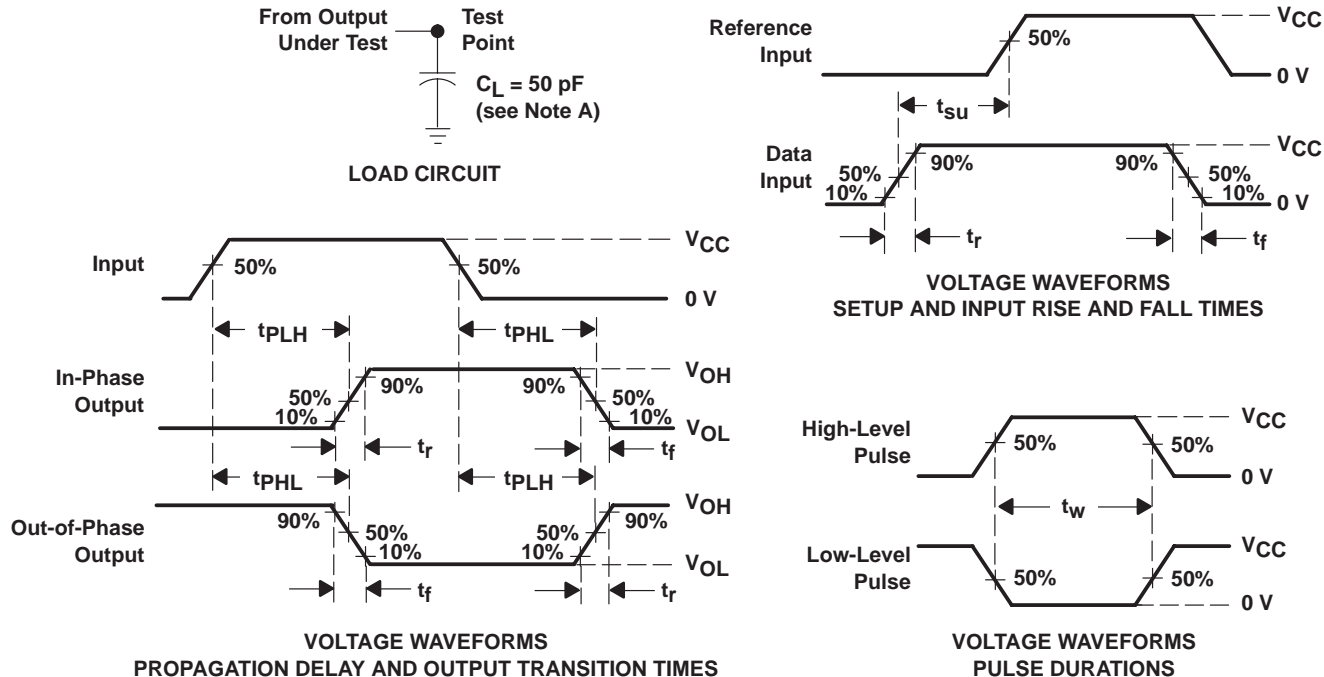
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------------|-------------------------------|-----------------|-----|------|
| C _{pd} | Power dissipation capacitance | No load | 88 | pF |



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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

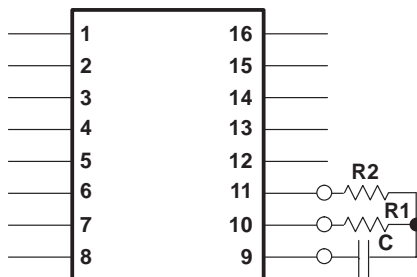
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CONNECTING AN RC-OSCILLATOR CIRCUIT TO THE 'HC4060 DEVICES

The 'HC4060 devices consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC- or crystal-oscillator circuits.

When an RC-oscillator circuit is implemented, two resistors and a capacitor are required. The components are attached to the terminals as shown:



To determine the values of capacitance and resistance necessary to obtain a specific oscillator frequency (f), use this formula:

$$f = \frac{1}{2(R1)(C)\left(\frac{0.405 R2}{R1 + R2} + 0.693\right)}$$

If $R2 \gg R1$ (i.e., $R2 = 10R1$), the above formula simplifies to:

$$f = \frac{0.455}{RC}$$

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



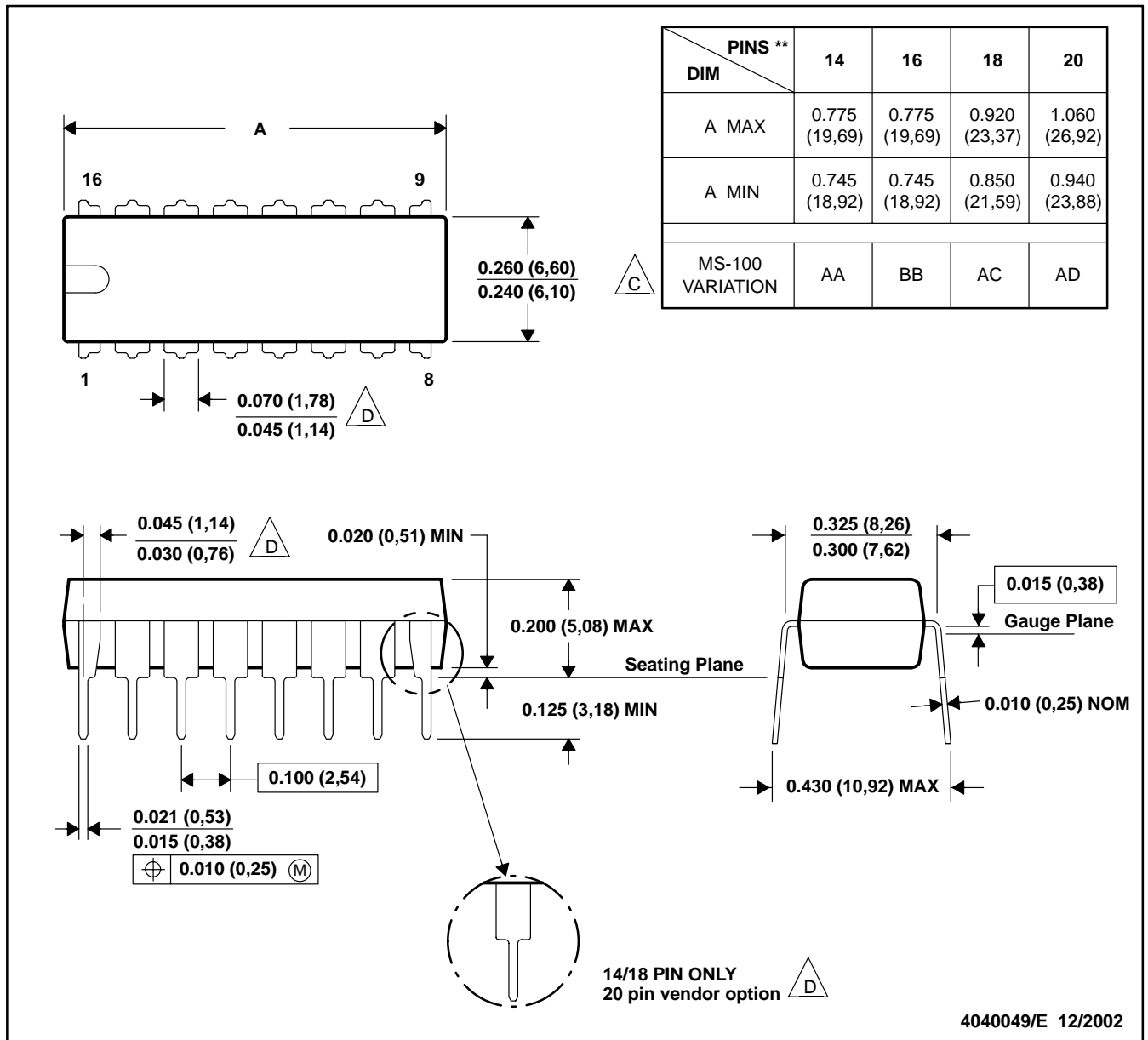
4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 D The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN

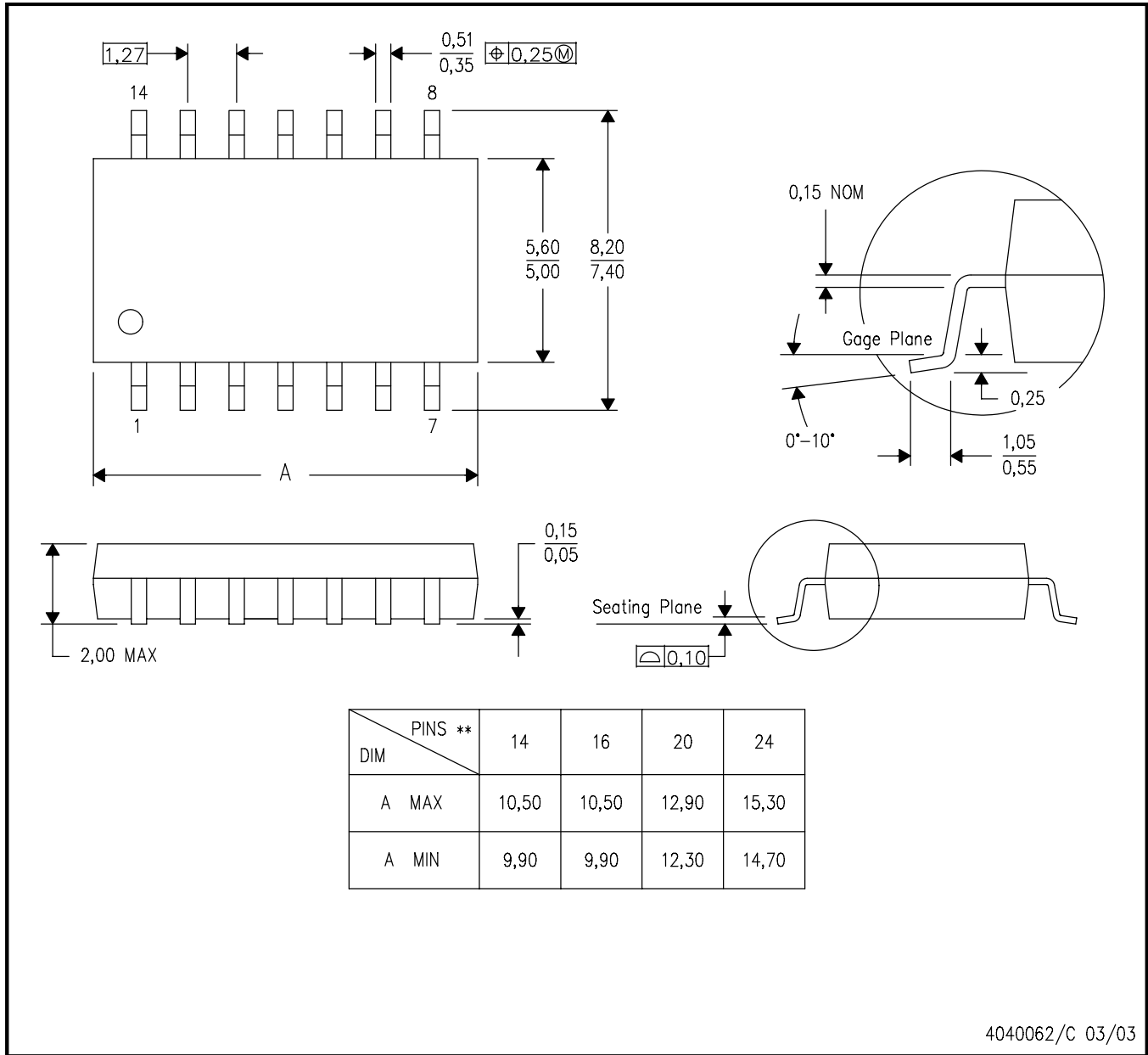


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G)**
14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

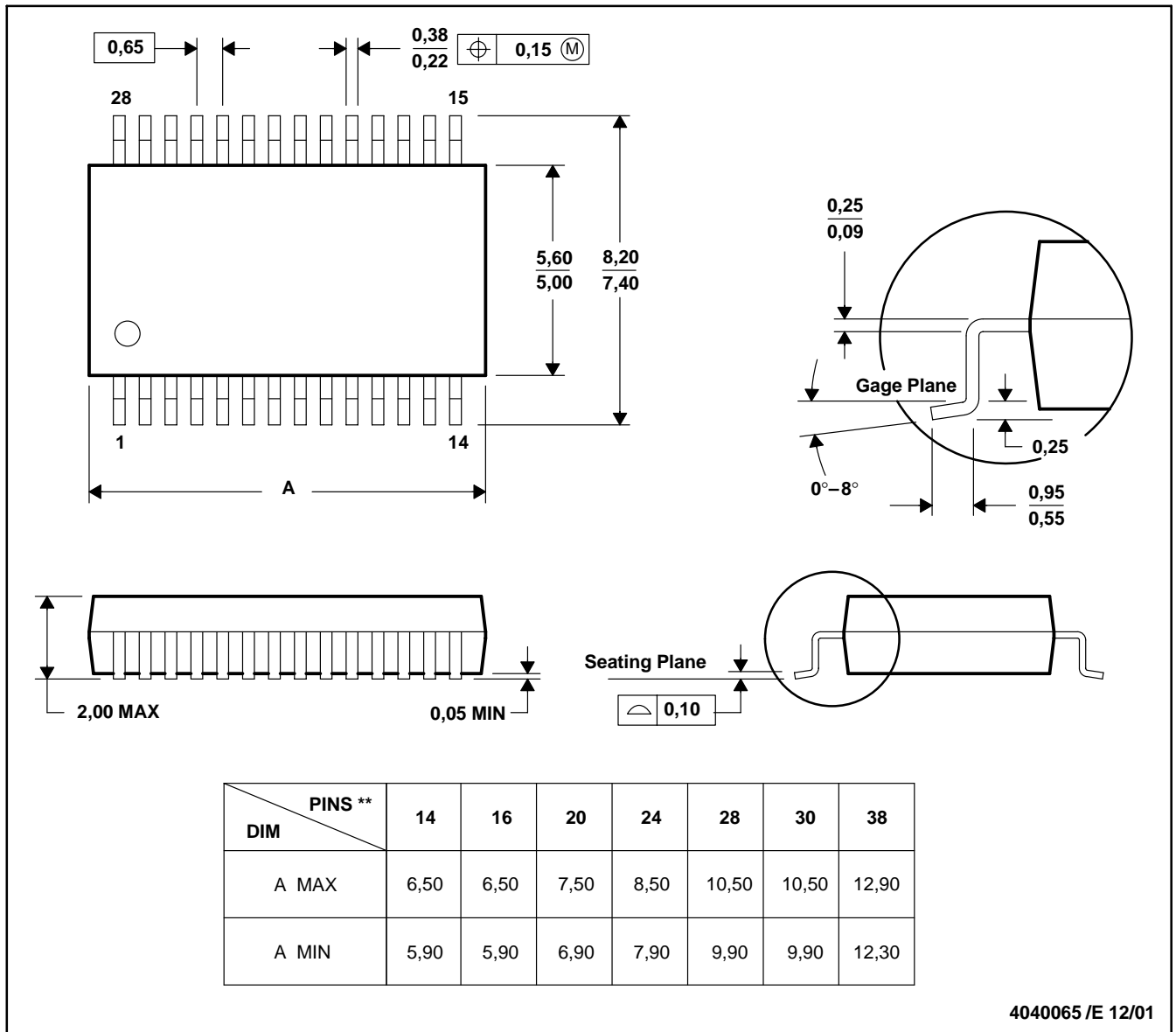


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

4040065 / E 12/01

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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