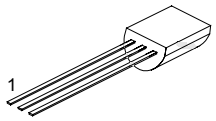
UTC XL/ML1225 SCR

DESCRIPTION

The XL1225/ML1225 silicon controlled rectifiers are high performance planner diffused PNPN devices. These parts are intended for low cost high volume applications.



TO-92

1:CATHODE 2:GATE 3:ANODE

ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise specified)

PARAMETERS	PART NO.	SYMBOL	TEST CONDITION	MIN. RATING	MAX. RATING	UNITS
Repetitive Peak Off-State Voltage	XL1225 ML1225	V_{DRM} V_{DRM}	Tj=40 to 125°C (rgk=1kΩ)	400 300		V
On-State Current		IT(RMS)	Tc=40°C	0.8		A
Average On-State Current		IT(AV)	Half Cycle=180, Tc=40°C	0.5		A
Peak Reverse Gate Voltage		V_{GRM}	IGR=10uA	1		V
Peak Gate Current		IGM	10us Max.	0.1		A
Gate Dissipation		PG(AV)	20ms Max.	150		mW
Operating Temperature		Tj		-40	125	°C
Storage Temperature		T_{STG}		-40	125	°C
Soldering Temperature		T_{SLD}	1.6mm from case 10s Max.		250	°C

ELECTRICAL CHARACTERISTICS (Ta=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Off state leakage current	I_{DRM}	@$V_{DRM(RGK=1K\Omega)}$, Tj=125°C		0.1	mA
Off state leakage current	I_{DRM}	@$V_{DRM(RGK=1K\Omega)}$, Tj=25°C		1.0	μA
On state voltage	VT	AT IT=0.4A AT IT=0.8A		1.4 2.2	V
On state threshold voltage	VT(TO)	Tj=125°C		0.95	V
On state slops resistance	Rt	Tj=125°C		600	m
Gate trigger current	IGT	VD=7V		200	μA
Gate trigger voltage	VGT	VD=7V		0.8	V
Holding current	IH	RGK=1KΩ		5	mA
Latching current	IL	RGK=1KΩ		6	mA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Critical rate of voltage rise	DV/DT	VD=0.67*VDRM(RGK=1KΩ), Tj=125°C			V/μs
Critical rate of current rise	DV/DT	IG=10mA, dIG/dt=0.1A/μs, Tj=125°C			A/μs
Gate controlled delay time	TGD	IG=10mA, dIG/dt=0.1A/μs,		2.2	μs
Commutated turn-off time	TG	Tj=85°C, VD=0.67*VDRM, VR=35V, IT=IT(AV)		200	μs
Thermal resistance junc. to case	Rθ JC				K/W
Thermal resistance junc. to case	Rθ JA				K/W

CLASSIFICATION OF I_{GT}

RANK	B	C	AA	AB	AC	AD
RANGE	50-100μA	100-200μA	8-15μA	15-20μA	20-25μA	25-50μA

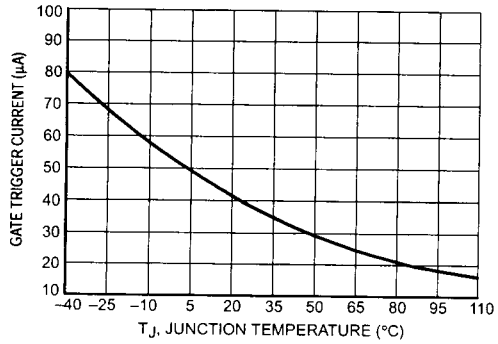


Figure 1. Typical Gate Trigger Current versus Junction Temperature

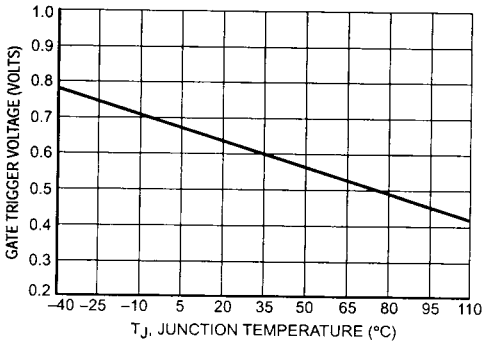


Figure 2. Typical Gate Trigger Voltage versus Junction Temperature

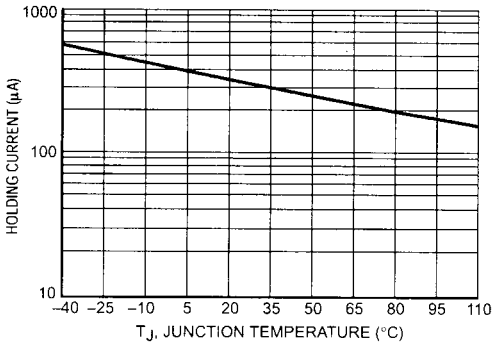


Figure 3. Typical Holding Current versus Junction Temperature

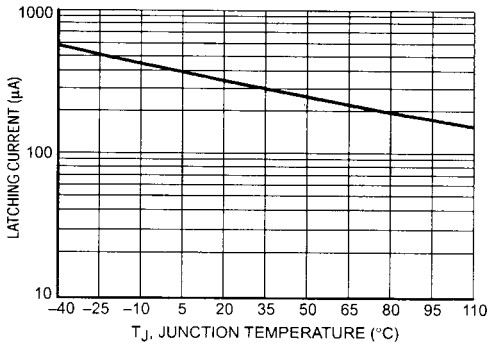


Figure 4. Typical Latching Current versus Junction Temperature

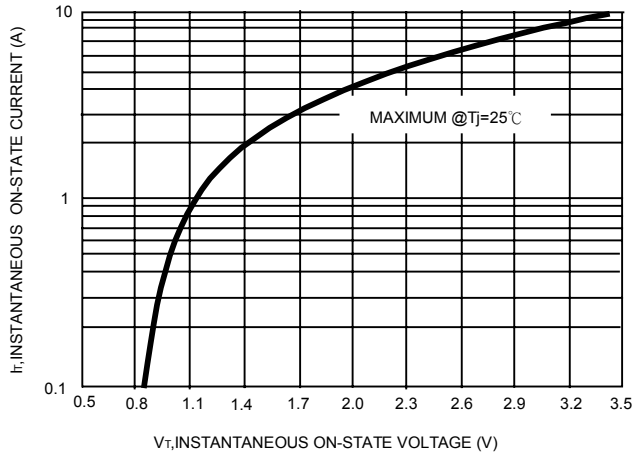


Figure 5. Typical On-State Characteristics