Features

- **Contactless Interface**
  - **Reads and Writes Passive RFID Tags in the Unlicensed 13.56 MHz Band**
  - **Employs ISO/IEC14443 Type A Modulation Schemes**
  - **Autonomous Operation Capability (can scan and read tags without host intervention – i.e. only passes data following successful read/write operation)**
  - **Compatible with NFC Initiation Only Device – User Has Control Over Initiation of all RFID Based Services and Features**
  - **Read/write Operation Between 1 cm and 10 cm Read Range, Depending on Reader/Tag Antenna Coil Sizes and Orientation Relative to the Reader**
  - **Collision Detection as Standard**
  - **Transparent Modes for Software Controlled Modulation Supports Maximum Flexibility and Future Protocols**
  - **Fast Data Communication Rate of 106 kbit/s**
  - **Suitable for Operation with a Wide Variety of Antenna Coil Sizes and Form Factors**
  - **Four Software Adjustable Carrier Field Drive Levels**
- **Controller and Software**
  - **On-board Powerful Atmel AVR® RISC microcontroler, programmed with Innovision® proprietary software.**
  - **Built in Self Test and Diagnostic Modes**
  - **Internal 8 MHz RC Oscillator for Micro or External Crystal Operation**
- **Host Interface**
  - **3-wire SPI Interface as Standard**
  - **Full Software Control via SPI bus at 115 Kbaud as Standard Interface**
- **Power Supply**
  - **Ultra Low Current Operation and Stand-by Sleep Mode Typically < 1 µA**
  - **Ultra Low Voltage Operation: 2.7V - 3.3V**
- **Additional features**
  - **Packages: LBGA36**
  - **LBGA Requires Only an External Crystal, 10 Passives and the Reader Antenna Coil**
  - **Operating temperature range: -30°C to +80°C**

Description

AT90RF135602 is an ultra small footprint low-cost Radio Frequency Identification (RFID) reader developed with Innovision Research & Technology plc to address multi-protocol 13.56 MHz RFID applications.

It is optimised for use with the established ISO/IEC14443 type A standard and is available in Low-profile Ball Grid Array (LBGA).

The LBGA incorporates a custom transceiver front-end along with a protocol & communications controller. It requires only an external crystal and minimal external passive components to interface to the reader antenna.

Protocols are software defined and hence configurable.

Integrated 13.56 MHz Contactless Reader with Embeded software

AT90RF135602

4407A–SCR–04/05

Benefits

- Low-cost – ideal for RFID applications where costs have traditionally proved prohibitive
- Ultra miniature footprint for compact reader design
- Low voltage operation ideal for rechargeable and/or portable applications
- Low operating current for optimal power utilisation
- Low quiescent current sleep mode further prolongs battery life of applications
- Easily integrated into host reader system
- Scalable on-board processor memory size and capacity for custom design solutions
- Operation with multiple protocols such as Philips Mifare® Ultralight, Innovision®-R&T Jewel™ and ISO/IEC14443 type A tags ensures multi-platform compatibility and seamless integration into legacy systems
- Software performs mapping between a common logical memory structure model and physical memory maps of multiple tags types
- Also operates with Innovision R&T proprietary protocols and transparent reader modes for even lower power consumption levels
- Powerful on board RISC processor is available to operate at higher levels of application protocol stack than on conventional reader solutions for more autonomous modes of operation

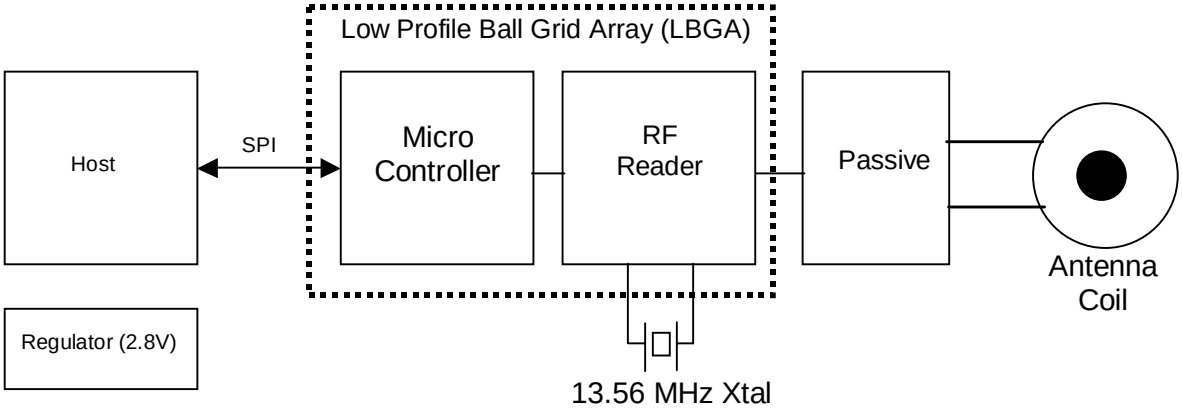
Applications

- Passive read/write RFID tag applications operating in the unlicensed 13.56 MHz band
- Hand-held and low-power battery operated ISO/IEC 14443 type A read/writers
- Reader to reader inductive/Near Field Communications

Block Diagram

The host system, typically containing an application microprocessor, can control the operation of the AT90RF135602 by interfacing commands and application data over a bi-directional Serial Peripheral Interconnect (SPI) interface.

Figure 1. Typical System Architecture

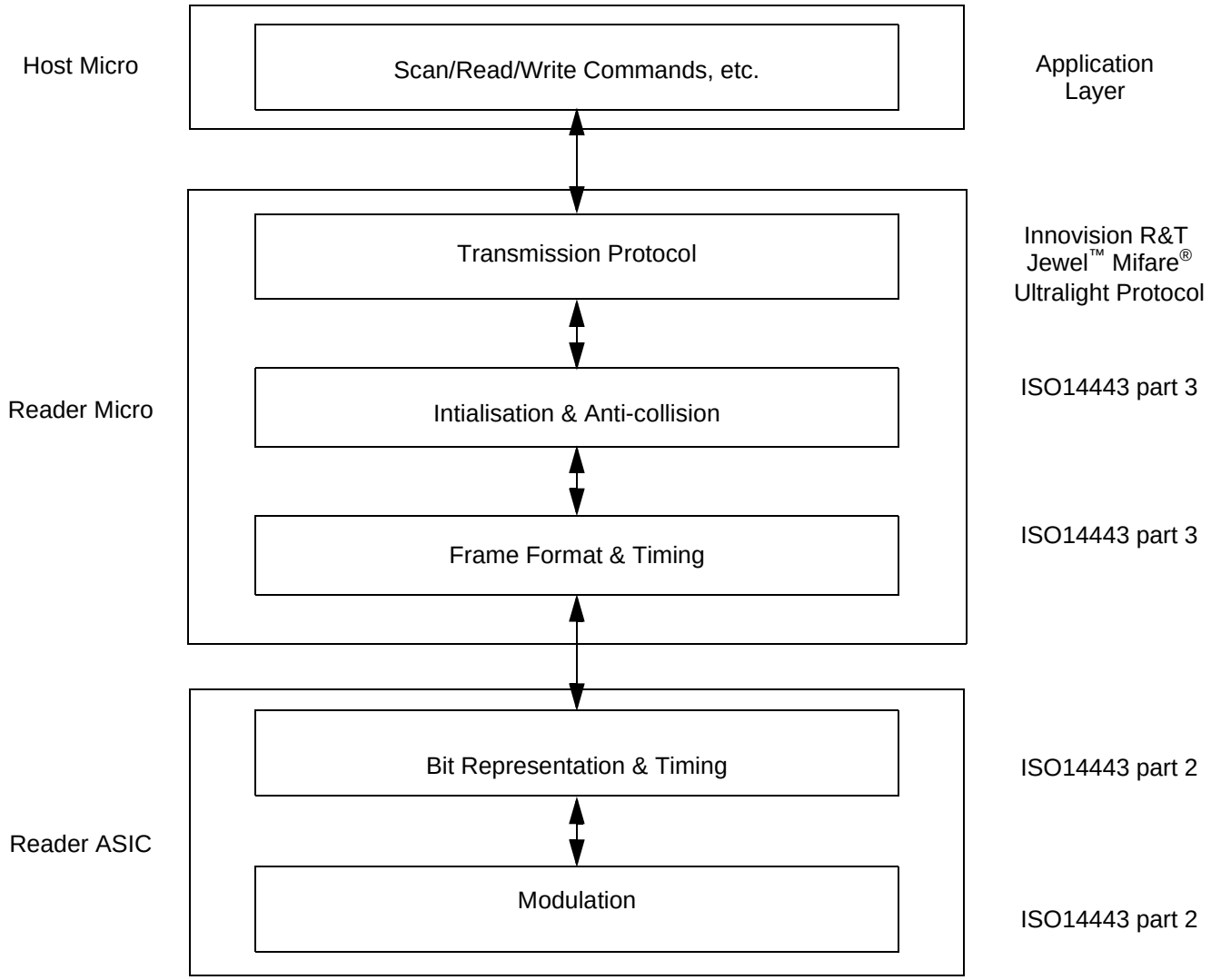


The partitioning of the system into its typical protocol layers is shown in Figure 2.

The exact boundary of each layer of the protocol stack is dependent on the specific application and, therefore, the optimal architectural split of the protocol layers.

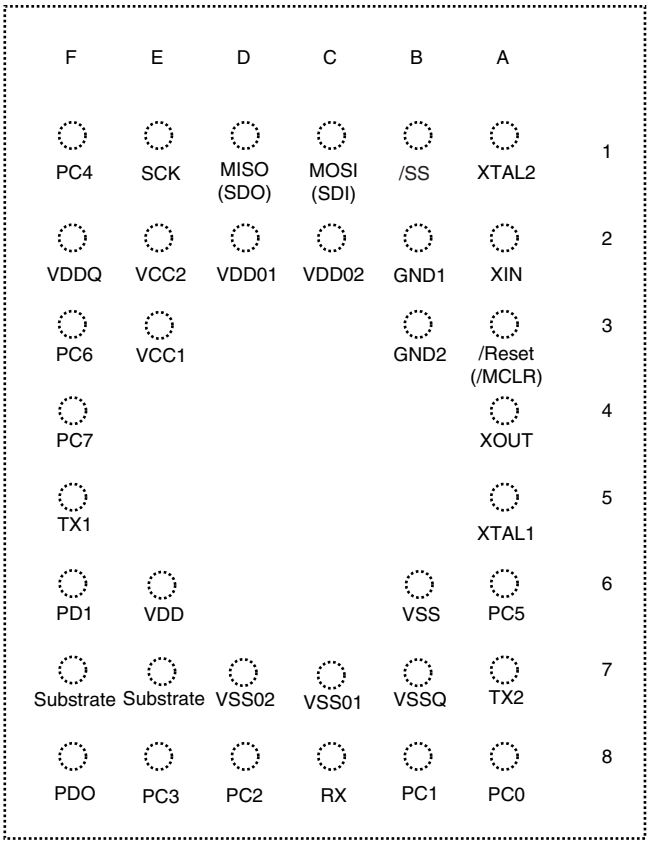
Software implementation of the protocol stack allows for operation with multiple parallel stacks as well as greater flexibility for customisation and future updates.

Figure 2. Overview of Typical Protocol Layers based on OSI 7-layerModel



Pinout

Figure 3. LBGA36 Package Pinout



Pin Description

Table 1. AT90RF15602 Pin Description

PIN Name	Pin Number	i/0/p Type	Description
VDDQ	F2	Power	Analogue Supply
VDD	E6	Power	Logic Supply
VDDO1	D2	Power	Output Stage Supply
VDDO2	C2	Power	Output Stage Supply
VCC1	E3	Power	MCU Supply
VCC2	E2	Power	MCU Supply
GND1	B2	Power	MCU GND
GND2	B3	Power	MCU GND
VSS	B6	Power	Logic GND
VSSQ	B7	Power	Analogue GND
VSSO1	C7	Power	Output Stage GND
VSSO2	D7	Power	Output Stage GND

Table 1. AT90RF15602 Pin Description (Continued)

PIN Name	Pin Number	i/0/p Type	Description
Substrate 1	F7	Power	GND
Substrate 2	E7	Power	GND
/SS	B1	Input	SPI Slave Select (Active Low) *
MOSI (SDI)	C1	Input	SPI Data Input *
MISO (SDO)	D1	Output	SPI Data Output *
SCK	E1	Input	SPI Clock *
/RESET (/MCLR)	A3	Input	Reset (Active Low)
PD0	F8		RESERVED
PD1	F6		RESERVED
PC0	A8		RESERVED
PC1	B8		RESERVED
PC2	D8		RESERVED
PC3	E8		RESERVED
PC4	F1		RESERVED
PC5	A6		RESERVED
PC6	F3		RESERVED
PC7	F4		RESERVED
TX1	F5	Output	Antenna Drive 1
TX2	A7	Output	Antenna Drive 2
RX	C8	Input	Antenna Receiver
XIN	A2	Input	13.56 MHz Crystal or CLK input
XOUT	A4	Output	13.56 MHz Crystal or N/C
XTAL1	A5		RESERVED
XTAL2	A1		RESERVED

Definition of Terms

ASIC	-	Application Specific Integrated Circuit
BIST	-	Built In Self Test
CRC	-	Cyclic Redundancy Check
CSUM	-	Check Sum
ETSI	-	European Telecommunication Standards Institute
FCC	-	Federal Communications Commission
Fc	-	Frequency of Carrier
FIFO	-	First In First Out
Fs	-	Frequency of Subcarrier
GUI	-	Graphical User Interface
TWI	-	Two Wires Interface
LBGA	-	Low-profile Ball Grid Array
OTP	-	One Time Programmable
PC	-	Personal Computer (IBM compatible)
PCD	-	Proximity Coupling Device
PCB	-	Printed Circuit Board
PICC	-	Proximity Integrated Circuit Card
RAM	-	Random Access Memory
SPI	-	Serial Peripheral Interconnect
TBA	-	To Be Advised
TBC	-	To Be Confirmed
UART	-	Universal Asynchronous Receiver Transmitter
XTAL	-	Quartz Crystal

Functional Specification

Outline Functional Specifications

The major determination of the functionality is the embedded software. The following specification is designated for the latest V2.7 software release.

The AT90RF135602 is designed to achieve the following requirements:

Passive RFID reader operation in the unlicensed 13.56 MHz band

Read/Write operation using ISO/IEC14443-2 type A modulation schemes at data communication rates of 106 kbit/s

Conform to the standard of ISO/IEC14443-3 type A as far as is required to operate with the Mifare Ultralight and the Innovision R&T low-cost Jewel RFID ICs

Low voltage operation from a 2.7V supply

Low current operation with stand-by sleep mode

Interface electrically to the host system controller via an SPI based interface and associated digital control signals

Operates with minimal battery power consumption to optimise the battery life in both active and standby modes

Operation with Innovision R&T low-cost, low power proprietary tag protocols

Reader to reader inductive Near Field Communications capability using Innovision R&T proprietary protocols in software

Transparent modes for direct software controlled modulation protocols for maximum flexibility

General Specifications

- Multi-protocol RFID IC:
  - ISO/IEC14443A parts 2 & 3 (frame format)
  - User transparent operation with both the Philips Mifare Ultralight and Innovision R&T low-cost Jewel tags
- Operation:Read/Write
- Number of bytes:
  - Ultralight: 48 user Read/Write bytes
  - Jewel: 96 user Read/Write bytes
- Tag scan rate:Variable by host
- Carrier frequency:External 13.56 MHz crystal controlled
- Carrier field drive level:
  - Four software adjustable carrier field drive and Q levels determined by selection of output stage drive impedance:

    Level1 – 40 Ω

    Level2 – 20 Ω (Default for v2.7)

    Level3 – 10 Ω

    Level4 – 5 Ω
- Antenna configuration:Balanced “push-pull” output stages driving a symmetrical series resonant antenna coil for optimal carrier field generation when operating from low voltage supply
- FCC/ETSI EMC Compliancy:Simple LC low-pass filters used on output stages to achieve harmonic reduction required for EMC compliancy
- Operating voltage range: 2.7 – 3.0 V
- Maximum voltage rating: 3.3 V
- Peak supply current: < 65 mA peak (depending on drive level selection, antenna matching and tuning)
- Sleep-mode quiescent current: <10 µA (1 µA typical)
- Protocol Control: Atmel pre-programmed RISC Microprocessor
- Software program memory: Pre-programmed with Innovision Firmware revision V2.7
- Data memory: Reserved
- Non-volatile memory: Reserved
- Interfaces:
  - 3 wire SPI interface at 115 kBaud

Figure 4. Recommended Circuit for Extended Range

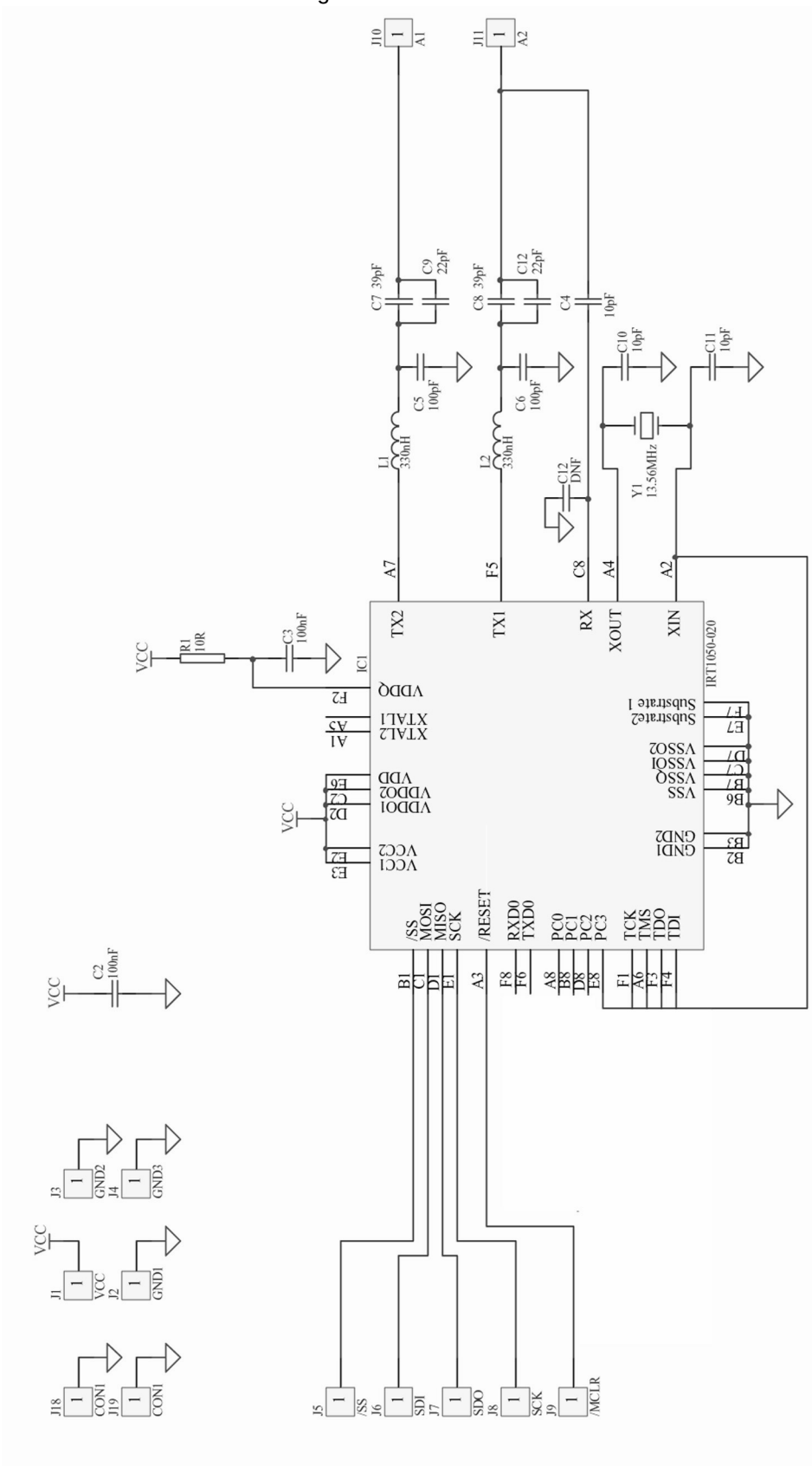
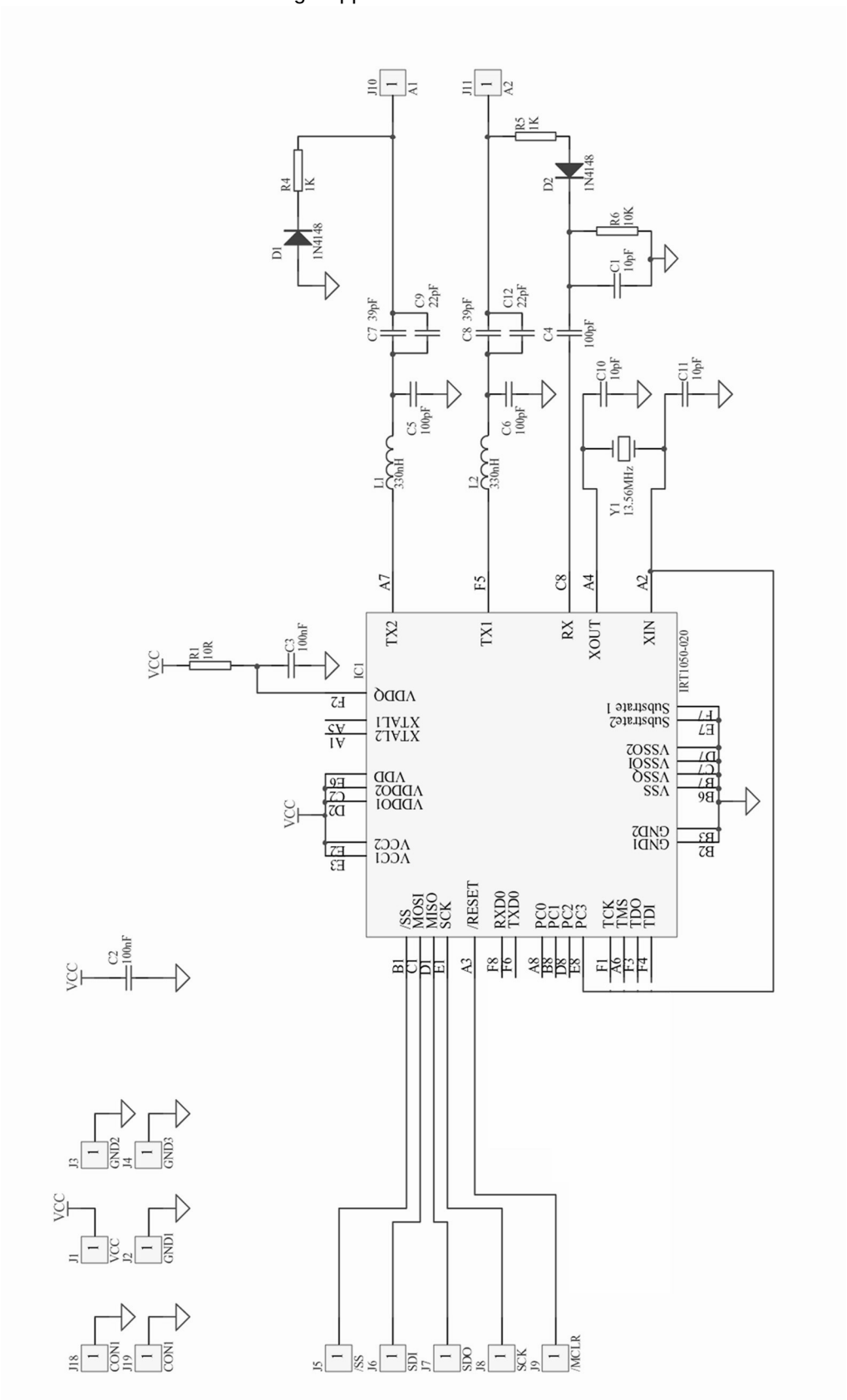


Figure 5. Recommended Circuit For Short Range Application



SPI Interface Protocol

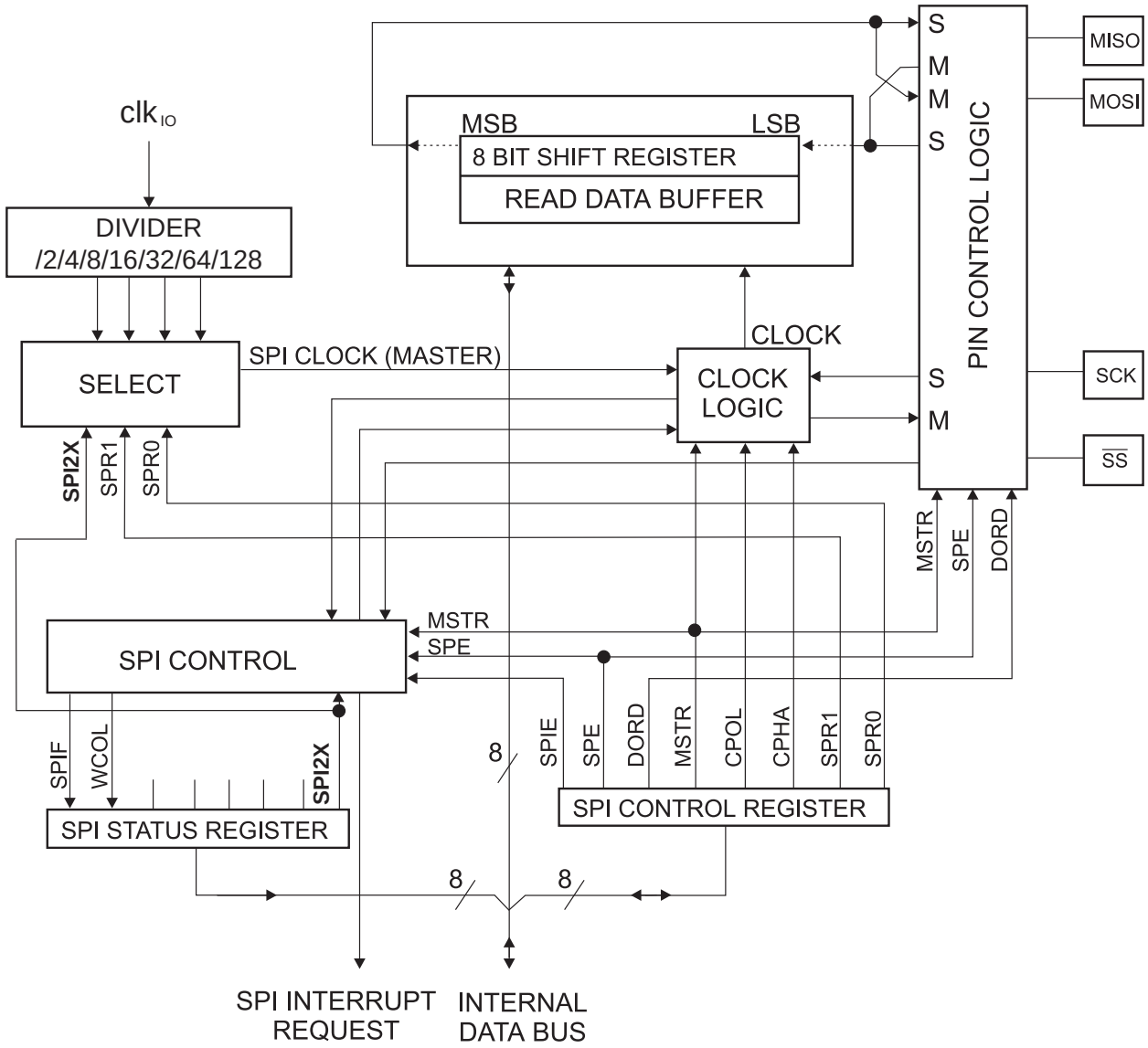
Serial Peripheral Interface – SPI

The Serial Peripheral Interface (SPI) allows high-speed synchronous data transfer between the AT90RF135602 and peripheral devices or between several AVR devices. The AT90RF135602 SPI includes the following features:

Features

- **Full-duplex, Three-wire Synchronous Data Transfer**
- **Master or Slave Operation**
- **LSB First or MSB First Data Transfer**
- **Seven Programmable Bit Rates**
- **End of Transmission Interrupt Flag**
- **Write Collision Flag Protection**
- **Wake-up from Idle Mode**
- **Double Speed (CK/2) Master SPI Mode**

Figure 6. SPI Block Diagram

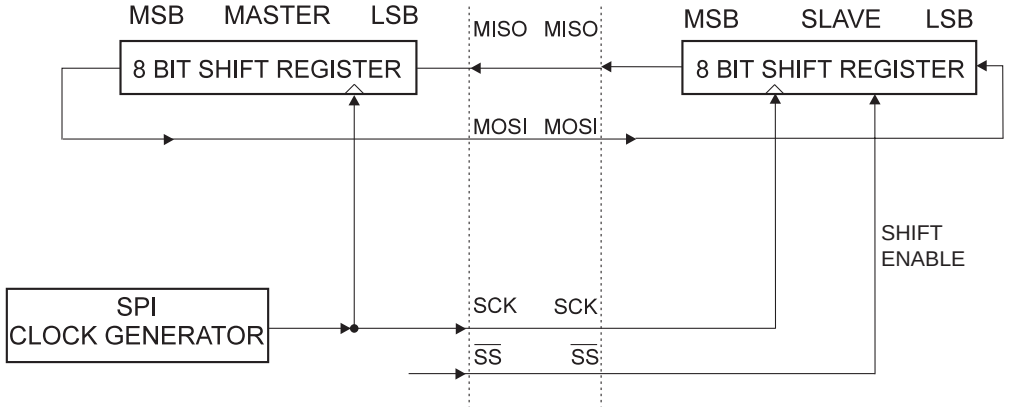


The interconnection between Master and Slave CPUs with SPI is shown in Figure 7. The system consists of two shift Registers, and a Master clock generator. The SPI Master initiates the communication cycle when pulling low the Slave Select $\overline{SS}$ pin of the desired Slave. Master and Slave prepare the data to be sent in their respective shift Registers, and the Master generates the required clock pulses on the SCK line to interchange data. Data is always shifted from Master to Slave on the Master Out – Slave In, MOSI, line, and from Slave to Master on the Master In – Slave Out, MISO, line. After each data packet, the Master will synchronize the Slave by pulling high the Slave Select, $\overline{SS}$, line.

When configured as a Master, the SPI interface has no automatic control of the $\overline{SS}$ line. This must be handled by user software before communication can start. When this is done, writing a byte to the SPI Data Register starts the SPI clock generator, and the hardware shifts the eight bits into the Slave. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If the SPI Interrupt Enable bit (SPIE) in the SPCR Register is set, an interrupt is requested. The Master may continue to shift the next byte by writing it into SPDR, or signal the end of packet by pulling high the Slave Select, $\overline{SS}$ line. The last incoming byte will be kept in the Buffer Register for later use.

When configured as a Slave, the SPI interface will remain sleeping with MISO tri-stated as long as the $\overline{SS}$ pin is driven high. In this state, software may update the contents of the SPI Data Register, SPDR, but the data will not be shifted out by incoming clock pulses on the SCK pin until the $\overline{SS}$ pin is driven low. As one byte has been completely shifted, the end of transmission flag, SPIF is set. If the SPI Interrupt Enable bit, SPIE, in the SPCR Register is set, an interrupt is requested. The Slave may continue to place new data to be sent into SPDR before reading the incoming data. The last incoming byte will be kept in the Buffer Register for later use.

Figure 7. SPI Master-slave Interconnection



The system is single buffered in the transmit direction and double buffered in the receive direction. This means that bytes to be transmitted cannot be written to the SPI Data Register before the entire shift cycle is completed. When receiving data, however, a received character must be read from the SPI Data Register before the next character has been completely shifted in. Otherwise, the first byte is lost.

In SPI Slave mode, the control logic will sample the incoming signal of the SCK pin. To ensure correct sampling of the clock signal, the frequency of the SPI clock should never exceed $f_{clkio}/4$.

General

This section describes the operation and interface protocol between the typical host controller and the AT90RF135602 for v2.7 of software.

The AT90RF135602 always operates as a slave to the host controller device acting as the master.

The SPI interface operation is specified by the /SS and /RESET lines as shown in the table below.

/RESET	/SS	Interface Mode
Low	Low or High	Reserved
High	High	Sleep mode
High	Low	SPI interface and AT90RF135602 active

To clarify:

The AT90RF135602 ignores SCK from the host and tri-states the MOSI and MISO lines whilst /SS is high

As the slave, the AT90RF135602 accepts the SCK from the host and produces serial output data from its MISO output only when /SS is low.

The MOSI input is used to receive commands and data from the host in conjunction with the SCK clock when /SS is low.

Operation from a cold power-up and reset defaults to be in low quiescent current “Sleep Mode” waiting for /SS to go low.

SPI Setup

AT90RF135602 is slave.

/SS idle condition is high.

Prior to transmitting a message the /SS line is set low by the host, after the message has been transmitted the /SS line is set back high again.

The interval between the host lowering /SS and then generating the first SCK pulse should be a minimum of 3us.

SCK idle condition is low.

The leading edge is rising and the trailing edge falling.

In each direction data is loaded on the rising clock edge and is valid (and sampled) on the falling clock edge.

The minimum interval between the 8th SCK of a byte and the 1st SCK of the next byte shall be 10us for status poll commands and 23us for all other commands.

SPI Command/Response Message Structure

The host generates the SPI clock signals to send “Command” messages to the AT90RF135602.

The host generates the SPI clock signals to receive “Response” messages from the AT90RF135602.

The generic message structure is independent of message direction and is transparent to the SPI hardware interface.

Messages are either single byte or multi-byte.

All messages are terminated by an 8-bit Checksum byte (CSUM) this is calculated as the 8-bit sum of all the proceeding bytes in the message.

Multi-byte messages are indicated by the most significant bit set to “1” in the first byte of the message.

The length of the additional information is determined by the message type and nature of the additional information bytes.

The maximum allowable length of a message including its checksum is 255 bytes.

SPI Message Type	Byte	Description
Single byte message (1 byte + Checksum)	1st Byte	0x00 – 0x7F Single byte message type
	2nd Byte	CSUM
Multi-byte message (Minimum of 3 bytes + Checksum)	1st Byte	0x80 – 0xFF Multi-byte message type
	2nd Byte	Information byte
	3rd Byte	Information byte
	0 – 251 Bytes	Additional information bytes
	Last Byte	CSUM

The host may command Read/Write to the whole of a tag or can restrict the operation to individual pages and sectors using a common message structure which can be independent of tag type.

Addressing Modes

The v2.7 AT90RF135602 software provides for two modes of addressing tags using either Logical or Physical addressing depending on the command variant.

For Logical addressing the application can work independent of tag type as long as the data capacity is not exceeded. The AT90RF135602 software will seamlessly handle the mapping of logical addresses over to either the Innovision Jewel or the Philips Mifare Ultralight depending on the type of tag it recognises as being present.

The mapping for logical start address is given in Appendix A.

For Physical addressing the application layer must first know which type of tag is present and then address the memory bytes using physical addresses from the tag datasheet.

The user is referred to relevant datasheet documentation.

AT90RF135602 Command Message Structure

To wake-up the AT90RF135602 and to start the tag read or write operations the host as the *master* must send either a single or a multi-byte Command message.

The single byte message consists of a command byte and checksum byte, as follows:

To AT90RF135602 = <CMD> <CSUM>

The multi-byte message consists of a command byte, start address byte, data length value byte, the data (if relevant to the command) and checksum byte as follows:

To AT90RF135602 = <CMD> <ADR> <DLV> <*DATA0*> <*DATA1*>…..<CSUM>

Where: <CMD> - is the command byte with top bit set (e.g. Read, Write, etc)

<ADR> - is the start address byte (0 to 255) for the operation*

<DLV> - is the length in number of bytes to read or write (0 to 240)

<*DATAx*> - is data byte(s) - sent least significant byte first - if relevant to the command (e.g. for writing)

<*CSUM*> – is the 8-bit sum of the proceeding bytes

The message is sent most significant byte (i.e. <CMD> byte) first.

The data bytes are sent least significant byte first.

The 8-bit bytes are sent MOST significant bit first.

Subsequent to a command message (which both wakes-up the AT90RF135602 and starts the tag read or write operations) the host as the *master* should poll periodically to assess the status and progress of the commanded operation.

* Start address is given in logical terms for user Read/Write area (see Appendix A)

Table of Commands

<CMD>	Explanation	Bytes
0x00	**Poll Status from AT90RF135602**	<CMD> = 0x00 <CSUM> = 0x00
0x70	Built-In Self Test (See Built-In self test section for further details)	<CMD> = 0x70 <CSUM> = 0x00
0x80	Read User Data Logical (Read requested number of user R/W data bytes from requested logical start address of any tag type)	<CMD> = 0x80 <ADR> = Start logical address <DLV> = Number of bytes to be read <CSUM> = Checksum User data starts at logical address 0x00
0x86	Read Physical (Read requested number of bytes from requested physical start address of known tag type) NB Application must know tag type	<CMD> = 0x86 <ADR> = Start physical address <DLV> = Number of bytes to be read <CSUM> = Checksum
0x90	Read UID/lock/OTP/User Data logical (Read requested number of UID, lock, OTP & user data bytes from requested logical start address of any tag type)	<CMD> = 0x90 <ADR> = Start logical address <DLV> = Number of bytes to be read <CSUM> = Checksum UID starts at logical address 0x00 to 0x07 Lock bits start at logical address 0x08 to 0x09 OTP bits start at logical address 0x0A to 0x0F User data starts at logical address 0x10

<CMD>	Explanation	Bytes
0xA0	Write User Data Logical (Write requested number of user data bytes starting at requested logical address of any tag type)	<CMD> = 0xA0 <ADR> = Start logical address <DLV> = Number of bytes to write (n) <DATA0>…<DATAn-1> = n bytes to write <CSUM> = Checksum User data starts at logical address 0x00
0xA4	Write User Data Logical to specific UID (Verify specific UID; if equal then write requested number of data bytes starting at requested logical address and verify, if still present)	<CMD> = 0xA4 <ADR> = Start logical address <DLV> = Number of bytes to write (n) <DATA0>…<DATA7> = UID of specified tag <DATA8>…<DATA7+n> = n bytes to write <CSUM> = Checksum User data starts at logical address 0x00
0xA6	Write Physical (Write requested number of bytes starting at requested physical address of known tag type and verify, if still present) NB: Application must know tag type	<CMD> = 0xA6 <ADR> = Start physical address <DLV> = Number of bytes to write (n) <DATA0>…<DATAn-1> = n bytes to write <CSUM> = Checksum
0xA8	Write Physical to specific UID (Verify specific UID; if equal then write requested number of bytes starting at requested physical address of known tag type and verify, if still present) NB: Application must know tag type	<CMD> = 0xA8 <ADR> = Start physical address <DLV> = Number of bytes to write (n) <DATA0>…<DATA7> = UID of specified tag <DATA8>…<DATA7+n> = n bytes to write <CSUM> = Checksum User data starts at logical address 0x00
0xAC	Reader IC Configuration diagnostic command	Configuration data – 3 bytes 0xAC010020 – selects 40Ω Driver resistance 0xAC030020 – selects 20Ω Driver resistance 0xAC050020 – selects 10Ω Driver resistance 0xAC070020 – selects 5Ω Driver resistance This setting remains in force for subsequent communications with the tag until the AT90RF135602 is reset. The default driver resistance after reset or power up is 20Ω for software v2.7.
0xB0	Write Lock/OTP/User Data logical (Write requested number of lock, OTP & user data bytes to requested logical start address of any tag type and verify, if still present) NB: Writing to UID area is not valid	<CMD> = 0xB0 <ADR> = Start logical address <DLV> = Number of bytes to write(n) <DATA0>…<DATA n-1> = n bytes to write <CSUM> = Checksum UID starts at logical address 0x00 to 0x07 Lock bits start at logical address 0x08 to 0x09 OTP bits start at logical address 0x0A to 0x0F User data starts at logical address 0x10

<CMD>	Explanation	Bytes
0xB4	Write Lock/OTP/User Data Logical to specific UID (Verify specific UID of tag; if equal then write requested number of lock, OTP & user data bytes to requested logical start address of any tag type and verify, if still present) NB: Writing to UID area is not valid.	<CMD> = 0xB4 <ADR> = Start logical address <DLV> = Number of bytes to write(n) <DATA0>…<DATA7> = UID of specified tag <DATA8>…<DATA7+n> = n bytes to write <CSUM> = Checksum UID starts at logical address 0x00 to 0x07 Lock bits start at logical address 0x08 to 0x09 OTP bits start at logical address 0x0A to 0x0F User data starts at logical address 0x10

See Appendix B for an example Command Response sequence.

AT90RF135602 Response Message Structure

At the same time as the host sends a message, the AT90RF135602 returns its status response:

Single byte response from AT90RF135602 = <STATUS> <*CSUM*>

If the AT90RF135602 is still busy processing the last command then the response data received during the 16 clock periods of the polling command message will be:

STATUS = 0x01 which means AT90RF135602 busy.

When the AT90RF135602 has finished its operation, or has error conditions, then either a single byte or a multi-byte status message will be returned by SPI clocks from the host.

Multi-byte response from AT90RF135602 =

<STATUS> <STATUS1> <DLV> <*DATA0*> <*DATA1 ...*<*CSUM*>

Where: <STATUS> – Status response

<STATUS1> – Status byte 1 which includes further information (e.g. tag type from the previous operation)

<DLV> – is the length in number of bytes that were successfully read or written (0 to 240). It is only present if relevant to the status response.

<*DATAx*> - is data byte(s), if relevant to the command (e.g. for reading)

<*CSUM*> – is the 8-bit sum of the proceeding bytes

The message is sent <STATUS> byte first.

The data bytes are sent least significant byte first.

The 8-bit bytes are sent most significant bit first.

Table of Responses

The checksum byte is not shown in the table below.

Single Byte Responses

<STATUS>	Explanation	Bytes
0x00	Normal operation	<STATUS> = 0x00 <CSUM> = Checksum
0x01	Busy processing last command	<STATUS> = 0x01 <CSUM> = Checksum
0x10	SPI Command Format Error	<STATUS> = 0x10 <CSUM> = Checksum
0x20	No Tag Found	<STATUS> = 0x20 <CSUM> = Checksum

Multi-byte Responses

<STATUS>	Explanation	Bytes
0x80	Read User Data Logical Successful	<STATUS> = 0x80 <STATUS1> = tag type <DLV> = number bytes successfully read (n) <DATA0>…<DATA n-1> = n bytes read <CSUM> = Checksum User data starts at logical address 0x00
0x86	Read User Data Physical Successful	<STATUS> = 0x86 <STATUS1> = tag type <DLV> = number bytes successfully read (n) <DATA0>…<DATA n-1> = n bytes read <CSUM> = Checksum
0x90	Read UID/Lock/OTP/User Data Logical Successful	<STATUS> = 0x90 <STATUS1> = tag type <DLV> = number bytes successfully read (n) <DATA0>…<DATA n-1> = n bytes read <CSUM> = Checksum UID starts at logical address 0x00 to 0x07 Lock bits start at logical address 0x08 to 0x09 OTP bits start at logical address 0x0A to 0x0F User data starts at logical address 0x10
0x8F	Read Error	<STATUS> = 0x8F <STATUS1> = Error code: 1 byte <CSUM> = Checksum
0xA0	Write User Data Logical Successful	<STATUS> = 0xA0 <STATUS1> = tag type <DLV> = number bytes successfully written <CSUM> = Checksum

<STATUS>	Explanation	Bytes
0xA4	Write User Data Logical to specific UID Successful	<STATUS> = 0xA4 <STATUS1> = tag type <DLV> = number bytes successfully written <CSUM> = Checksum
0xA6	Write Physical Successful	<STATUS> = 0xA6 <STATUS1> = tag type <DLV> = number bytes successfully written <CSUM> = Checksum
0xA8	Write Physical to specific UID Successful	<STATUS> = 0xA8 <STATUS1> = tag type <DLV> = number bytes successfully written <CSUM> = Checksum
0xB0	Write Lock/OTP/User Data Logical Successful	<STATUS> = 0xB0 <STATUS1> = tag type <DLV> = number bytes successfully written <CSUM> = Checksum
0xB4	Write Lock/OTP/User Data Logical to specific UID Successful	<STATUS> = 0xB4 <STATUS1> = tag type <DLV> = number bytes successfully written <CSUM> = Checksum
0xAF	Write Error	<STATUS> = 0xAF <STATUS1> = Error code: 1 byte <CSUM> = Checksum
0xBA	Built-In Self Test Response (See Built-In self test section for further details).	<STATUS> = 0xBA <STATUS1> = Test Result <DATA0>…<DATA n-1> = Software Version: 2 bytes Serial Number/Production Information: 8 bytes <CSUM> = Checksum

Tag Type

<STATUS1>	Explanation
0x44	Mifare Ultralight
0x0C	Innovision Jewel

Error Code

<STATUS1>	Explanation
0x10	Verify error during write
0x11	Wrong serial number tag present for specific write
0x12	Area to be written is locked
0x13	Start address out of range
0x14	Write size exceeds tag capacity

See Appendix B for an example Command Response sequence.

Sleep-Mode

The AT90RF135602 will enter low quiescent current “Sleep Mode” when /SS is high and all tag operations have been completed.

SPI Clock Frequency

This is determined by the host micro-controller, since this is the master and hence will generate the SCK signal.

The recommended SPI clock frequency is 115kHz.

Power On Reset, Reset & Host In-circuit Programming

Power On Reset (POR)

From cold start the POR will occur followed by initialisation of the microprocessor. From application of power the AT90RF135602 will be ready to receive an SPI command data within 6 mS.

Reset

The active low /RESET signal from the host will cause the AT90RF135602 to enter the reset condition. From release of this signal high the AT90RF135602 will be ready to receive SPI command data within 6 mS.

When /RESET is held low the AT90RF135602 will enter serial programming mode. In this mode the SPI SCK, MISO, MOSI lines may be used to upgrade the firmware.

Built-In Self Test (BIST) Mode

General

The BIST consists of a single sequence of test stages designed as a confidence test that the AT90RF135602 is operational and also as a basic diagnostic aid if operation becomes impaired.
Beyond this it is not possible to perform an exhaustive test of operational performance without the presence of a tag for functional test purposes.

Initiation

The BIST mode is activated by the single byte Host SPI command 0x70.

BIST Sequence:

- CRC Verification of all Flash Program Memory

  If this test fails, subsequent tests are not performed.
- Integrity of all RAM Memory

  If this test fails, subsequent tests are not performed.
- Loop around Test

The Loop around Test is designed to test the Xtal oscillator, antenna drive and demodulator sections of the AT88RF135602 for connectivity and operation to a limited functional extent.

BIST Response

The BIST response is composed of 12 bytes followed by a checksum. The structure of the response is shown in following table:

Byte	Name	Description
1 <STATUS>	Built-In Self Test response	0xBA
2 <STATUS1>	Test Result	The test result byte indicates the progress of the self-test. Test errors are indicated in a bit-wise fashion as listed below: 0x00 : All tests passed 0x01 : Flash CRC verification problem 0x02 : RAM integrity problem 0x04 : Loop back problem
3-4 <DATA0> …. <DATA1>	Software Version	2 byte (MSB first) data representing the software version of the application in Flash Memory. For example 0x02, 0x07 represents version V2.7
5-12 <DATA2> …. <DATA9>	Serial number and production information	8 bytes, (MSB first), representing the serial number and production information stored in EEPROM.

An example of the BIST response is shown below

```
0xBA, 0x00, 0x02, 0x07, 0x11, 0x22, 0x33, 0x44, 0x55, 0x66, 0x77,
0x88

0xBA:  BIST Response
0x00:  Successful test result
0x02,0x07: Software Version 2.7
0x11,0x22,0x33,0x44: Serial/Production Information 0x11223344
0x55,0x66,0x77,0x88: Serial/Production information 0x55667788
```

Appendix A – Tag Memory Maps

A1 Mapping Between Logical Address & Philips Mifare Ultralight Physical Memory

Logical Address for user data only; 0x80 0xA0 0xA4	Logical Address for; 0x90 0xB0 0xB4	Physical Address	Description		
		Page	Byte Number	Name	Comments
-	0–2	0	0-2	SN0 – SN2	Serial Number (UID)
-	3–6	1	0-3	SN3 – SN6	Serial Number (UID)
-	7	-	-	-	-
-	8-9	2	2-3	Lock0-Lock1	Lock Bytes
-	10–13	3	0-3	OTP0 – OTP3	OTP – writes are bit-wise “or-ed“ with existing contents
-	14-15	-	-	-	-
0-3	16-19	4	0 – 3	Data0 – Data3	User Data area - read/write
4-7	20-23	5	0 – 3	Data4 – Data7	User Data area - read/write
8-11	24-27	6	0 – 3	Data8 – Data11	User Data area - read/write
12-15	28-31	7	0 – 3	Data12 – Data15	User Data area - read/write
16-19	32-35	8	0 – 3	Data16 – Data19	User Data area - read/write
20-23	36-39	9	0 – 3	Data20 – Data23	User Data area - read/write
24-27	40-43	10	0 – 3	Data24 – Data27	User Data area - read/write
28-31	44-47	11	0 – 3	Data28 – Data31	User Data area - read/write
32–35	48–51	12	0 – 3	Data32 – Data35	User Data area - read/write
36-39	52-55	13	0 – 3	Data36 – Data39	User Data area - read/write
40-43	56-59	14	0 – 3	Data40 – Data43	User Data area - read/write

A2 Mapping Between Logical Address & Innovision Jewel Physical Memory

Logical Address for user data only; 0x80 0xA0 0xA4	Logical Address for; 0x90 0xB0 0xB4	**Physical Address**	**Description**		
		Block (Hex)	**Byte Number**	**Name**	**Comments**
-	0–7	0	0-7	UID0 – UID7	Unique identification Number (used to verify correct tag is the target of read/write commands)
-	8–9	E	0-1	LOCK0 – LOCK1	Lock Bytes
-	10-15	E	2-7	OTP0 – OTP5	OTP – writes are bit-wise “or-ed“ with existing contents
0–7	16-23	1	0-7	Data0 – Data7	User Data area - read/write
8-15	24-31	2	0-7	Data8 – Data15	User Data area - read/write
16-23	32-39	3	0-7	Data16 – Data23	User Data area - read/write
24-31	40-47	4	0-7	Data24 – Data31	User Data area - read/write
32-39	48-55	5	0-7	Data32 – Data39	User Data area - read/write
40-47	56-63	6	0-7	Data40 – Data47	User Data area - read/write
48-55	64-71	7	0-7	Data48 – Data55	User Data area - read/write
56-63	72-79	8	0-7	Data56 – Data63	User Data area - read/write
64-71	80–87	9	0-7	Data64 – Data71	User Data area - read/write
72-79	88-95	A	0-7	Data72 – Data79	User Data area - read/write
80–87	96-103	B	0-7	Data80 – Data87	User Data area - read/write
88-95	104-111	C	0-7	Data88 – Data95	User Data area - read/write

A3 Lock Bit Functionality

This section outlines the operation of the lock bits located at logical address 8 & 9 for commands 0x90, 0xB0, 0xB4.

The Lock bits are used to 'write protect' blocks of memory.
For example, bit 0 of lock byte 0 locks the first 8 data bytes (addresses 0x10 to 0x17 for commands 0x90, 0xB0, 0xB4)
Bit 1 of lock byte 0 locks the second block of 8 data bytes (addresses 0x18 to 0x1F for commands 0x90, 0xB0, 0xB4)

The correlation between lock bits and areas of logical memory locked is shown in the table below:

Lock Byte 0

Memory locations locked (decimal)	**Bit**							
	MSB – 7	6	5	4	3	2	1	LSB - 0
0x80, 0x84, 0xA0, 0xA4 commands	56 – 63*	48 – 55*	40 – 47	32 – 39	24 – 31	16 – 23	08 – 15	00 – 07
0x90, 0xB0, 0xB4 commands	72 – 79*	64 – 71*	56 – 63	48 – 55	40 – 47	32 – 39	24 – 31	16 – 23

Lock Byte 1

Memory locations locked (decimal)	**Bit**							
	MSB – 7	**6**	**5**	**4**	**3**	**2**	**1**	**LSB - 0**
0x80, 0x84, 0xA0, 0xA4 commands	unused	unused	unused	unused	88 – 95*	80 – 87*	72 – 79*	64 – 71*
0x90, 0xB0, 0xB4 commands	unused	unused	unused	unused	104 –111*	96 – 103*	88 – 95*	80 – 87*

Appendix B – Command Examples

B1 Command Response Sequence Example 1

To read 3 bytes of data starting from logical address DATA4:

Command, <CMD> = 0x80

Start address, <ADR> = 0x04

Data length value, <DLV> = 0x03

Checksum, <CSUM> = 0x87

WITH TAG PRESENT

Initiate Read;

C1: <80><04><03><87>

R1: <00><00><XX><XX>

Poll status;

C2: <00><00>

R2: <01><01>AT90RF135602 is busy

Poll status;

C3: <00><00>

R3: <01><01>AT90RF135602 is busy

Poll status;

C4: <00><00><XX><XX><XX><XX><XX>

R4: <80><44><03><44><55><66><C6> Read successful

Response = 0x80

Tag type = 0x44 (Mifare Ultralight)

Number of bytes successfully read = 0x03

Data4=0x44, Data5=0x55, Data6=0x66

Checksum = 0xC6

B2 Command Response Sequence Example 2

To read 3 bytes of data starting from logical address DATA4:

Command, <CMD> = 0x80

Start address, <ADR> = 0x04

Data length value, <DLV> = 0x03

Checksum, <CSUM> = 0x87

NO TAG PRESENT

Initiate Read;

C1: <80><04><03><87>

R1: <00><00><XX><XX>

Poll status;

C2: <00><00>

R2: <01><01>AT90RF135602 is busy

Poll status;

C3: <00><00>

R3: <01><01>AT90RF135602 is busy

Poll status;

C4: <00><00>

R4: <20><20> No tag found

Status = 0x20

Checksum = 0x20

B3 Command Response Sequence Example 3

To write 4 bytes of data, starting from logical address DATA5:

Command, <CMD> = 0xA0.

Start address, <ADR> = 0x05.

Data length value, <DLV> = 0x04.

DATA5 = 0x55, DATA6 = 0x66, DATA7 = 0x77, DATA8 = 0x88.

Checksum, <CSUM> = 0x63.

WITH TAG PRESENT

Initiate Write;

C1: <A0><05><04><55><66><77><88><63>

R1: <00><00><XX><XX><XX><XX><XX><XX>

Poll status;

C2: <00><00>

R2: <01><01>AT90RF135602 is busy

Poll status;

C3: <00><00>

R3: <01><01>AT90RF135602 is busy

Poll status;

C4: <00><00><XX><XX>

R4: <A0><44><04><E8> Write successful

Response = 0xA0

Tag Type = 0x44

Number of bytes successfully written = 0x04

Checksum = 0xE8

Electrical Characteristics

Absolute Maximum Ratings

I = industrial .....-40°C to 85°C
Operating Temperature..... -30°C to + 80°C
StorageTemperature ..... -40°C to + 85°C
Voltage on V_{CC} to V_{SS} .....-0.5V to + 6.5V
Voltage on Any Pin to V_{SS}.....-0.5V to V_{CC} + 0.5V
Power Dissipation Typical..... 120 mW
Power Dissipation Max ..... 300 mW

Note: Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

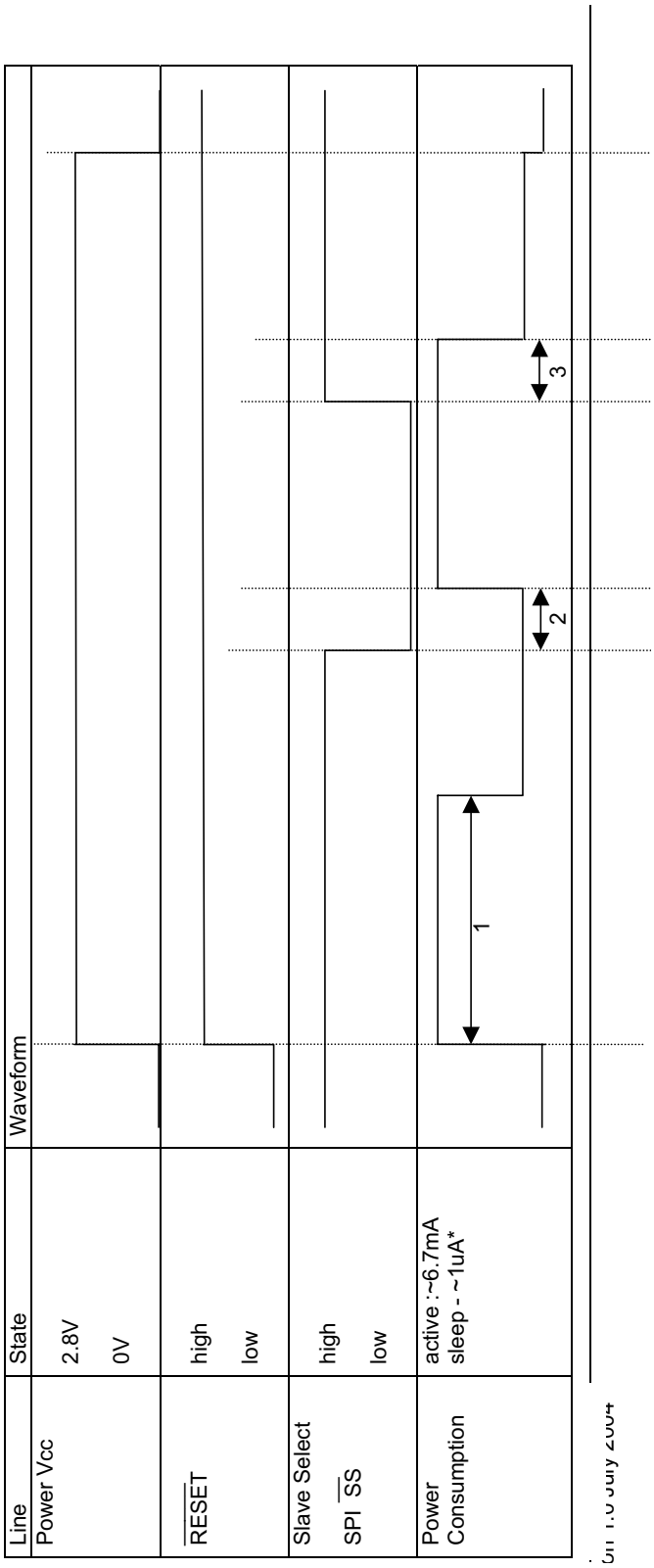
Power dissipation is based on the maximum allowable die temperature and the thermal resistance of the package.

DC Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	Supply voltage		2.7	2.8	3.0	V
$I_{CC\ Power\ Down}$	Sleep mode current consumption			1uA	10uA	µA
$I_{CC\ Active}$ (field off)	Operating current			6.6		mA
$I_{CC\ Active}$ (field on)	Transmitting current	Max drive level		40	65	mA
$I_{OL/H}$	Output current at Tx1 or Tx2		-100		100	mA
	Output resistance at Tx1 or Tx2	Drive level 1		40		Ω
		Drive level 2		20		Ω
		Drive level 3		10		Ω
		Drive level 4		5		Ω
	Rise and fall time for 100% ASK					µS
	Xtal frequency range		13	13.56	14	MHz
	Ext clock Xin		1		Vcc	V (p-p)
	Rx input resistance		8.8	11	13.2	kΩ
	Rx input capacitance			4		pF
	Rx input delta carrier envelope change					mV p-p
	Rx input envelope amplitude		1		2	V p-p
V_{IL}	Input Low Voltage		-0.5		0.3Vcc	V
V_{IH}	Input High Voltage		0.6Vcc		Vcc+0.5	V
V_{OL}	Output Low Voltage	I_{OL}=10mA Vcc=2.7V			0.5	V
V_{OH}	Output High Voltage	I_{OH}=-10mA Vcc=2.7V	2.2			V

AC Parameters

Figure 8. Power Characteristics



Note: 1. Sleep current is n~1uA with the PC3-Xin link and ~36uA without the link, (operational mode set appropriately)

Figure 9. SPI Characteristics

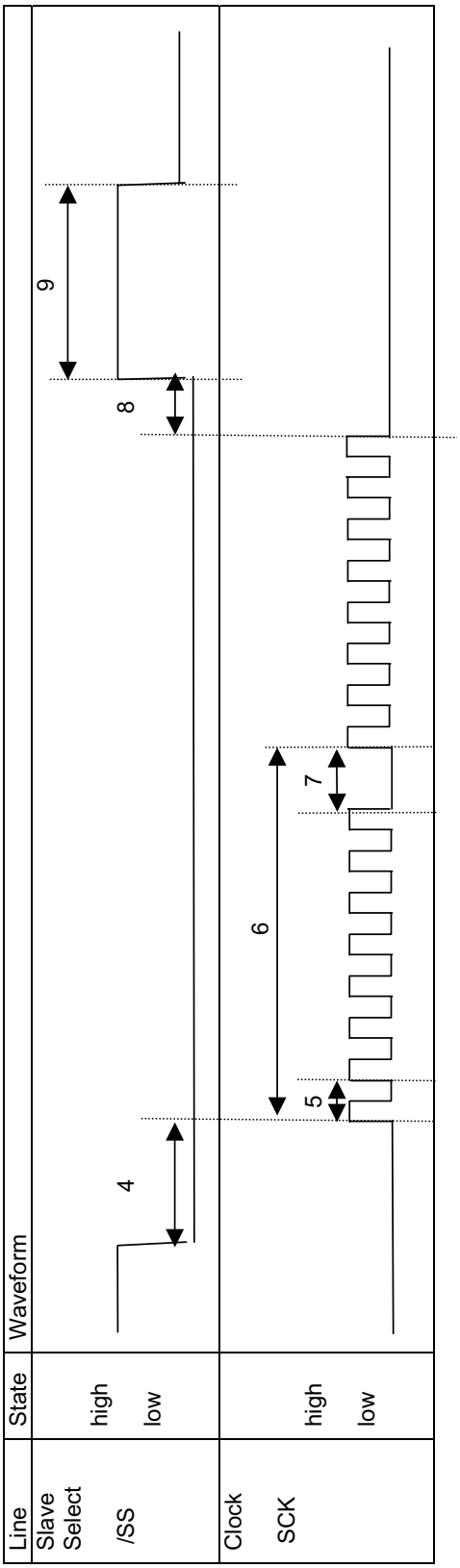


Figure 10. Command Execution Characteristics

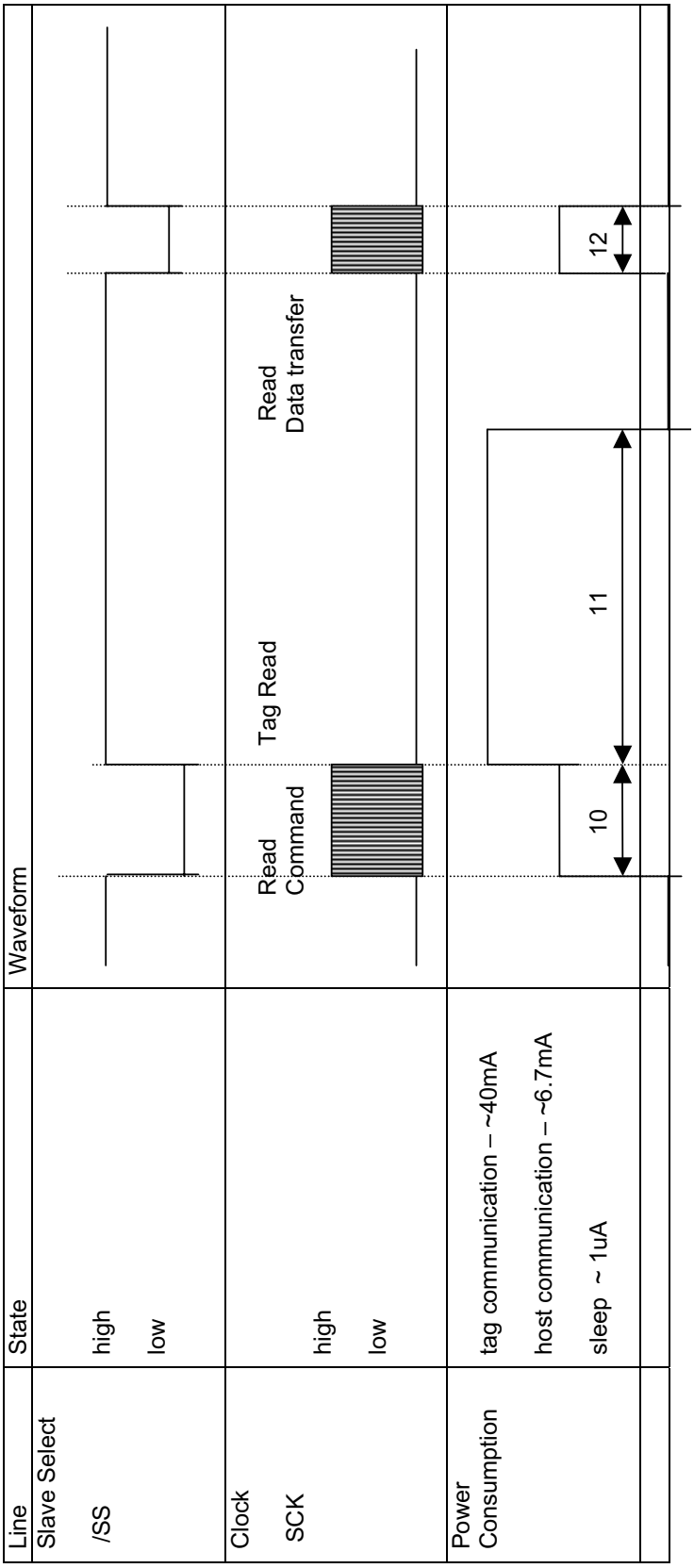


Table 2. Interface Timing Parameters

Id	Description	Min (µs)	Typical	Max (µs)
1	AT90RF135602 Cold Power up time	-	498 ms	-
2	SPI /SS low to exit from sleep mode (warm power up time)	-	20 us	-
3	SPI /SS high to entry into sleep mode	-	20 us	-
4	SPI /SS low to SPI SCK high	3	-	-
5	SPI SCK Period	3.2	-	-
6	SPI Data Rate	poll : 40 non-poll : 50	-	-
7	SPI LSB to MSB period	poll : 10 non-poll : 23	-	-
8	SPI SCK low to SPI /SS high	6	-	-
9	SPI /SS high time	3	-	-
10	transmission of command 0x80 to read 16 bytes		0.8 ms	
11	Reading 16 bytes from mifare ultralight tag		8.0 ms	
12	polling the response to the read		1.3 ms	
	/SS high to MISO tri-state	-	10 ns	-
	/SS low to MISO output	-	15 ns	-

Note:
1. "-" No value applicable
2. The AT90RF135602 will enter its power saving sleep mode when the /SS line is inactive (high) and any tag read/write operation has been completed.
3. The AT90RF135602 will exit its sleep mode when /SS goes active (low).
4. The Host should maintain /SS active only for the duration of the communication, this allows the AT90RF135602 to know when it is safe to enter sleep mode or when its SPI transmission buffer may be updated.
5. The AT90RF135602 will tri-state the MISO line when /SS is high.
6. The AT90RF135602 will enter serial programming mode if /RESET is held low.

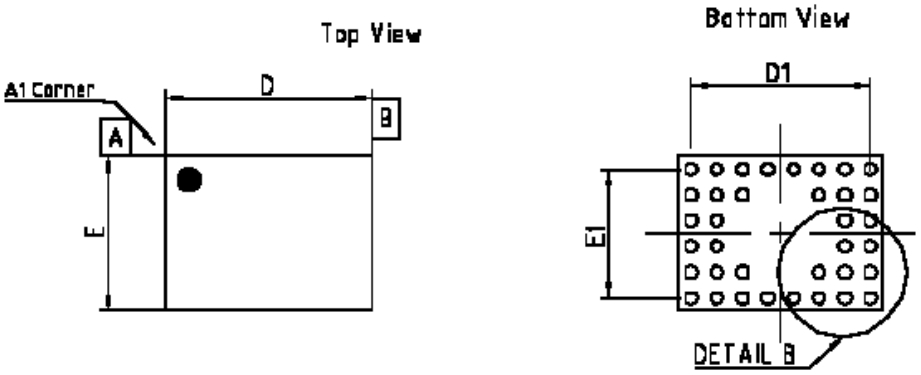
$\overline{\text{RESET}}$	$\overline{\text{SS}}$	Interface Mode
low	-	Reserved
high	high	SPI interface sleeping MISO tri-state
high	low	SPI interface active

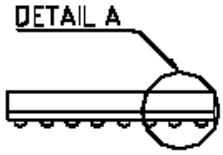
Ordering information

Part Number	Supply Voltage (V)	Temperature Range	Package	Packing	Green Compliance
AT90RF135602-7MTUL	2.7 - 3.3	Industrial	LBGA36	Tray	Yes

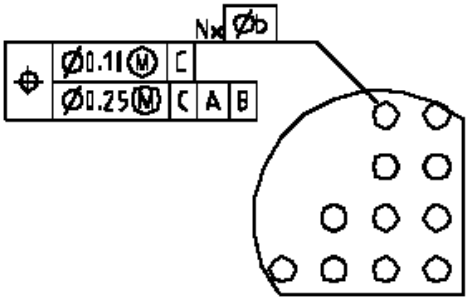
Packaging Information

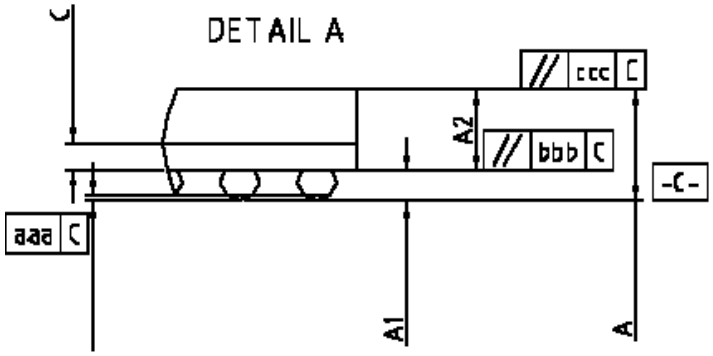
LBGA 36 Pin





DETAIL B





Dimensional Ref.			
REF.	Min.	Nom	Max.
A			1.5
A1	0.35	0.4	0.45
A2		1.12	
D	7.8	8.1	8.2
D1		7	
E	5.8	6.1	6.2
E1		5	
b		1.5	
c	0.28	1.32	0.36
e		1.1	
f		1.5	
m		8 x 6	
n		36	

Dimensional Tol.	
aaa	0.15
bbb	1.21
ccc	0.25

Notes
1. All dimensions in MM
2. 'e' represents the basic solder ball pitch
3. 'm' represents the basic solder ball matrix size. And 'n' is the number of attached solder balls
4. 'b' is measurable at the maximum solder ball diameter parallel the the primary datum –C–
5. Dimension 'aaa' is measured parallel to primary datum –C–
6. Primary datum –C– and the seating plane are defined by the spherical crowns of the solder balls
7. The package surface shall be matte finish charmilles 24 to 27
8. Package warp shall be 1.150 max.
9. Substrate base is BT Resin
11. The over package thickness 'A' already considers collapse balls
11. Reference Jedec MO-192 Issue D, Jan/111

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