

### n FEATURES

- Ÿ Ultra low  $V_{CC}$  operation voltage : 1.9V ~ 3.6V
- Ÿ Very low power consumption :
  - $V_{CC} = 2.0V$  10mA(Max.) operating current  
0.01uA (Typ.) CMOS standby current
  - $V_{CC} = 3.0V$  18mA(Max.) operating current  
0.02uA (Typ.) CMOS standby current
- Ÿ High speed access time :
  - 10 100ns(Max.)
- Ÿ Automatic power down when chip is deselected
- Ÿ Easy expansion with  $\overline{CE}$  and  $\overline{OE}$  options
- Ÿ I/O Configuration x8/x16 selectable by  $\overline{LB}$  and  $\overline{UB}$  pin.
- Ÿ Three state outputs and TTL compatible
- Ÿ Fully static operation
- Ÿ Data retention supply voltage as low as 1.5V

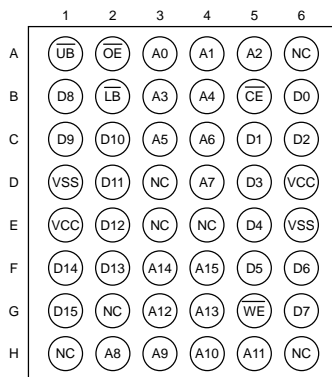
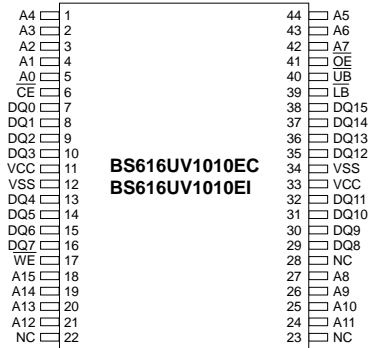
### n DESCRIPTION

The BS616UV1010 is a high performance, ultra low power CMOS Static Random Access Memory organized as 65,536 words by 16 bits and operates from a wide range of 1.9V to 3.6V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed and low power features with typical CMOS standby current of 0.01uA and maximum access time of 100ns in 1.9V operation. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and active LOW output enable ( $\overline{OE}$ ) and three-state output drivers. The BS616UV1010 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The BS616UV1010 is available in JEDEC standard 44-pin TSOP II and 48-ball BGA package.

### n PRODUCT FAMILY

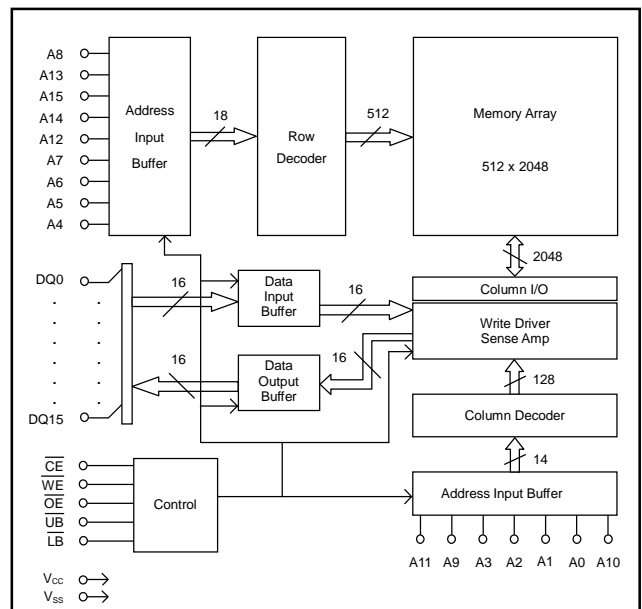
PRODUCT FAMILY	OPERATING TEMPERATURE	$V_{CC}$ RANGE	SPEED (ns)	POWER DISSIPATION				PKG TYPE
				STANDBY ( $I_{CCSBY}$ , Max)		Operating ( $I_{CC}$ , Max)		
				$V_{CC}=3.0V$	$V_{CC}=2.0V$	$V_{CC}=3.0V$	$V_{CC}=2.0V$	
BS616UV1010EC	+0°C to +70°C	1.9V ~ 3.6V	100	1.0uA	0.5uA	20mA	15mA	TSOP2-44
BS616UV1010AC								BGA-48-0608
BS616UV1010EI	-40°C to +85°C	1.9V ~ 3.6V	100	1.5uA	1.0uA	20mA	15mA	TSOP2-44
BS616UV1010AI								BGA-48-0608

### n PIN CONFIGURATIONS



48-ball BGA top view

### n BLOCK DIAGRAM



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**n PIN DESCRIPTIONS**

Name	Function
<b>A0-A15 Address Input</b>	These 16 address inputs select one of the 65,536 x 16-bit words in the RAM
<b><math>\overline{\text{CE}}</math> Chip Enable 1 Input</b>	$\overline{\text{CE}}$ is active LOW. Chip enable must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and is in standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
<b><math>\overline{\text{WE}}</math> Write Enable Input</b>	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{\text{WE}}$ is HIGH and $\overline{\text{OE}}$ is LOW, output data will be present on the DQ pins; when $\overline{\text{WE}}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
<b><math>\overline{\text{OE}}</math> Output Enable Input</b>	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{\text{OE}}$ is inactive.
<b><math>\overline{\text{LB}}</math> and <math>\overline{\text{UB}}</math> Data Byte Control Input</b>	Lower byte and upper byte data input/output control pins.
<b>DQ0-DQ15 Data Input/Output Ports</b>	There 16 bi-directional ports are used to read data from or write data into the RAM.
<b>V<sub>CC</sub></b>	Power Supply
<b>V<sub>SS</sub></b>	Ground

**n TRUTH TABLE**

MODE	$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{LB}}$	$\overline{\text{UB}}$	DQ0~DQ7	DQ8~DQ15	V <sub>CC</sub> CURRENT
Not selected (Power Down)	H	X	X	X	X	High Z	High Z	I <sub>CCSB</sub> , I <sub>CCSB1</sub>
Output Disabled	L	H	H	X	X	High Z	High Z	I <sub>CC</sub>
Read	L	H	L	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	I <sub>CC</sub>
				H	L	High Z	D <sub>OUT</sub>	I <sub>CC</sub>
				L	H	D <sub>OUT</sub>	High Z	I <sub>CC</sub>
Write	L	L	X	L	L	D <sub>IN</sub>	D <sub>IN</sub>	I <sub>CC</sub>
				H	L	X	D <sub>IN</sub>	I <sub>CC</sub>
				L	H	D <sub>IN</sub>	X	I <sub>CC</sub>

NOTES: H means V<sub>IH</sub>; L means V<sub>IL</sub>; X means don't care (Must be V<sub>IH</sub> or V<sub>IL</sub> state)

**n ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>**

SYMBOL	PARAMETER	RATING	UNITS
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to 7.0	V
T <sub>BIAS</sub>	Temperature Under Bias	-40 to +125	°C
T <sub>STG</sub>	Storage Temperature	-60 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W
I <sub>OUT</sub>	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**n OPERATING RANGE**

RANG	AMBIENT TEMPERATURE	V <sub>CC</sub>
Commercial	0°C to + 70°C	1.9V ~ 3.6V
Industrial	-40°C to + 85°C	1.9V ~ 3.6V

**n CAPACITANCE <sup>(1)</sup> (T<sub>A</sub> = 25°C, f = 1.0MHz)**

SYMBOL	PAMAMETER	CONDITIONS	MAX.	UNITS
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>IO</sub>	Input/Output Capacitance	V <sub>IO</sub> = 0V	8	pF

1. This parameter is guaranteed and not 100% tested.

**n DC ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = -40°C to +85°C)**

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP. <sup>(1)</sup>	MAX.	UNITS	
V <sub>CC</sub>	Power Supply		1.9	--	3.6	V	
V <sub>IL</sub>	Input Low Voltage	V <sub>CC</sub> =2.0V	-0.5 <sup>(2)</sup>	--	0.6	V	
		V <sub>CC</sub> =3.0V			0.8		
V <sub>IH</sub>	Input High Voltage	V <sub>CC</sub> =2.0V	1.4	--	V <sub>CC</sub> +0.2 <sup>(3)</sup>	V	
		V <sub>CC</sub> =3.0V	2.0				
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0V to V <sub>CC</sub>	--	--	1	µA	
I <sub>LO</sub>	Output Leakage Current	V <sub>IO</sub> = 0V to V <sub>CC</sub> , CE = V <sub>IH</sub> or OE = V <sub>IH</sub>	--	--	1	µA	
V <sub>OL</sub>	Output Low Voltage	V <sub>CC</sub> = Max, I <sub>OL</sub> = 1.0mA	V <sub>CC</sub> =2.0V	--	0.2	V	
		V <sub>CC</sub> = Max, I <sub>OL</sub> = 2.0mA	V <sub>CC</sub> =3.0V		0.4		
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.5mA	V <sub>CC</sub> =2.0V	V <sub>CC</sub> -0.2	--	V	
		V <sub>CC</sub> = Min, I <sub>OH</sub> = -1.0mA	V <sub>CC</sub> =3.0V				2.4
I <sub>CC</sub>	Operating Power Supply Current	CE = V <sub>IL</sub> , I <sub>IO</sub> = 0mA, f = F <sub>MAX</sub> <sup>(4)</sup>	V <sub>CC</sub> =2.0V	--	--	15	mA
			V <sub>CC</sub> =3.0V			20	
I <sub>CCSB</sub>	Standby Current – TTL	CE = V <sub>IH</sub> , I <sub>IO</sub> = 0mA	V <sub>CC</sub> =2.0V	--	--	0.5	mA
			V <sub>CC</sub> =3.0V			1.0	
I <sub>CCSB1</sub> <sup>(5)</sup>	Standby Current – CMOS	CE ≥ V <sub>CC</sub> -0.2V V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤ 0.2V	V <sub>CC</sub> =2.0V	--	0.01	1.0	µA
			V <sub>CC</sub> =3.0V			0.02	

1. Typical characteristics are at T<sub>A</sub>=25°C.

2. Undershoot: -1.0V in case of pulse width less than 20 ns.

3. Overshoot: V<sub>CC</sub>+1.0V in case of pulse width less than 20 ns.

4. F<sub>MAX</sub>=1/t<sub>RC</sub>.

5. I<sub>CCSB1(MAX.)</sub> is 0.5µA/1.0µA at V<sub>CC</sub>=2.0V/3.0V and T<sub>A</sub>=70°C.

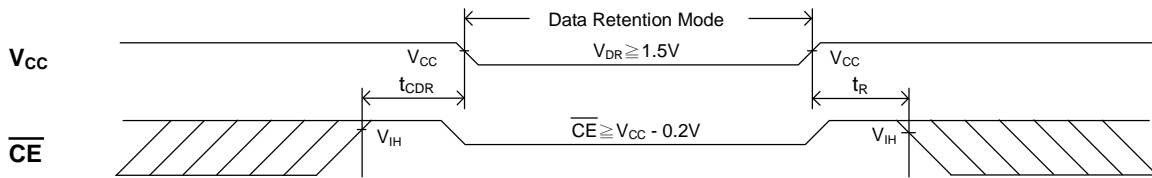
**n DATA RETENTION CHARACTERISTICS (T<sub>A</sub> = -40°C to +85°C)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. <sup>(1)</sup>	MAX.	UNITS
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	CE ≥ V <sub>CC</sub> -0.2V V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤ 0.2V	1.5	--	--	V
I <sub>CCDR</sub> <sup>(3)</sup>	Data Retention Current	CE ≥ V <sub>CC</sub> -0.2V V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤ 0.2V	--	0.01	0.3	µA
t <sub>CDR</sub>	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t <sub>R</sub>	Operation Recovery Time		t <sub>RC</sub> <sup>(2)</sup>	--	--	ns

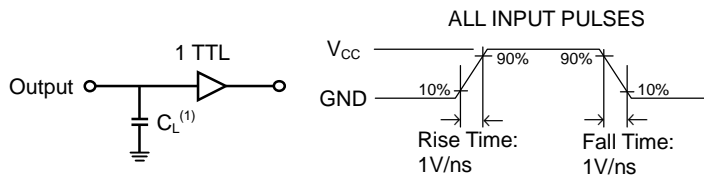
1. V<sub>CC</sub>=1.5V, T<sub>A</sub>=25°C.

2. t<sub>RC</sub> = Read Cycle Time.

3. I<sub>CCRD\_Max.</sub> is 0.2µA at T<sub>A</sub>=70°C.

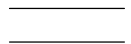




**n LOW  $V_{CC}$  DATA RETENTION WAVEFORM (1) ( $\overline{CE}$  Controlled)**

**n AC TEST CONDITIONS  
(Test Load and Input/Output Reference)**

Input Pulse Levels	$V_{CC} / 0V$	
Input Rise and Fall Times	1V/ns	
Input and Output Timing Reference Level	0.5 $V_{CC}$	
Output Load	$t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}$	$C_L = 5pF + 1TTL$
	Others	$C_L = 30pF + 1TTL$



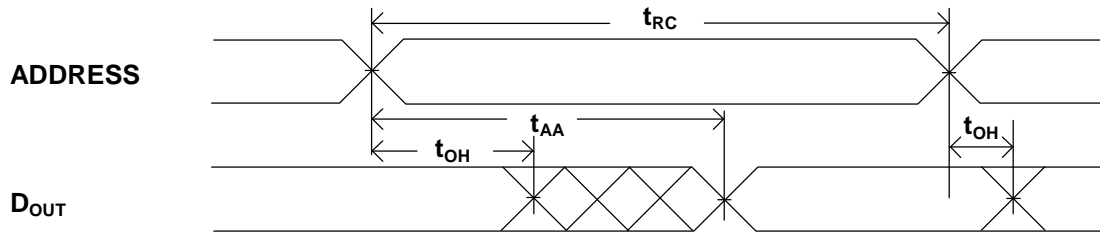
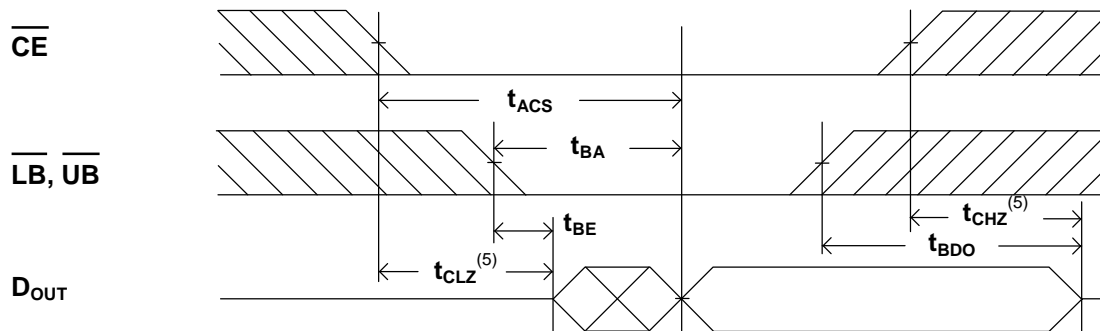
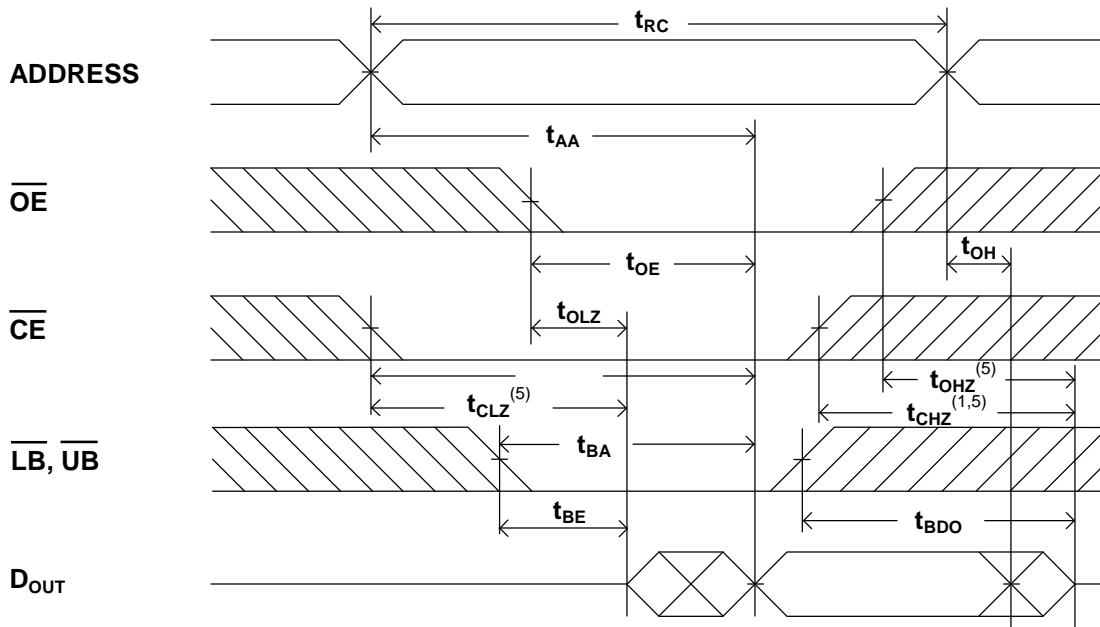
1. Including jig and scope capacitance.

**n KEY TO SWITCHING WAVEFORMS**

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM "H" TO "L"	WILL BE CHANGE FROM "H" TO "L"
	MAY CHANGE FROM "L" TO "H"	WILL BE CHANGE FROM "L" TO "H"
	DON'T CARE ANY CHANGE PERMITTED	CHANGE : STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

**n AC ELECTRICAL CHARACTERISTICS ( $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )**
**READ CYCLE**

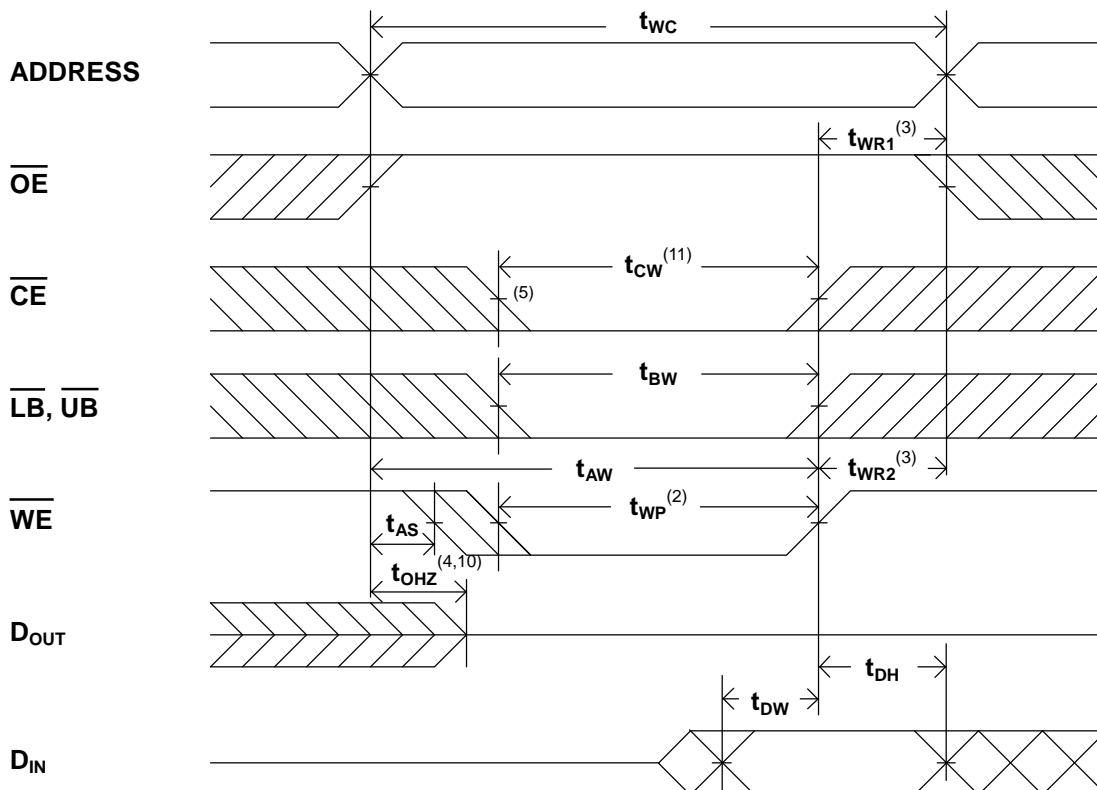
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 100ns			UNITS
			MIN.	TYP.	MAX.	
$t_{AVAX}$	$t_{RC}$	Read Cycle Time	100	--	--	ns
$t_{AVQX}$	$t_{AA}$	Address Access Time	--	--	100	ns
$t_{ELQV}$	$t_{ACS}$	Chip Select Access Time ( $\overline{CE}$ )	--	--	100	ns
$t_{BLQV}$	$t_{BA}$	Data Byte Control Access Time ( $\overline{LB}, \overline{UB}$ )	--	--	100	ns
$t_{GLQV}$	$t_{OE}$	Output Enable to Output Valid	--	--	50	ns
$t_{ELQX}$	$t_{CLZ}$	Chip Select to Output Low Z ( $\overline{CE}$ )	15	--	--	ns
$t_{BLQX}$	$t_{BE}$	Data Byte Control to Output Low Z ( $\overline{LB}, \overline{UB}$ )	15	--	--	ns
$t_{GLQX}$	$t_{OLZ}$	Output Enable to Output Low Z	15	--	--	ns
$t_{EHQZ}$	$t_{CHZ}$	Chip Select to Output High Z ( $\overline{CE}$ )	--	--	40	ns
$t_{BHQZ}$	$t_{BDO}$	Data Byte Control to Output High Z ( $\overline{LB}, \overline{UB}$ )	--	--	40	ns
$t_{GHQZ}$	$t_{OHZ}$	Output Enable to Output High Z	--	--	35	ns
$t_{AVQX}$	$t_{OH}$	Data Hold from Address Change	15	--	--	ns

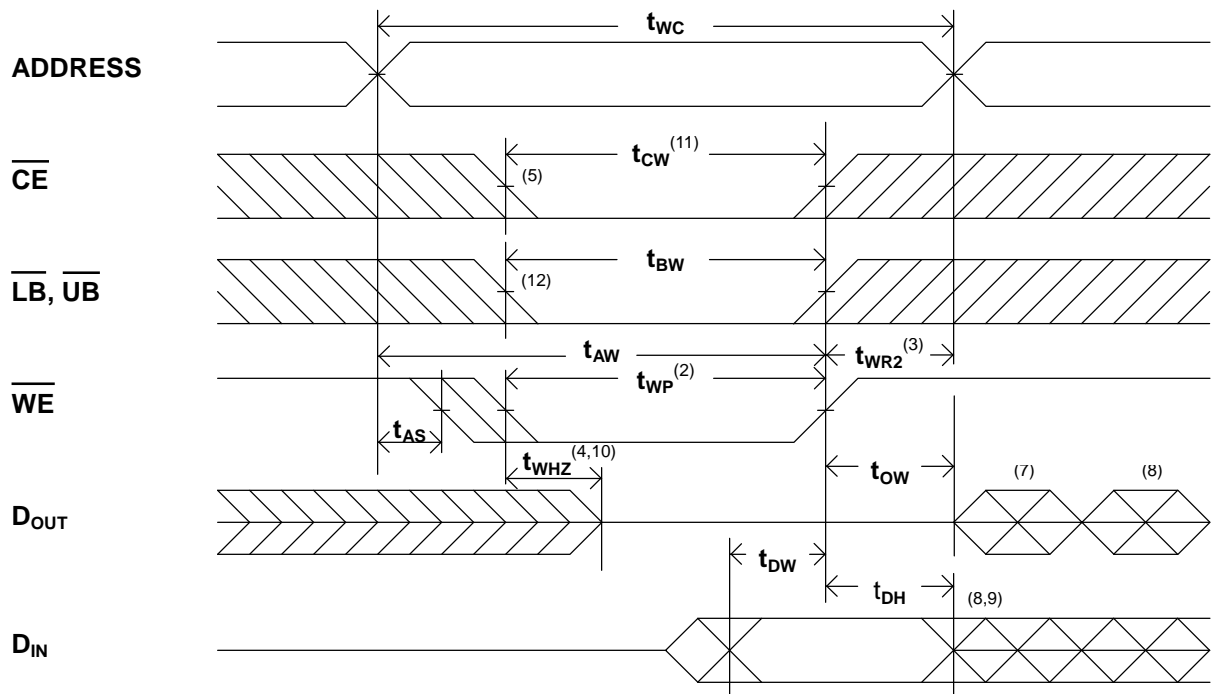
**n SWITCHING WAVEFORMS (READ CYCLE)**
**READ CYCLE 1** <sup>(1,2,4)</sup>

**READ CYCLE 2** <sup>(1,3,4)</sup>

**READ CYCLE 3** <sup>(1,4)</sup>

**NOTES:**

1.  $\overline{WE}$  is high in read Cycle.
2. Device is continuously selected when  $\overline{CE} = V_{IL}$ .
3. Address valid prior to or coincident with  $\overline{CE}$  transition low.
4.  $\overline{OE} = V_{IL}$ .
5. Transition is measured  $\pm 500\text{mV}$  from steady state with  $C_L = 5\text{pF}$ .  
The parameter is guaranteed but not 100% tested.

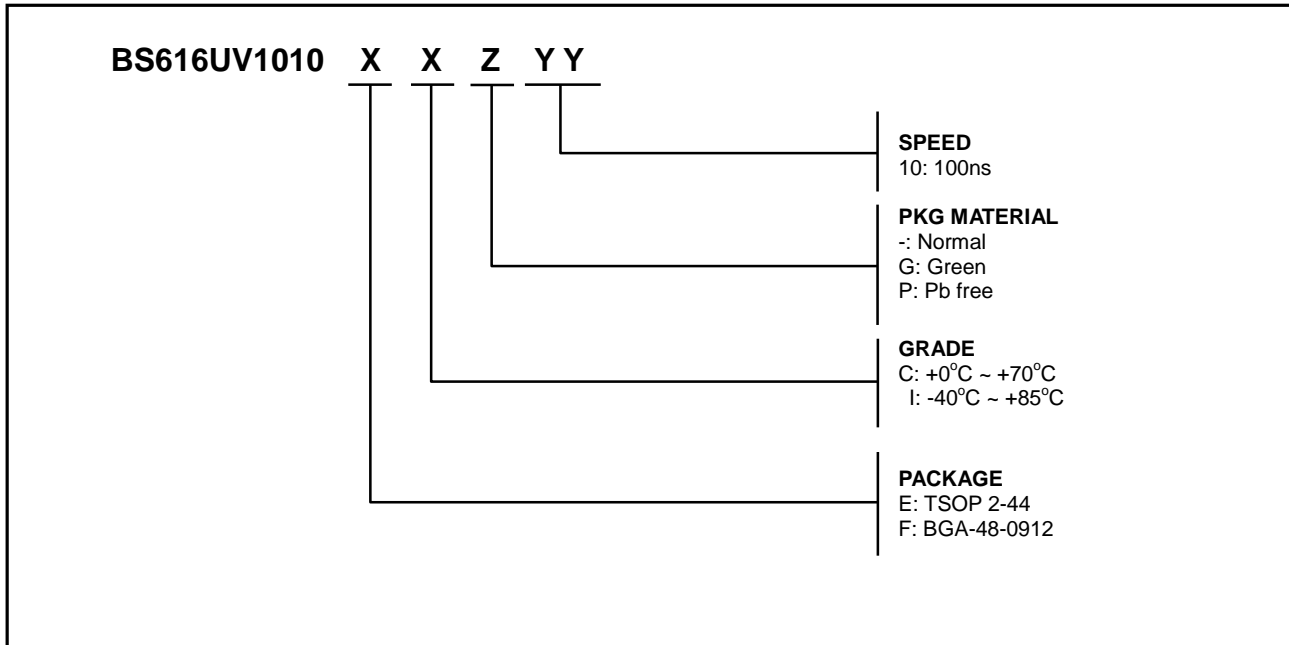
**n AC ELECTRICAL CHARACTERISTICS ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )**
**WRITE CYCLE**

JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 100ns			UNITS
			MIN.	TYP.	MAX.	
$t_{AVAX}$	$t_{WC}$	Write Cycle Time	100	--	--	ns
$t_{AVWL}$	$t_{AS}$	Address Set up Time	0	--	--	ns
$t_{AVWH}$	$t_{AW}$	Address Valid to End of Write	100	--	--	ns
$t_{ELWH}$	$t_{CW}$	Chip Select to End of Write	100	--	--	ns
$t_{BLWH}$	$t_{BW}$	Data Byte Control to End of Write ( $\overline{LB}$ , $\overline{UB}$ )	100	--	--	ns
$t_{WLWH}$	$t_{WP}$	Write Pulse Width	50	--	--	ns
$t_{WHAX}$	$t_{WR}$	Write Recovery Time ( $\overline{CE}$ , $\overline{WE}$ )	0	--	--	ns
$t_{WLQZ}$	$t_{WHZ}$	Write to Output High Z	--	--	40	ns
$t_{DVWH}$	$t_{DW}$	Data to Write Time Overlap	40	--	--	ns
$t_{WHDX}$	$t_{DH}$	Data Hold from Write Time	0	--	--	ns
$t_{GHQZ}$	$t_{OHZ}$	Output Disable to Output in High Z	--	--	40	ns
$t_{WHQX}$	$t_{OW}$	End of Write to Output Active	10	--	--	ns

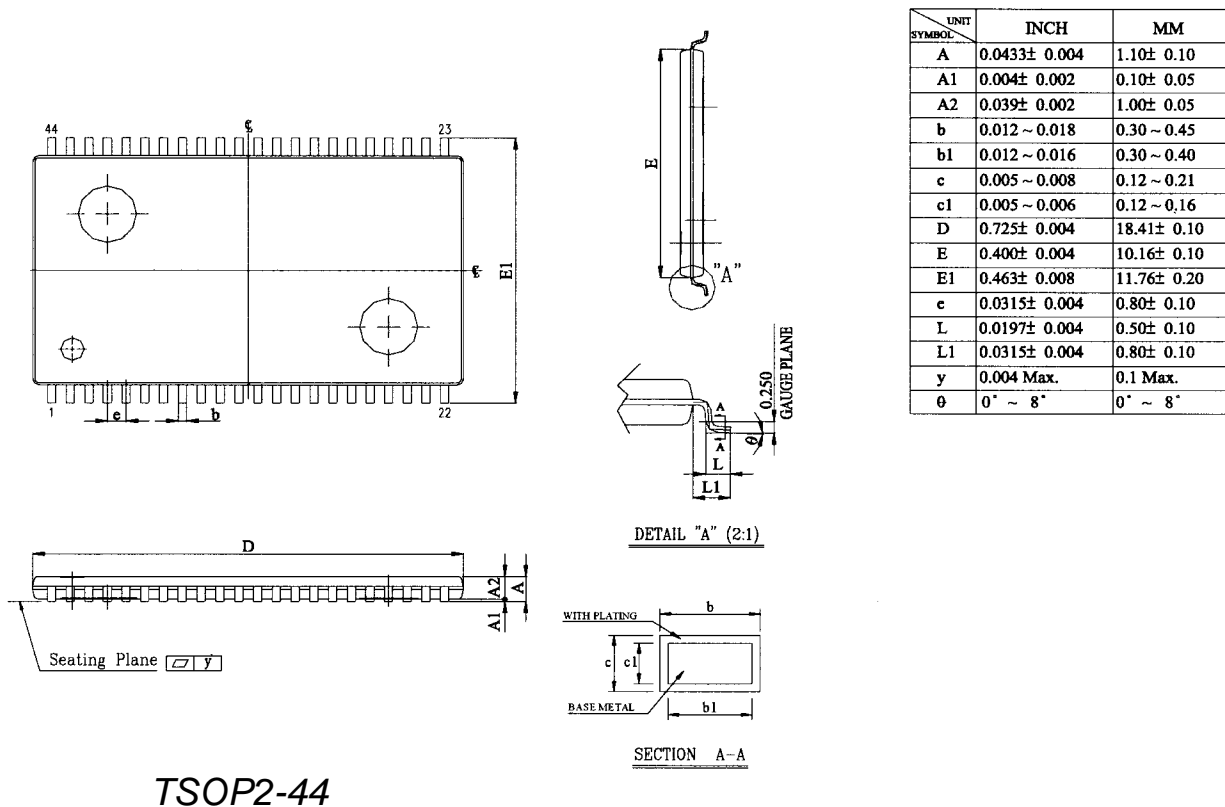
**n SWITCHING WAVEFORMS (WRITE CYCLE)**
**WRITE CYCLE 1 <sup>(1)</sup>**


**WRITE CYCLE 2** <sup>(1,6)</sup>

**NOTES:**

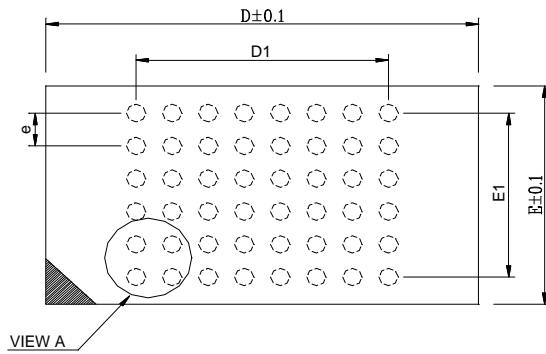
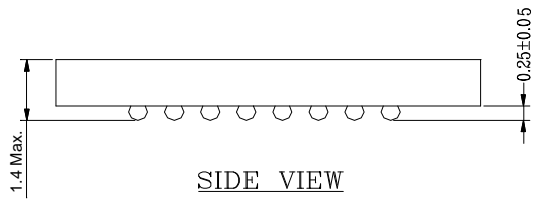
1.  $\overline{WE}$  must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  and  $\overline{WE}$  low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3.  $t_{WR}$  is measured from the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the  $\overline{CE}$  low transition occurs simultaneously with the  $\overline{WE}$  low transitions or after the  $\overline{WE}$  transition, output remain in a high impedance state.
6. OE is continuously low ( $OE = V_{IL}$ ).
7.  $D_{OUT}$  is the same phase of write data of this write cycle.
8.  $D_{OUT}$  is the read data of next address.
9. If CE is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured  $\pm 500\text{mV}$  from steady state with  $C_L = 5\text{pF}$ .  
The parameter is guaranteed but not 100% tested.
11.  $t_{CW}$  is measured from the later of  $\overline{CE}$  going low to the end of write.
12. The change of Read/Write cycle must accompany with  $\overline{CE}$  or address toggled.

**n ORDERING INFORMATION**

**Note:**

BSI (Brilliance Semiconductor Inc.) assumes no responsibility for the application or use of any product or circuit described herein. BSI does not authorize its products for use as critical components in any application in which the failure of the BSI product may be expected to result in significant injury or death, including life-support systems and critical medical instruments.

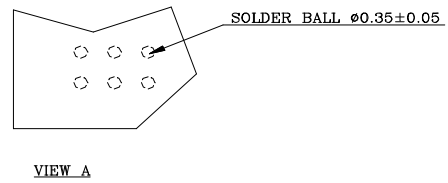
**n PACKAGE DIMENSIONS**




**n PACKAGE DIMENSIONS (continued)**

**NOTES:**

- 1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
- 2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.
- 3: SYMBOL 'N' IS THE NUMBER OF SOLDER BALLS.

BALL PITCH e = 0.75				
D	E	N	D1	E1
8.0	6.0	48	5.25	3.75



*48 mini-BGA (6 x 8)*