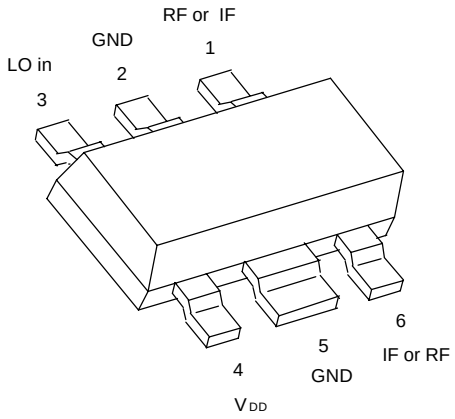
Preliminary Data

* **Ultralinear Mixer** with integrated LO-Buffer
* Very high **Input-IP3 of typical 25dBm**
* Very low **LO-Power demand of typ. 0dBm**
* Suited for Up- and Down-Conversion
* Wide LO-Frequency Range
  <500MHz to >2,5GHz
* Wide LO-Level Range
* Single ended Ports
* RF- and IF-Port Impedance 50 Ohm
* Operating Voltage Range: < 3 to 6V
* Very low Current Consumption of typical 7mA
* All Gold Metallisation



ESD: **E**lectro**s**tatic **d**ischarge sensitive device
Observe handling Precautions!

Type	Marking	Ordering code (tape and reel)	Package [1]
CMY210	**M3**	**Q62702 M 0016**	**MW-6**

Maximum Ratings	**Port**	**Symbol**	**Value**		**Unit**
			min	**max**	
Supply Voltage	4	V_{DD}	0	6	V
DC-Voltage at LO Input	3	V_3	-3	0,5	V
DC-Voltage at RF-IF Ports [2]	1, 6	$V_{1,6}$	- 0,5	+ 0,5	V
Power into RF-IF Ports	1, 6	$P_{in,RF}$		10	dBm
Power into LO Input	3	$P_{in,LO}$		10	dBm
Channel Temperature		T_{Ch}		150	°C
Storage Temperature		T_{stg}	-55	150	°C
Thermal Resistance					
Channel to Soldering Point (GND)		R_{thChS}	≤100		K/W

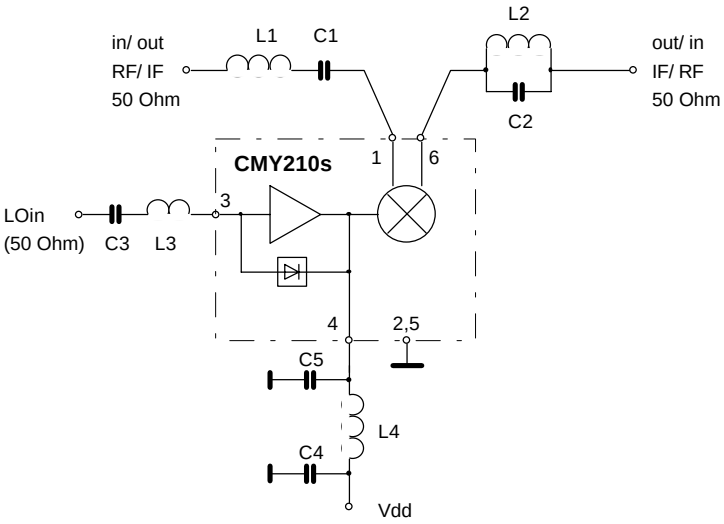
1) For detailed dimensions see chapter Package Outlines
2) For DC test purposes only, no DC voltages at pins 1, 6 in application

Electrical Characteristics

Test conditions: T_a = 25°C; V_{DD}= 3V, see test circuit; f_{RF} = 1620MHz; f_{LO} = 1500MHz; P_{LO} = 0dBm; f_{IF} = 120MHz, unless otherwise specified:

Parameter, Test Conditions	Symbol	min	typ	max	Unit
Operating Current	I_{op}	-	7	-	mA
Conversion Loss	L_c	-	5,5	-	dB
SSB Noise Figure	F_{ssb}	-	5,5	-	dB
2 Tone 3rd Order IMD $P_{RF1} = P_{RF2}$ = -3dBm f_{RF1} = 1615MHz; f_{RF2} = 1620MHz; f_{LO} =1500MHz	d_{IM3}	-	56	-	dBc
3rd Order Input Intercept Point	$IP3_{in}$	-	25	-	dBm
P_{-1dB} Input Power	P_{-1dB}	-	20	-	dBm
LO Leakage at RF/IF-Port (1,6)	$P_{LO\ 1,6}$	-	-6	-	dBm

Test circuit / application example



Notes for external elements:

L1, C1: Filter for upper frequency;
C2, L2: Filter for lower frequency;
each filter is a throughpath for the desired frequency (RF or IF) and isolates the other frequency (IF or RF) and its harmonics.
These two filters must be connected to pin 1 and pin 6 directly.
Parasitic capacitances at the ports 1 and 6 must be as small as possible.
L4 and C5 are optimized by indicating lowest I_{op} at used LO-frequency; same procedure for L3.
The ports 1, 3 and 6 must be DC open.

f *LO*	L1	C1	L2	C2	L3	C3	L4	C4	C5
MHz	nH	pF	nH	pF	nH	pF	nH	pF	pF
500	11	8.2	19	4.7	6	47	19	47	3.3
1000	7	4.7	9	3.3	6	33	16	33	0
1500	4	2.2	7,5	2.2	6	18	8.5	18	0
2000	*)	2.2	*)	1.5	4	15	*)	15	0
2500	*)	2.2	*)	1.5	3	15	*)	15	0
notes next pg	1)	1)	1)	1)	3)	3)	2)	2)	2)

Approximate values of used elements for down- (or up-) conversion with a lower frequency of 10MHz to 120MHz (IF or RF; in or out); parasitics will cause deviations; therefore exact values will be defined by application, especially for *).

General description and notes:

The CMY 210 is an all port single ended general purpose Up- and Down-Converter.
It combines small conversion losses and excellent intermodulation characteristics with a low demand of LO- and DC-power.
The internal level controlled LO-Buffer enables a good performance over a wide LO level range.
The internal mixers principle with one port RF and IF requires a frequency separation at pin 1 and 6 respectively.

Note 1:
Best performance with lowest conversion loss is achieved when each circuit or device for the frequency separation meets the following requirements:

Input Filter: Throughpass for the signal to be mixed; reflection of the mixed signal and the harmonics of both.

Output Filter: Throughpass for the mixed signal and reflection of the signal to be mixed and the harmonics of both.

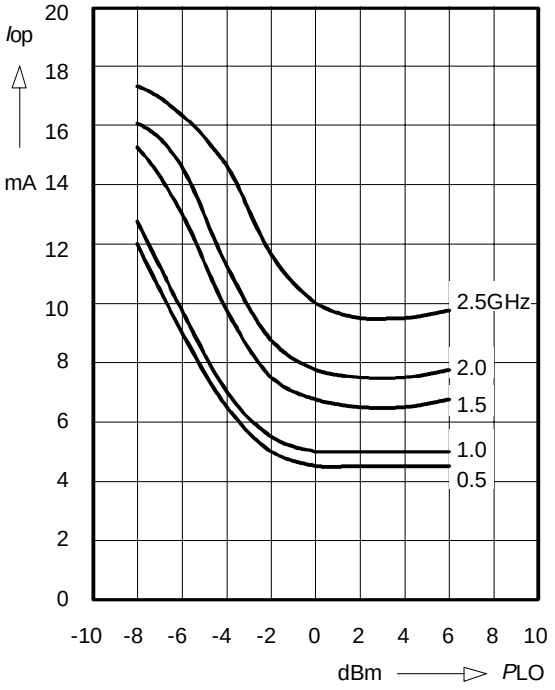
The impedance for the reflecting frequency range of each filter toward the ports 1 and 6 should be as high as possible.
In the simplest case a series- and a parallel- resonator circuit will meet these requirements but also others as appropriate drop in filters or micro stripline elements can be used.
The two branches with filters should meet immediately at the package leads of the port 1 and 6.
Parasitic capacitances at these ports must be kept as small as possible.
The mixer also can be driven with a source- and a load impedance different to 50Ω, but performance will degrade at larger deviations.

Note 2:
The LO-Buffer needs an external inductor L4 at port 4; the value of inductance depends on the LO frequency. It is tuned for minimum I_{op} consumption into port 4.
At lower LO frequencies it can be reduced by an additonal capacitor C5.

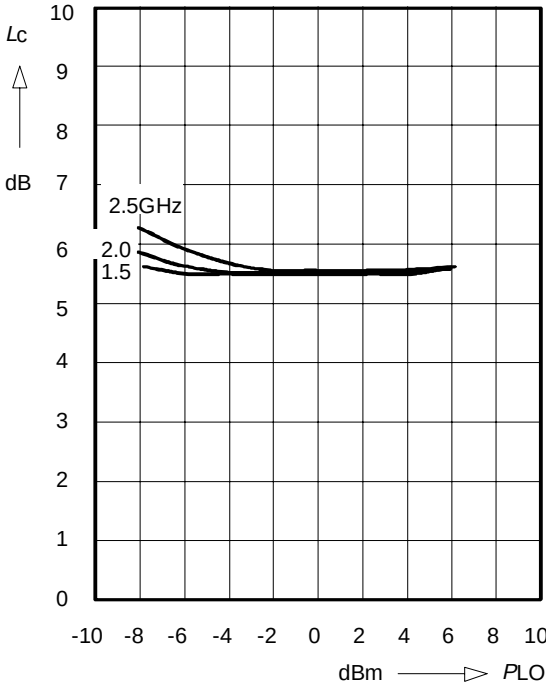
Note 3:
The LO Input impedance at Port 3 can be matched with a series inductor. It also can be tuned for a minimum current I_{op} into port 4. C3 is a DC blocking capacitor.
Since the input impedance of port 3 can be slightly negative at lower frequencies, the source reflection coefficient should be kept below 0.8 ($Z_0 = 50\ \Omega$) within this frequency range.

The Conversion Noise Figure Fssb is corresponding with the value of Conversion Loss L_c. The LO signal must be clean of noise and spurious at the frequencies $f_{LO} \pm f_{IF.}$

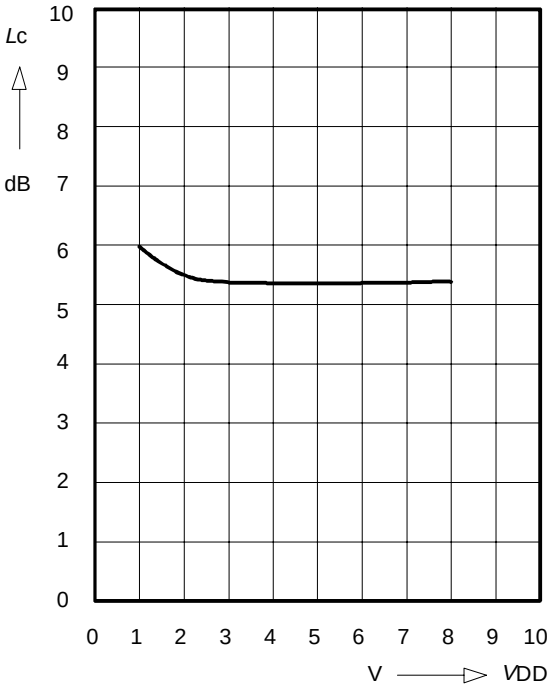
Operating Current $I_{op} = f(P_{LO})$
V_{DD} = 3V
f_{LO} = Parameter



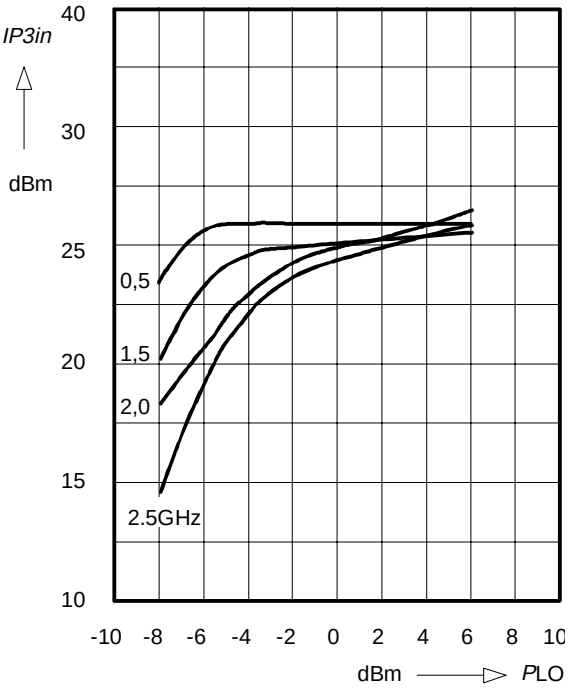
Conversion Loss $L_C = f(P_{LO})$
V_{DD} = 3V; f_{IF} = 120MHz
f_{LO} = Parameter



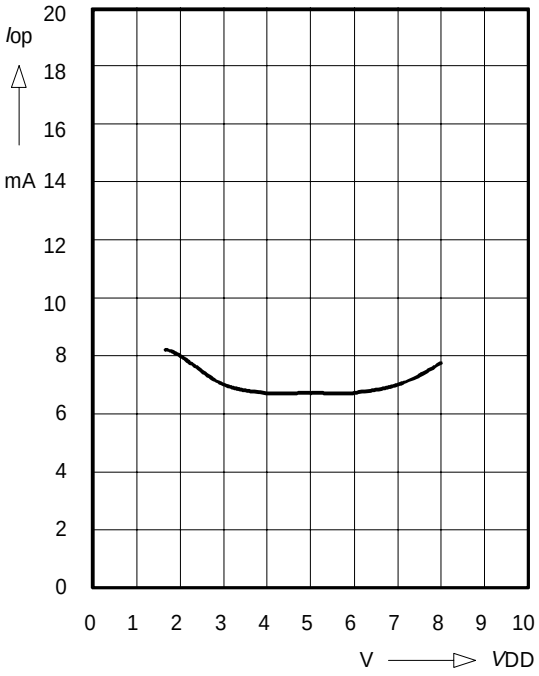
Conversion Loss $L_C = f(V_{DD})$
P_{LO} = 0dBm
f_{LO} = 1500MHz; f_{IF} = 120MHz



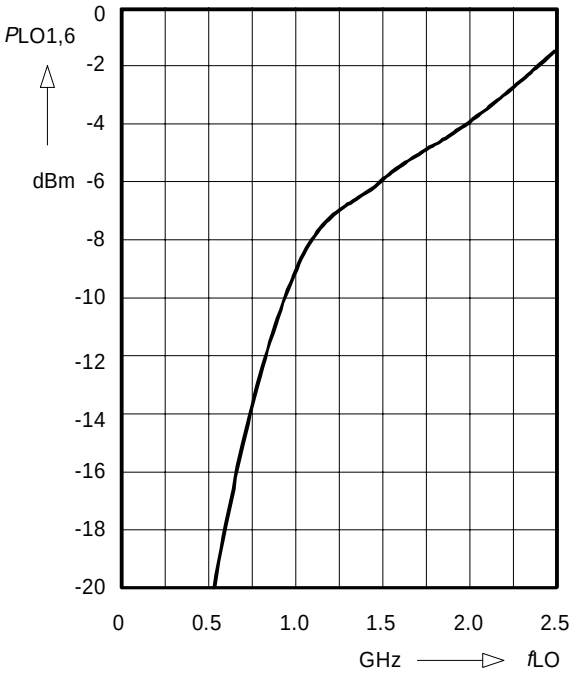
Third Order IP3 $IP3in = f(P_{LO})$
P_{In} = 2 x -3dBm; f_{IF} = 40/45MHz
V_{DD} = 3V; f_{LO} = Parameter;



Operating Current $I_{op} = f(V_{DD})$
P_{LO} = 0dBm
f_{LO} = 1500MHz

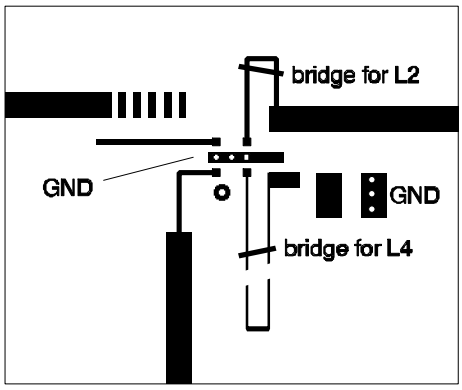


LO-Leakage at Port 1, 6 $P_{LO1,6} = f(f_{LO})$
P_{LO} = 0dBm
V_{DD} = 3V



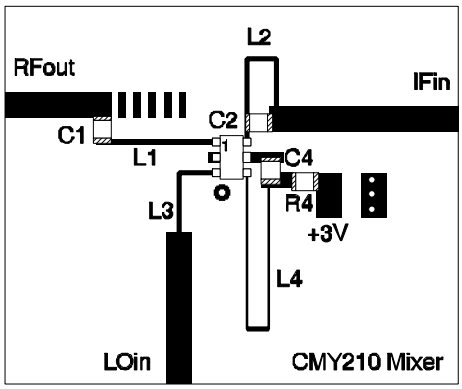
Additional informations and an example of a general purpose mixer pcb:

This general purpuse mixer demonstration board is used to show the performance of the CMY 210. The hints below will be helpful to achieve good intermodulation behaviour.



Material: Epoxy; size 24mm x 30mm; thickness 1mm

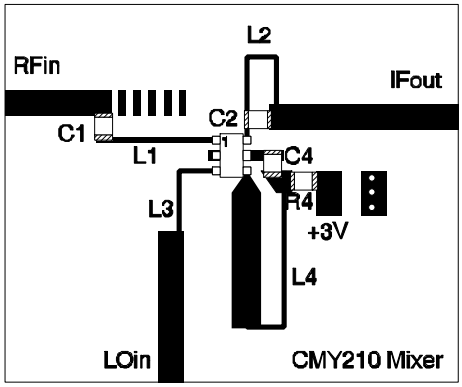
A good ground connection for CMY210 is necessary; here it is realized by 3 vias **under** the CMY 210 device. Best IM3 performance is obtained, when the capacitor C4 is grounded at the upper CMY 210 ground line without any additional vias (so the RF-Signal is encoupled from the LO-buffer best possible). Frequency tuning is done by selecting suitable capacitors C1 and C2, positioning C1 along the L1-line and by reducing the inductance of L2 and L4 by a bridge; unnecessary lines should be disconnected.



This example showes an up-converter.

The IM3 performance of upconverters mostly can be improved by tuning L4 slightly smaller then required for a minimum current consumption.

In other words, the resonant frequency of the buffer circuit at PIN4 (internal capacitor and L4) is tuned by L4 to a frequency slightly above the L.O.-frequency.



This example showes a down-converter.

Here an improved IM3-performance mostly can be obtained by a more capacitive load at CMY 210 port pin 4.
Here it is realized by a broader part of the L4 inductor line toward to port 4 and tuning L4 to a value sligthly smaller then for a minimum current consumption into port 4.

In other words, the resonant frequency of the buffer circuit at PIN4 (internal capacitor and L4) is tuned by L4 to a frequency slightly above the L.O.-frequency.